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MULTICARRIER MODULATED MULTI LEVEL INVERTER BASED DVR AND DSTATCOM FOR MITIGATING SWELL

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ABSTRACT

The most commonly occurring power quality issue such as voltage swell may cause mal- operation and loss of production. This paper presents voltage swell reduction technique using multi-level inverter based DVR and DSTATCOM employing CBSVPWM algorithm. SVPWM generates fewer harmonics when compared to SPWM. However, as the number of levels in the inverter output voltage increases, the control complexity also increases. To reduce the complexity involved in conventional SVPWM, a novel modulation scheme, CBSVPWM is presented in this paper. The proposed 3 level and 5 level neutral point clamped DVR and DSTATCOM are simulated using multicarrier based SVPWM technique for generating pulses to the inverter. Simulations carried out using MATLAB/SIMULINK prove that the proposed control algorithm is able to compensate any type of voltage swell and also compensation is perfect with negligible THD.

Keywords: dynamic voltage restorer, distribution static compensator, space vector modulation, neutral point clamped inverter.

INTRODUCTION

The use of sophisticated electrical and electronics equipment such as computers, variable speed drives etc. demand high quality power supply. Power quality issues such as swells, sags and harmonics affect the performance of the sensitive loads. New technologies have introduced flexible controllers to mitigate the power quality problems. A voltage swell is an increase to the value between 1.1 to 1.8 PU in RMS value at power frequency for durations less than 1 minute.

These unwanted voltage swells can be reduced by connecting custom power devices either in series or shunt to the load. DVR and D-STATCOM are two such devices to mitigate swells. DVR is a series device to inject dynamically controlled voltage in series with the system bus voltage and the D-STATCOM is a shunt connected device used to inject a dynamically controlled current in shunt with bus voltage through injection transformers.

In recent years, multilevel inverters have gained importance in medium voltage, high power applications because of their better performance compared to two-level inverters, such as reduced harmonics in output voltage and current, lower dv/dt and lower switching losses. Neutral Point Clamped Inverters are most widely used in distribution system applications because of their own advantages [1].

This paper presents an effective voltage compensation scheme by DVR and DSTATCOM employing CBSVPWM. In conventional SVPWM, sector identification, switching-vector determination and switching-time calculation are time consuming and quite complicated.As the number of inverter output levels increases, the control complexity also increases. To decrease the complexity in the conventional control algorithm, a novel modulation scheme known as carrier based SVPWM is introduced. In this proposed algorithm,

there is no need to use look up table for sector identification and can be easily extended to m- level [2-4].

The present paper employs the most popular Level Shifted Phase Disposition multicarrier modulation method for generating the PWM pattern in which (m-1) carrier signals are compared with the modulating signal to generate 'm' levels in the inverter output voltage [5].

DYNAMIC VOLTAGE RESTORER

DVR is a series connected custom power device to protect sensitive loads from voltage disturbances such as swells, sags and harmonics etc. DVR injects controllable voltage through an injection transformer in series with the bus voltage such that desired voltage magnitude can be maintained at the load as shown in Figure-1. When supply voltage V_s changes, the DVR injects a voltage V_{DVR} so as to maintain the load voltage at desirable level. DVR is simply a VSC that produces an ac output voltage and injects in series with supply voltage through a transformer [6-8].
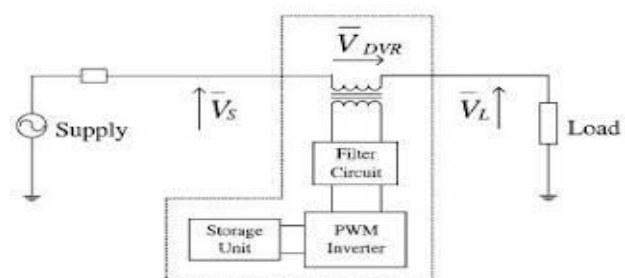

Figure-1. Schematic representation of the DVR.

The main objective of the control circuit is to maintain constant voltage at the point of common coupling

at which a sensitive load is connected, under system disturbances. In this scheme, only rms value of terminal voltage is measured and reactive power measurement is not required [9-10].

The error signal obtained after comparing the reference voltage with measured terminal voltage is used to generate modulating signals in case of SPWM and SVPWM techniques.

This modulating signal is then compared with carrier (triangular) signals to generate the switching signals for the converter switches in both modulation techniques. The SPWM technique is very simple and easy to implement. But, in this paper, it is aimed to prove that Space Vector Pulse Width Modulation is efficient and offers good response.

DISTRIBUTION STATIC COMPENSATOR

The D-STATCOM is a VSC which injects dynamically controlled current in shunt with bus voltage through coupling transformer. This shunt injected current corrects the voltage swells by adjusting the voltage drop across the system impedance. The injected current magnitude can be controlled by adjusting the output of the converter. The DSTATCOM consisting of a VSC, a DC energy storage device and a coupling transformer connected in shunt with the AC system is shown in Figure-2[11-13].

The shunt connected VSC has a multifunctional topology and can be used for the following different purposes:

a) Voltage regulation and compensation of reactive power
b) Correction of power factor and
c) Elimination of current harmonics.

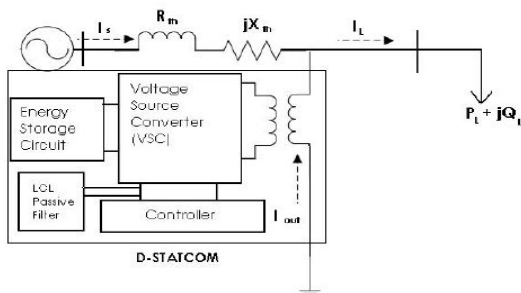In this present work, such device is employed for voltage regulation.

Figure-2. Schematic representation of the D-STATCOM.

From the schematic diagram, it is clear that the value of I_{out} can be controlled by adjusting the output voltage of the converter.
The shunt injected current I_{out} can be written as,

$$I_{out} = I_L - I_S \quad = \quad I_L - (V_{TH} - V_L /Z_{TH}) \tag{1}$$

Where, I_L = load current,
I_S = source current, V_{TH} = thevenin voltage,
V_L = load voltage and Z_{TH} = thevenin impedance

$$I_{out} \angle \gamma = I_L \angle - \theta - \frac{V_{TH}}{Z_{TH}} \angle (\delta - \beta) + \frac{V_L}{Z_{TH}} \angle (-\beta) \tag{2}$$

From the above equation, it is clear that I_{out} will correct the voltage sags or swells by adjusting the voltage drop or rise across the system impedance.

Here also, the control system measures only the rms terminal voltage and reactive power measurement is not required and same control scheme is applicable for both DVR and DSTATCOM.

MULTILEVEL NEUTRAL POINT CLAMPED INVERTER

Figure-3 shows three level neutral point clamped (NPC) topology. Each leg consists of four switches and two clamping diodes. The DC supply is composed of two capacitors in series and the voltage is split into three levels ($+V_{dc/2}$, 0, $-V_{dc/2}$) thereby reducing the stress on the switches.
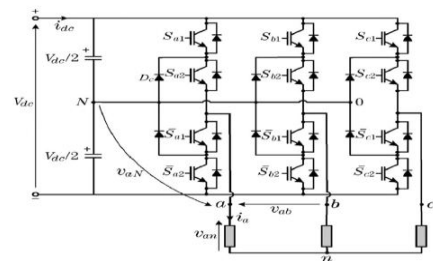

Figure-3. Three-level NPC inverter topology.

The phase A output voltage Vao can have three different levels: +Vdc/2, 0, -Vdc/2. For voltage level+Vdc/2,Sa1 and Sa2 are turned ON, for 0 level Sa2 and Sa1' are turned ON and for voltage level -Vdc/2 Sa1' and Sa2' are turned ON. These states can be defined as 2, 1, and 0 respectively.

Table-1. Switching variables of three level inverter.

States mode	S_{a1}	S_{a2}	Sa1'	Sa2'	S_a
$+V_{dc/2}$	ON	ON	OFF	OFF	2
0	OFF	ON	ON	OFF	1
$-V_{dc/2}$	OFF	OFF	ON	ON	0

A five level NPC inverter consists of eight switching devices per phase and four clamping diodes. The DC supply consists of four capacitors in series and the

voltage is split into five levels ($+V_{dc/2}$, $+V_{dc/4}$, 0, $-V_{dc/4}$, $-V_{dc/2}$).

MODULATION STRATEGY

Carrier based SVPWM scheme

As shown in Figure-4(a), during one sampling interval, when the switching state becomes '0' from '1' for each phase at different time, an effective voltage will be applied to the load. Ts is the sampling time, T_{eff}, is the difference between two switching times T_{as} and T_{bs} is called the 'effective time'. If the value of T_{eff} is negative, then a negative voltage is applied to the load, i.e. T_{bs} is greater than T_{as}.

As the time must be positive, transition of the switching state must take place during a consecutive sampling interval. The effective time determines the inverter output voltage and so the theory of time can be extended to negative region as shown in Figure-4(b).

With the introduction of imaginary time value, the relation between time and voltage for the operation of one leg of inverter can be deduced as follows:

$T_{as} = \frac{Ts}{Vdc} V_{as}$, where V_{as} is the phase A voltage on the load side.

(a)

(b)

(c)
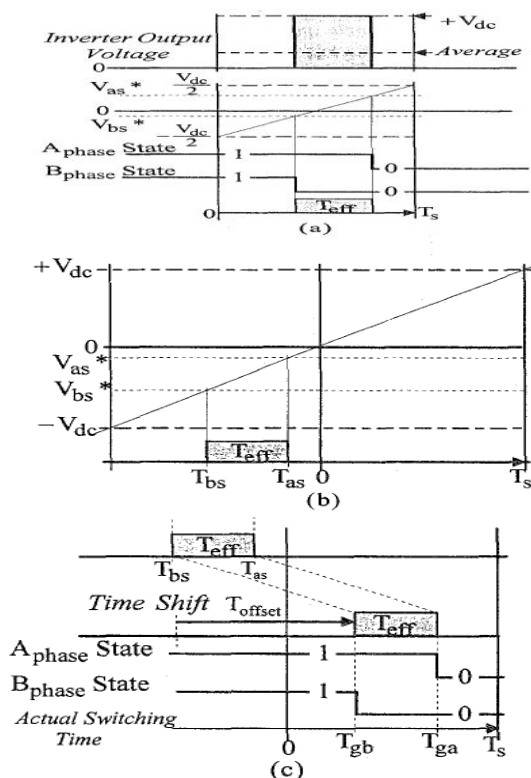
(a) Relationship between the effective time and the output voltage. (b) Extended concept for effective time. (c) Actual gating time generation.

Figure-4. PWM implementations.

The same principle can be applied for the remaining phases also. These times T_{as}, T_{bs} and T_{cs} are called 'imaginary switching times' and from these imaginary switching times, the effective time can be obtained as follows:

$$T_{eff} = T_{as} - T_{bs} = \frac{Ts}{Vdc}(V_{as} - V_{bs}) \qquad (3)$$

While generating the actual gating signals, we have one degree of freedom using which the effective time can be relocated anywhere within the sampling interval. In order to generate the actual gating pulses for each inverter leg, time shifting operation is applied to the imaginary switching times as follows:

$$\left. \begin{array}{l} T_{ga} = T_{as} + T_{offset}, \\ T_{gb} = T_{bs} + T_{offset} \\ T_{gc} = T_{cs} + T_{offset.} \end{array} \right\} . \qquad (4)$$

With this principle, inverter operation can be performed accurately using a simple equation and the same can be easily extended to 3 phase scheme also. The imaginary times are defined as follows:

$$T_{as} = \frac{Ts}{Vdc} V_{as}{}^{*}, T_{bs} = \frac{Ts}{Vdc}V_{bs}{}^{*} \text{ and } T_{cs} = \frac{Ts}{Vdc}V_{cs}{}^{*} \qquad (5)$$

In Space vector PWM method, the constant reference voltage vector v * can be represented by means of the two nearest active vectors as follows.

$$V^{*} = (T_1.V_n + T_{2.} V_{n+1}) / T_s \qquad (6)$$

The applying times T_1 and T_2 are not the actual gating times, but are the time durations in which active vectors are applied. These can be deduced as follows.

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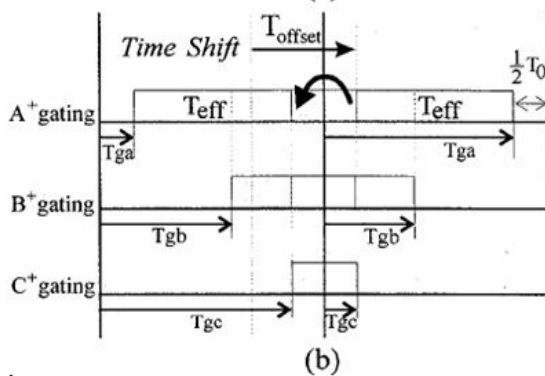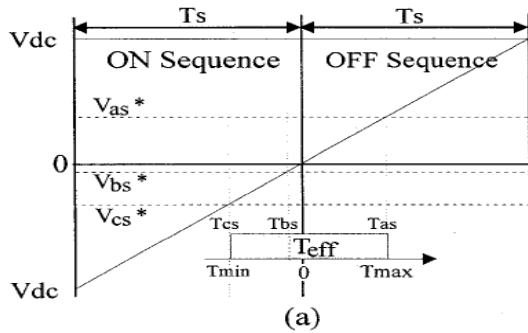
(a) Relationship between the effective time and the output voltage.(b) CBSVPWM gating generation.

Figure-5. PWM implementations by the proposed PWM method (in case of Sector 1)

$$T_1 = \frac{\sqrt{3}.Ts}{Vdc}\left[\frac{\sqrt{3}}{2}V_d^{s*} - \frac{1}{2}V_q^{s*}\right]$$
$$= \frac{Ts}{Vdc}\left[V_d^{s*} + (\frac{1}{2}V_q^{s*} - \frac{\sqrt{3}}{2}V_d^{s*})\right]$$
$$= T_{as} - T_{bs}$$

$$T_2 = \frac{\sqrt{3}.Ts}{Vdc}\left[V_q^{s*}\right] = T_{bs} - T_{cs} \qquad (7)$$

From the above, it is evident that the applying times T_1 and T_2 are nothing but the effective times. The zero time is to be symmetrically distributed in one sampling period as shown in Figure-5(b), such that the whole modulation task of SVPWM is completed. With the help of a sorting algorithm, T_{max} and T_{min} will relocate the effective time at the centre of the sampling period. Thus, the actual gating signals for inverter phase can be obtained using the time shifting operation as given below.

$$T_{ga} = T_{as} + T_{offset}, T_{gb} = T_{bs} + T_{offset}, \qquad (8)$$
$$T_{gc} = T_{cs} + T_{offset},$$

The time shifting value is

$$T_{offset} = \frac{1}{2}T_0 - T_{min} \text{ Where, } T_{eff} = T_{max} - T_{min}. \qquad (9)$$
$$T_{max} = max(T_{as}T_{bs}T_{cs}), T_{min} = min(T_{as}T_{bs}T_{cs}) \qquad (10)$$
$$T_0 = T_s - T_{eff}$$

Carrier based SVPWM scheme is adopted for 3 level and 5 level Neutral Point Clamped inverter based DVR and DSTATCOM for swell reduction. In this multilevel carrier based scheme, to generate 'm' level output voltage, (m-1) carrier signals are required. Therefore, in this work, the modulating wave is compared with two level shifted carrier signals for 3 level inverter and four carrier signals for 5 level inverter.
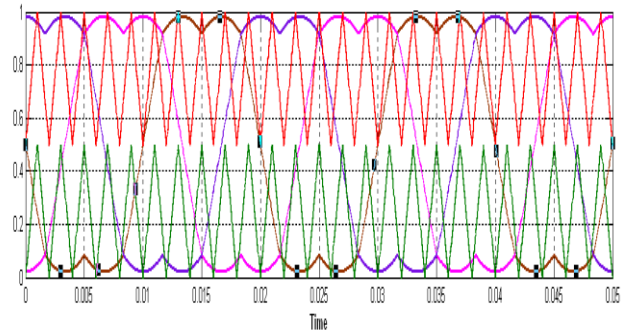

Figure-6. Level shifted multi carrier waves and Space Vector modulating wave for three level inverter.
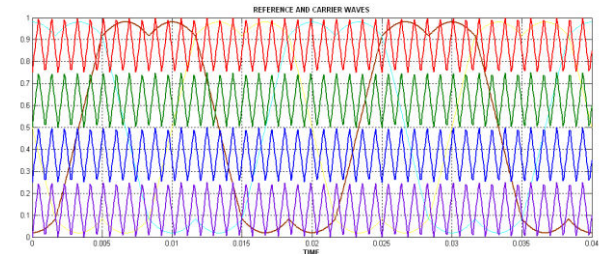

Figure-7. Level shifted multi carrier waves and Space Vector modulating wave for five level inverter.

SIMULATION RESULTS

Simulation results of unbalanced swell

In order to evaluate the performance of DVR and DSTATCOM for unbalanced and balanced compensation in voltage, initially, a voltage swell is deliberately created in two phases only. However, both DVR and DSTATCOM can handle balanced and unbalanced swells very effectively and the same is presented under heading of "simulation results for both balanced and unbalanced swells".

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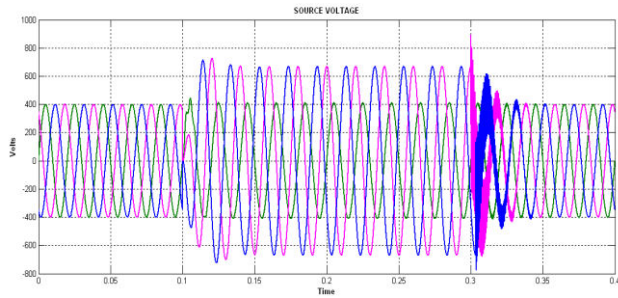
Simulation results of three level DVR
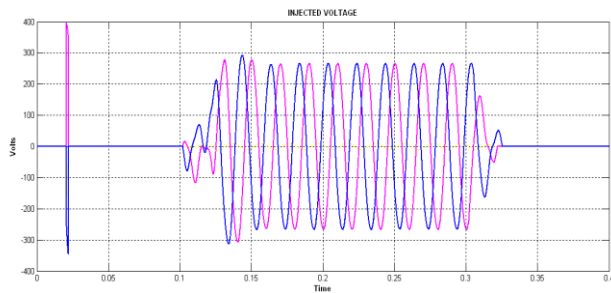

Figure-8. Source voltage.

Figure-9. Injected voltage.

Figure-8.Shows swell of 270V (i.e. a voltage of 670V during swell) in two phases and Figure-9 indicates the injection of 99.1% in phase opposition.

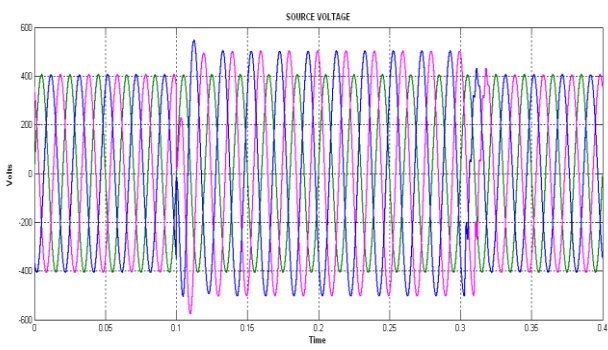## Simulation results of five level DVR
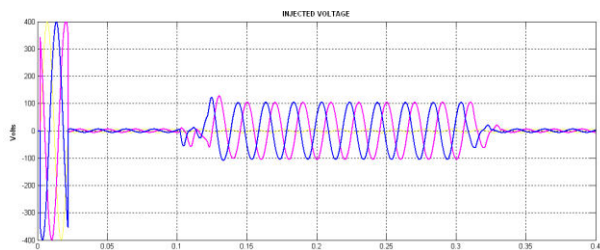

Figure-10. Source voltage.

Figure-11. Injected voltage.

Figure-10 shows swell of 100V in two phases (i.e. total voltage during swell is 500V) and Figure-11 indicates injection of almost 100% in the two phases.

Simulation results of three level DSTATCOM
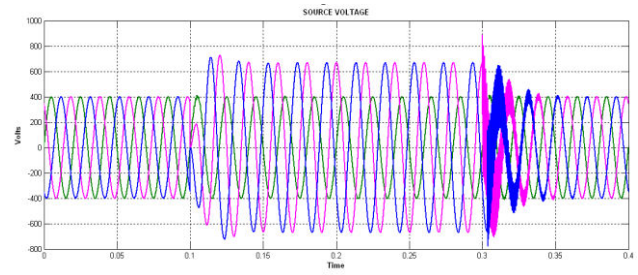
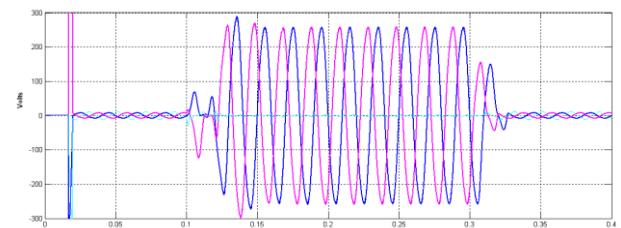**Figure-12.** Source voltage.

Figure-13. Injected voltage.

Figure-12.Shows swell of 270V in two phases and Figure-13 indicates voltage injection of 96.2%.
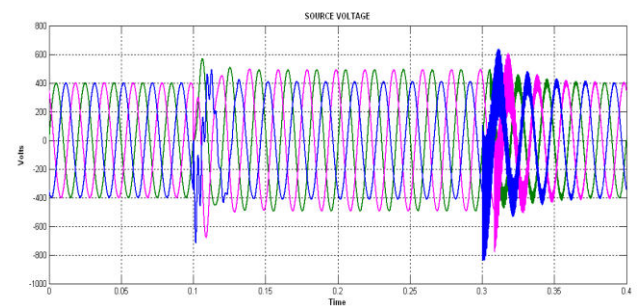
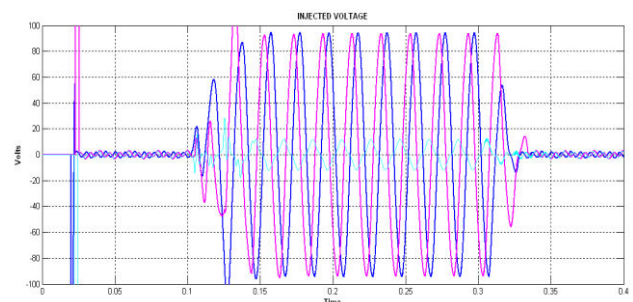## Simulation results of five level DSTATCOM

Figure-14. Source voltage.

Figure-15. Injected voltage.

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Figure-14 shows swell of 100V in two phases and Figure-15 indicates 97% of voltage injection in the two phases.

Simulation results for bothbalanced andunbalanced swells

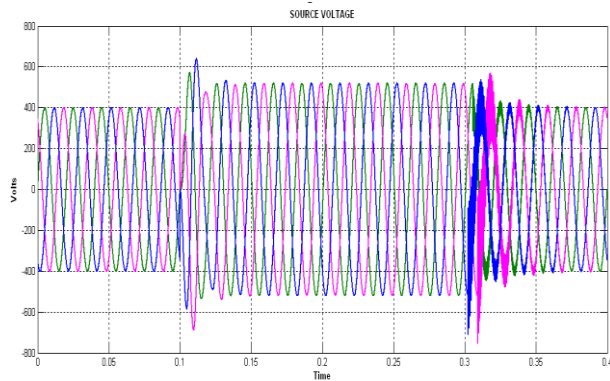**Simulation results of 3 level DVR**
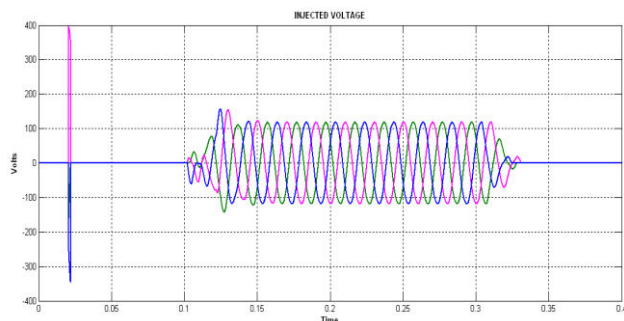

Figure-16. Source voltage.

Figure-17. Injected voltage.

Figure-16.Shows swell in three phases and Figure-17 indicates the injected voltage in all the three phases.
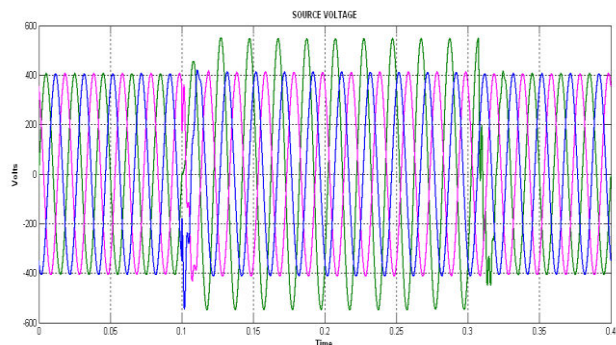
Simulation results of 5level DVR
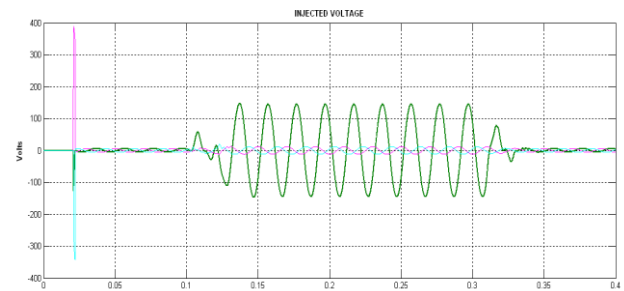

Figure-18. Source voltage.

Figure-19. Injected voltage.

Figure-18 shows swell in one phase and Figure-19 shows the injected voltage in one phase in opposition.
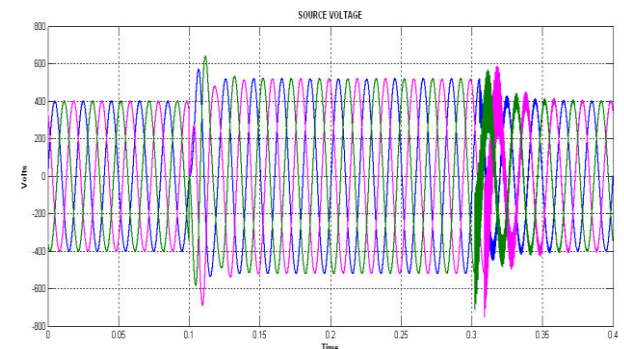
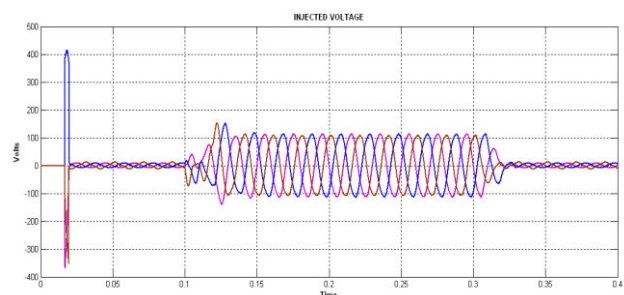**Simulation results of 3 level DSTATCOM**

Figure-20. Source voltage.

Figure-21. Injected voltage.

Figure-20 shows swell in all the three phases and Figure-21 indicates the injected voltage.

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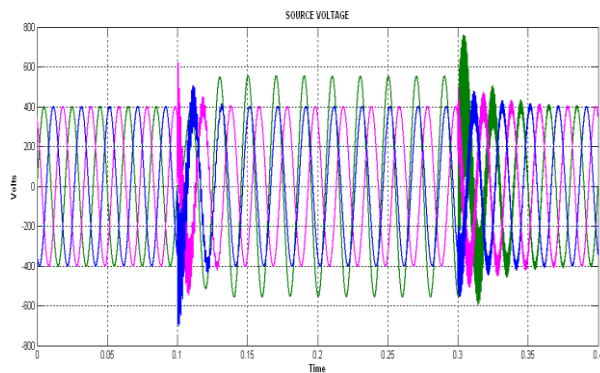
Simulation results of 5 level DSTATCOM
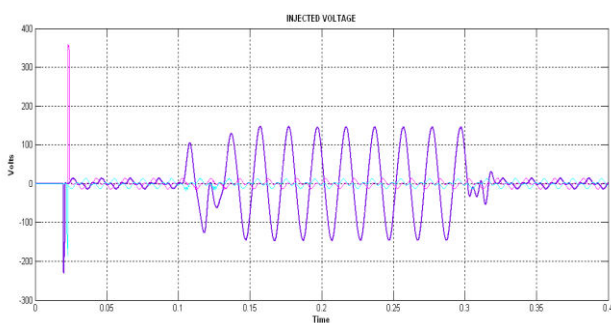

Figure-22. Source voltage.

Figure-23. Injected voltage.

Figure-22 shows swell in one phase and Figure-23 indicates the injected voltage in phase opposition.

The THD in the load voltage after compensation of swell is measured and tabulated below.

Table-2. Comparison of voltage injection and THD in the load voltage.

Inverter levels	DVR		DSTATCOM	
	%voltage injection	%THD	%voltage injection	%THD
3	99.1	2.52	96.2	4.29
5	100	1.48	97	2.93

CONCLUSIONS

The three level and five level inverter based DVR and DSTATCOM are simulated using carrier based SVPWM technique for compensation of swell. For the purpose of evaluation of the performance of both DVR and DSTATCOM for balanced and unbalanced voltage compensation, initially, voltage swell is created deliberately in two phases only. Later, simulations were carried out for both balanced (three phase swell) and unbalanced (swell in single phase) conditions also. From the simulation results, it is clear that DVR and DSTATCOM can compensate both balanced and unbalanced swells effectively. But, DVR is capable of regulating the voltage more effectively compared to DSTATCOM. It is also observed that the total harmonic distortion in the load voltage is less in case of DVR compared to DSTATCOM and also as the inverter output levels increase; the THD in the load voltage reduces. However, there is not much difference in the injected voltage of 3 level and 5 level inverters. The above technique can be extended for higher levels for further reduction in the THD content.

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