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THE ARCHITECTURE OF THE BROADBAND AMPLIFIERS WITHOUT CLASSICAL STAGES WITH A COMMON BASE AND A COMMON EMITTER

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ABSTRACT

This article considers a new design method of broadband amplifiers (BrA) for automation and control systems with higher voltage transfer ratio (Gain = 8÷58 dB). The feature of the proposed architectures of BrA lies in their implementation on the basis of emitter followers and current mirrors in the elemental basis of bipolar n-p-n transistors, for example, designated for the technological process SGB25VD and in the absence of classical stages with a common emitter or a common base. The results of computer simulations in the Cadence and Orcad environments are submitted.

Keywords: broadband amplifier, current mirror, emitter follower, transfer ratio.

INTRODUCTION

The use of CMOS transistors is a main vector of the development of integrated circuits for sensor systems and automatic devices. At equal geometry rules the operating band of bipolar transistor amplifiers, among which the complementary-symmetry circuits [1-2] occupy a special place, occurs higher than on the field-effect devices. There are other advantages of BJTs [3-4]. In addition, there are "niches" for the effective application of the circuits on active elements of BJT [5].

The use of conventional active loads in the analog integrated circuits with the technology SGB25VD [3] is limited by the capacities of CMOS transistors as p-n-p bipolar transistors are not realized in this technology. The concepts of inherent compensation and cancellation of impedances, suggested in [3], allow developing analog functional units (operational amplifiers, comparators, voltage regulators, etc.) without application of FETs and p-n-p bipolar transistors.

This article considers a new design method of broadband amplifiers (BrA) [3], based on the fundamental properties of current and voltage followers [6-8]. Their main difference lies in the absence of classic stages with a common emitter or a common base.

THE ARCHITECTURE OF THE BROADBAND AMPLIFIERS ON THE BASIS OF A DIFFERENTIAL EMITTER FOLLOWER

The architecture of BrA (Figure-1), suggested in [2], allows obtaining the output voltage at asymmetrical load starting which depends on the voltage ($u_{in.1}$) on the base of both transistors VT1 and VT2 of input emitter followers, i.e. realizing the functions of the differential amplifier $u_{in} = K_0(u_{in.1} - u_{in.2})$, where $K_0 >> 1$ - is the voltage gain of BrA.

In the static mode the emitter current values of transistors VT1 and VT2 are set by the current sources I_1 and I_2 and they are also due to the choice of resistance values of resistors R1 and R2.

If the voltage $u_{in.1}$ is applied to the input In.1 it causes an increase of current i_{R1} through the resistor R1:

$$i_{R1} = \frac{u_{in.1} + u_1}{R_1} \approx \frac{u_{in.1}(1 + K_0)}{R_1}, \quad (1)$$

where $K_0 = u_{out}/u_{in.1}$ - is the voltage gain of BrA.

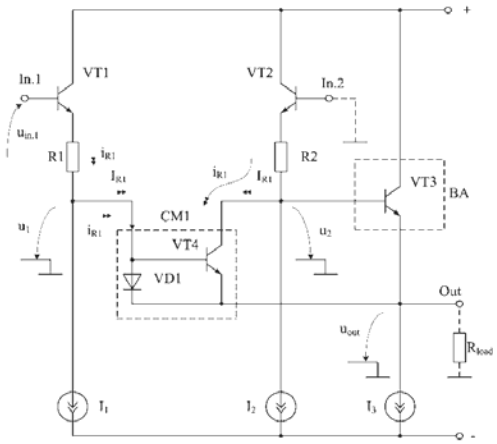


Figure-1. The architecture of BrA on the base of the emitter followers and the current mirror (CM1).

Meanwhile, the current increment i_{R1} is transmitted through the current mirror CM1 into the resistor R_2 and causes an increase of voltage on this resistor. Therefore, the voltage u_2 on the current source I_2, stabilizing the current flow, decreases. It leads to a decrease of the voltage on the output u_{out} of the broadband amplifier and on the current source I_1, this is due to the

fact that at the transfer ratio K_{BA}=1 of the buffer amplifier (on the transistor VT3) the following equation is satisfied:

$$u_{out} \approx u_2 \approx u_1 . \quad (2)$$

Thus, the voltage phase u_{out} on the output of the BrA is opposed to the input voltage phase u_{in} and the amplification factor is equal to:

$$Gain \approx \frac{\frac{R_2}{R_1} K_{i12.1}}{1-\frac{R_2}{R_1} K_{i12.1}}, \quad (3)$$

where $K_{i12.1}$≈1 – is the current transfer ratio of the current mirror (CM1).

If $R1$=$R2$, and the coefficient $K_{i12.1}$= 0.98÷0.99, then at high-resistance load (R_{load}=∞) the coefficient K_0 will be:

$$K_0 \approx \frac{1}{1-K_{i12.1}} >> 1 . \quad (4)$$

It means that the circuit of Figure-1 provides the amplification, which is bigger than one.

If the load resistance $R_{load} \neq \infty$, we'll have the following:

$$K_0 \approx \frac{\frac{R_2^*}{R_1} K_{i12.1}}{1-\frac{R_2^*}{R_1} K_{i12.1}} >> 1 , \quad (5)$$

where $R_2^* = R_2 \| \beta_3 R_{load} \leq R_2$ - is the equivalent resistance n the output circuit of the current mirror (CM1);

β_3 – is the current gain of the base of transistor VT3 of the output of emitter follower (BA).

In this case, to get the maximum value of $K_{0.max}$. it is necessary to choose R1 taking into consideration the following equation:

$$R_1 = K_{i12.1} R_2^* . \quad (6)$$

If the input voltage $u_{in.2}$ is applied through the second input of BrA (In.2), it induces the common-mode voltage change on the base of transistor VT3. The values of the output voltage u_{out} and the voltage u_1 also change. Consequently, the current flow through the resistor R1 decreases, this causes a decrease of the output current of the current mirror (CM1) and the current flow through the resistor R2. Therefore, in this mode the output voltage of BrA and the input voltage $u_{in.2}$ have the same phase.

The computer simulation of BrA, carried out on transistors of FSUE R and DE "Pulsar", shows that K_0 of the stage (Figure-1) can be more than 100 dB if it comprises an ideal current mirror ($K_{i12.1}$=1) and an ideal buffer amplifier. It is enough in most cases of the use in automatic devices. Thus, with the chosen parameters of elements ($R_1 = R_2 = 300$ Ohm, $I_1 = I_2 = 1$ mA, K_{BA}=1) the circuit of Figure-1 provides the amplification of the signal with $Gain \geq 80$ dB, if $K_{CM} = K_{i12.1} > 0.8$ Figure-2.

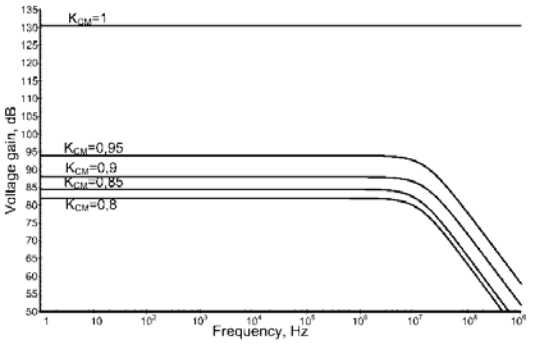


Figure-2. The dependence of the cut-off amplification factor of BrA (Figure-1) on the transfer ratio of current mirror $K_{i12.1}$=K_{CM} if K_{BA}=1.

In practical circuits of BrA with a standard current mirror the coefficient $K_0 \approx 10^3$ (60 dB). It is possible to get $K_0 = 10^4 \div 10^5$, if we design the current mirror (CM1) in a special way. For example, it can be similar to Vilson's scheme or it may have more sensitive buffer amplifiers providing K_{BA}≈1.

The limit values of $K_{0.max}$ when $K_{i12.1} = K_{CM} = 1$ are defined by the technological dispersion of emitter resistors (Figure-3).

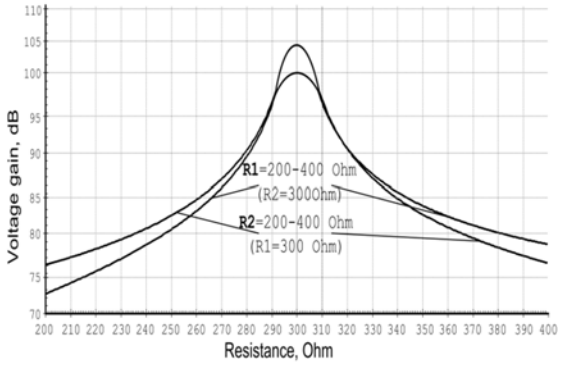


Figure-3. The influence of the dispersion of the resistors R1 and R2 on the cut-off amplification factor of BrA (Figure-1).

However, the numerical values of K_0 reach $K_0 > 70$ dB, if the relative error of resistors R1 and R2 is not higher than $\Delta R / R \le 30\%$.

Figure-4 shows the circuit of BrA (Figure-1) in the Cadence computer simulation carried out on SiGe prototypes of integrated transistors. Figure-5 illustrates the dependence of the voltage gain of BrA on the frequency.

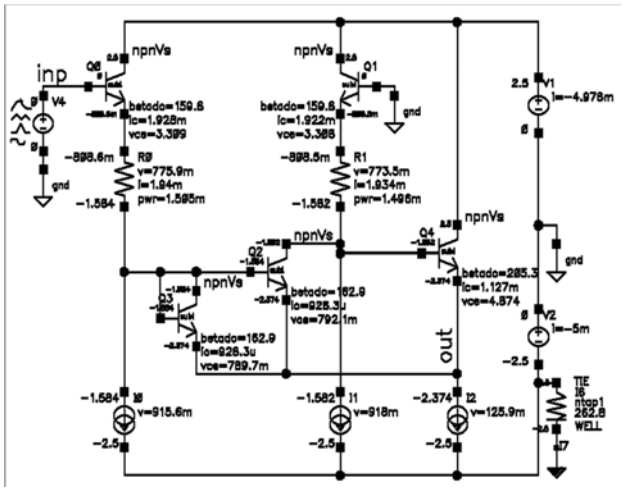


Figure-4. The circuit of BrA in the Cadence computer simulation.

According to the graphs, shown in (Figure-5), the voltage gain of BrA (Figure-4) reaches 12 dB.

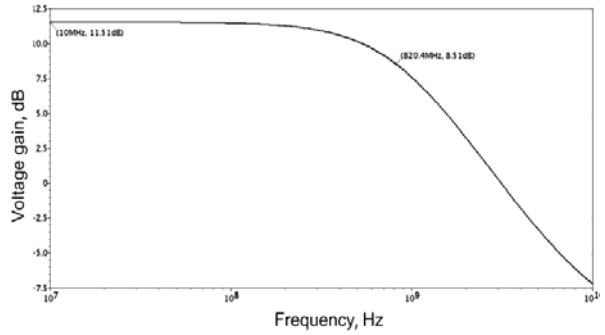


Figure-5. The dependence of the voltage gain of BrA (Figure-4) on the frequency.

THE DIFFERENTIAL STAGES BASED ON NPN SIGE TRANSISTORS

According to the architecture of Figure-1 the circuits of different differential stages are realized on the basis of n-p-n SiGe transistors (Figure-6) [3].

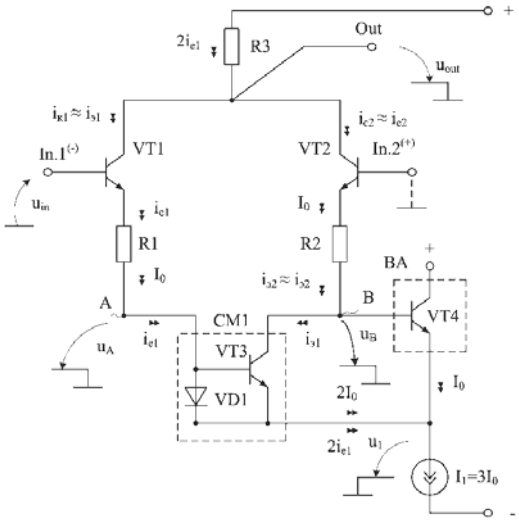


Figure-6. Differential stage designed on the basis of current and voltage followers [3].

If positive voltage increment u_{in} is applied to the input 1 of DS (Figure-6), it causes an increase of emitter and collector currents of the transistor VT1:

$$i_{e1} \approx \frac{u_{in} - u_A}{R_1 + r_{e1}} \approx \frac{u_{in}(1+K_0)}{R_1} \approx i_{c1}, \quad (7)$$

where $r_{e1} << R_1$ - are resistances of emitter junction of the transistor VT1;

$R_1 = R_2$ - are resistance values of R1 and R2;

$K_0 >> 1$ - is a voltage transfer ratio from input 1 into the circuit of emitter of the transistor VT4 (3).

The numerical values of K_0 (3) are defined by the difference between resistances of R1 and R2. They also depend on the rate of accuracy of the current mirror (CM1) and the buffer amplifier (BA) which is defined by the difference of their transfer ratios from one ($K_{i2.1}$, K_{BA}).

The increment i_{e1} comes to the input of the current mirror (CM1), the output current of which is $i_{out} \approx i_{e1}$. Then the increment i_{e1} goes to the resistor R2, emitter and collector of the transistor VT2:

$$i_{e2} \approx i_{e1} = (1+K_0)\frac{u_{in}}{R_1} = i_{c2}. \quad (8)$$

That is why the alternating current i_{R3} will flow through the resistor R3 and it will generate the output voltage u_{out}:

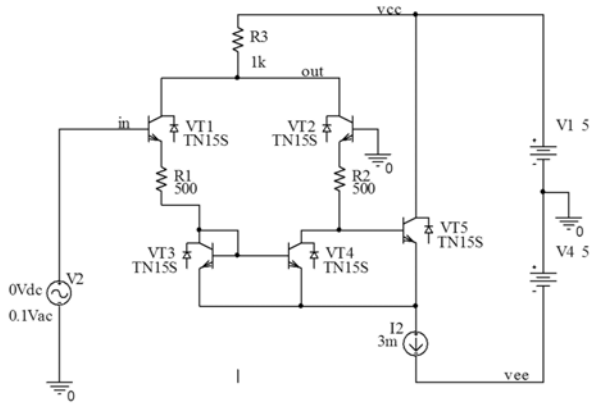
$$i_{R3} \approx 2i_{e1} = 2(1+K_0)\frac{u_{in}}{R_1}, \quad (9)$$

$$u_{out} = \frac{2(1+K_0)}{R_1} R_3 . \quad (10)$$

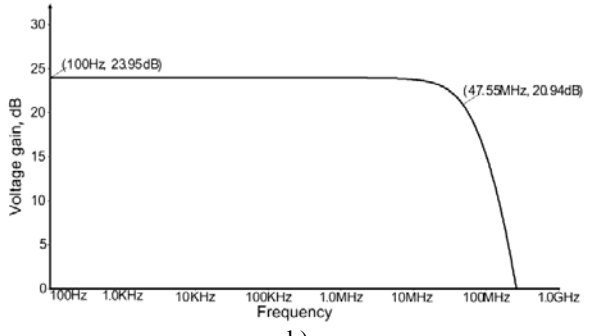
Consequently, the voltage gain of DS (Figure-6) will be:

$$Gain \approx 2(1+K_0)\frac{R_3}{R_1} >> \frac{R_3}{R_1+R_2} . \quad (11)$$

For practical circuits $K_0 = 50 \div 100$, this increases the amplification factor considerably. These conclusions are proved by the results of computer simulation of the circuits (Figure-7) on the prototypes of the transistors produced by FSUE R and DE "Pulsar".



a)



b)

Figure-7. The circuit of DS (Figure-6) in the PSpice environment of computer simulation (a) and frequency dependence of its voltage gain (b).

SIGE OPERATIONAL AMPLIFIERS

The operational amplifiers (OA) are realized on the basis of differential stages of Figure-6 which allow introducing common negative feedback on direct current (Figure-8).

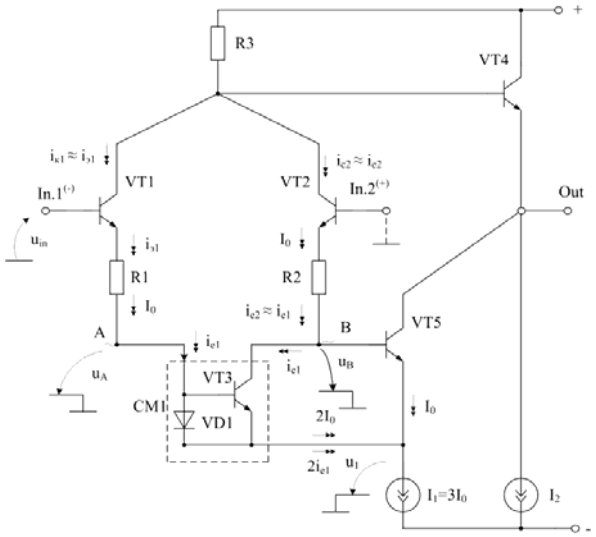
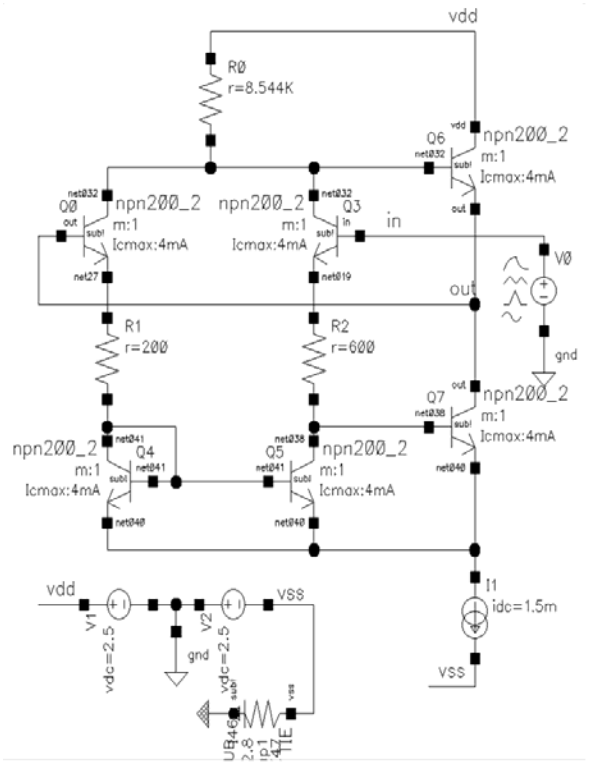
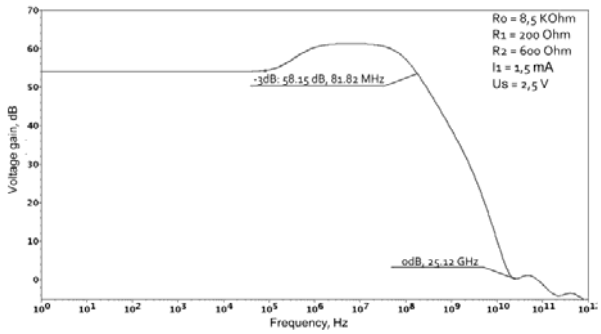


Figure-8. The circuit of the operational amplifier based on the current mirror (CM1) and emitter followers.

Figure-9 shows the circuit of OA (Figure-8) in the Cadence computer simulation on SiGe integrated transistors SG25H1 and frequency dependence of its voltage gain.



a)



b)

Figure-9. The circuit of OA in the Cadence computer simulation on SiGe integrated transistors (a) and frequency dependence of its voltage gain (b).

The analysis of the graphs of Figure-9 shows that, at constant current the voltage gain of the operational amplifier is in the range of 50-60 dB.

CONCLUSIONS

The considered architectures of amplifiers extend the idea, existing among engineers, about design methods of analog integrated circuits, realized on SGB25VD, SG25H1 technologies without p-n-p transistors.

The limit values of amplification factors of differential stages of the considered category are defined by the difference between resistances of emitter resistors R1 and R2 which must not have dispersion more than 30%; by their absolute value and also by the correction of the current ratio of current mirror CM1 from unity, by the input resistance of buffer amplifier and its voltage transfer ratio (K_{BA}).

The most effective field of application of the considered broadband amplifiers, differential stages and operational amplifiers made on their basis is low voltage technological processes, where p-n-p transistors are not realized or they are very ineffective.

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