VOL. 10, NO. 18, OCTOBER 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

A 2.4 GHZ LOW NOISE AMPLIFIER USING FORWARD BODY BIAS TECHNIQUE FOR WIRELESS SENSOR NETWORK APPLICATIONS

Anishaziela Azizan, Sohiful Anuar Zainol Murad, Mohd Nazrin, Md Isa and Rizalafande Che Ismail
School of Microelectronic Engineering, University Malaysia Perlis, Kangar, Perlis, Malaysia
E-Mail: syaziela_88@yahoo.com.my

ABSTRACT

This work presents a 2.4 GHz low noise amplifier (LNA) for wireless sensor network in CMOS 0.13-µm Silterra process. The forward body bias technique with cascode configuration has been adopted in order to implement a suitable LNA for low power consumption target. The supply voltage was varied from 0.4 V to 0.6 V as to optimize the tradeoffs for LNA performances. The simulation results show that the power consumption of 0.2 mW is achieved. However, the best performance of the proposed LNA is obtained at supply voltage of 0.5 V due to the tradeoffs between power consumption, s-parameters, noise figure (NF) and linearity. A gain of 12.03 dB, NF of 4.95 dB and input third order intercept point (IIP3) of -7.5 dBm at 2.4 GHz is obtained. The input return loss (S11) and the output return loss (S22) is below than -10 dB with the calculated figure of merit (FOM) is 6.46 (1/mW).

Keywords: low noise amplifier, forward body bias, low power consumption, tradeoffs, performances, figure-of-merit (FOM).

INTRODUCTION

A wireless sensor network (WSN) develops rapidly nowadays due to the demand of its functions in the recent markets. WSN consists a group of low cost, low power, multifunction and also, small in size of wireless nodes, which works together to collect, process the data and communicate wirelessly. WSN is used in many applications such as remote sensing, monitoring healthcare, security system, home automation and traffic control. While in agriculture, WSN is used to monitor environmental parameters such as temperature, carbon dioxide (CO_2) concentration, and humidity, intensity of radiation and wind pressure or speed. The basic specifications of WSN are the reliability, accuracy, flexibility, expenses, the difficulty of development and power consumptions [1]. But due to the battery powered, power consumption is become as one of the most important specification.

For intelligent farming, in order to enhance the efficiency and growth in crop yield while improving the cultivation by collecting different data, WSN can be applied. Information and data on weather condition, soil environment, monitoring, soil humidity and pH level can greatly help in improving the yield of the crop in order to keep up the soil fertility. However, WSN are still rarely applied in farming nowadays. This paper will focus on studying, analyzing and implementing the technique in the circuit architecture of LNA as it is a first block of the receiver as shown in Figure-1 [2]. The main objective of the LNA design is to consume less power with suitable output performances.

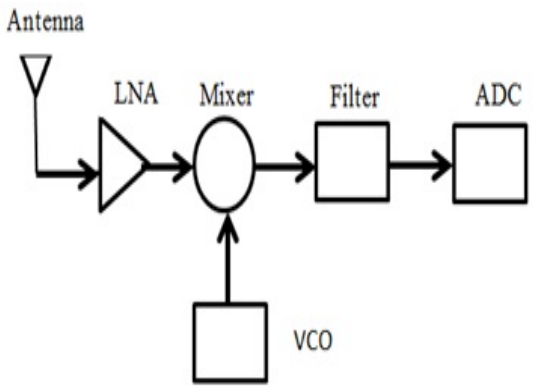

Figure-1. WSN receiver block diagram.

LNA circuit design

Figure-2 shows a schematic design of the proposed LNA. The design is based on forward body bias technique. As to increase the gain and obtain good linearity, the circuit is integrated with a cascode structure which consists of two NMOS transistors. The main element of this LNA is the transistor M_1 and M_2. Notice that the NMOS transistors have four ports, that is, gate (G), drain (D), source (S), and body (B). The source of M_1 is connected to ground, forming that the transistor M_1 is in a common-source configuration. The gate of M_1 is the input port of signals while the drain of M_2 is the output port of signals. For low power consumption, the body is connected to a positive voltage source which could reduce the threshold voltage (V_{TH}) of NMOS transistors.

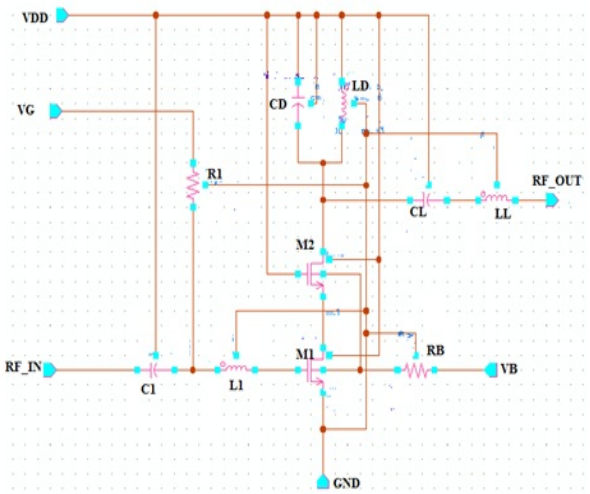

Figure-2. Schematic of the proposed LNA.

In this design, the V_B is set to 0.3 V which is much less than 0.7 V, that is, the turn-on voltage of PN junctions. Therefore, the body-source junction of the NMOS transistor in this LNA has a negligible leakage current. In the circuit as shown in Figure-2, the R_1 denotes the biasing resistance at the gate of transistor M_1. The inductance L_D connected to the drain of transistor M_2 can increase the gain of this LNA. The C_1 and C_L are the coupling capacitors.

The function of C_1 and L_1 is for input matching of 50 Ω and the value is also tuned in order to ensure the circuit operates at 2.4 GHz. The size of the transistor will determine how low the current as to get lowest power consumption and also to increase the gain and efficiency.

The series LC circuit of C_L and L_L are as a part of the output matching. Both value is tuned to get the desired output matching at center frequency of 2.4 GHz. R_2 and R_B are added into the design because both resistors could increase the gain while reducing the noise figure of the output.

SIMULATION RESULTS

LNA circuit design in Figure-2 was simulated using Cadence Spectre. Figure-3 shows the plot of s-parameter for S11, S22 and S21. As depicted in the graph, it can be seen that the performance of S21 is 12.03 dB. Besides, the propose LNA achieves to get S11 of -14.27 dB and S22 of -12.41 dB. It shows that the circuit has a good input and output matching. Figure-4 illustrates the noise figure of the LNA. From the simulated result, it indicates that the lowest NF could be achieved is 4.95 dB, which is between the desire output specifications.

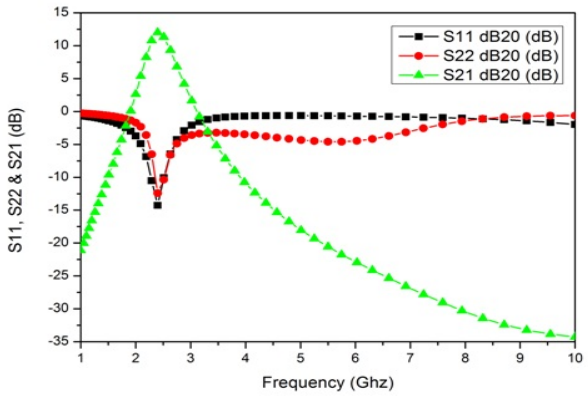

Figure-3. S-Parameters of the proposed LNA.

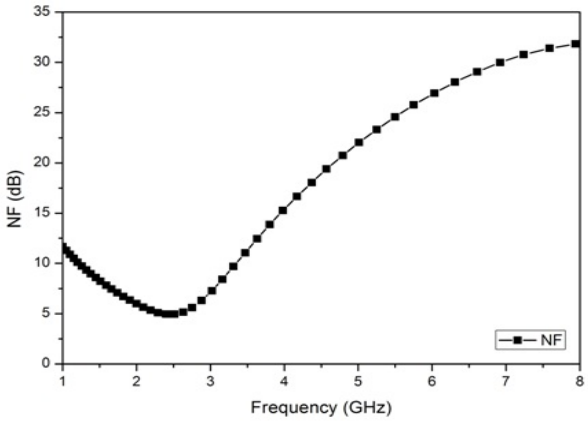

Figure-4. Noise figure.

The plot of the stability factor is shown in Figure-5. The LNA is unconditionally stable, which the stability for the propose LNA as the value is greater than 1. In terms of linearity, the circuit is able to fulfill the requirements which the input third order intercept point (IIP3) is -7.5 dBm as can be seen in Figure-6.

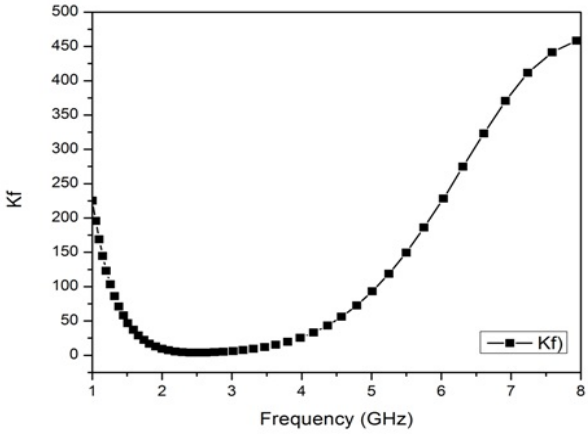

Figure-5. Stability.

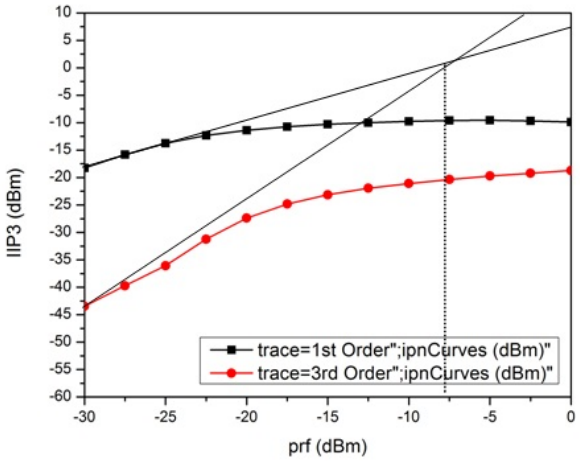

Figure-6. IIP3 of the proposed LNA.

Results summary

From the simulated results, the performances obtained from this propose LNA designed is comparable with other published work recently. The chosen published works are a combination of different technology and LNA topologies. As can be seen from Table-1, it can be concluded that the forward body bias technique with cascade architecture could achieve a better LNA performance. This work obtained highest figure of merit (FOM) and also lower power consumption compare with previous work. The FOM is being considered as it depicts the tradeoffs between power consumption, noise figure and gain of the LNA circuit. Therefore, the comparison is made based on the calculated FOM obtained. It can be seen that, from this new schematic of LNA, the performance of the LNA in improved compared to the others work.

Table-1. Performances comparison of recently published LNA.

References	[3]	[4]	[5]	[6]	[7]	This Work
CMOS Technology (µm)	0.18	0.18	0.18	0.13	0.13	0.13
Supply Voltage (V)	0.6	0.6	1.8	1.2	0.8	0.5
Frequency (GHz)	3.1-0.6	2.4	1.5	0.1-2	3.66	2.4
NF (dB)	3.7-5.5	2.88	3.62	1.6-1.8	2	4.95
Gain (dB)	14.6	10.1	22	21.7-23.8	14	12.03
IIP3 (dBm)	-13.19	N/A	N/A	-9.92	10.5	-7.50
Power (mW)	3.1	0.84	19.6	5.3	2.45	0.3
FOM (1/mW)	0.68	4.05	0.49	5.15	3.53	6.26

CONCLUSIONS

This paper focused on designing a new topology of LNA that would result in low power consumption with specific circuit performance. In this work, a low supply voltage of 0.5 V was used in order to get lowest power consumption. By using forward body bias technique with cascode configuration, the FOM of 6.26 (1/mW) is achieved with power consumption of 0.3 mW. The simulation results validate peak performance at 2.4 GHz that suitable for wireless sensor network applications.

ACKNOWLEDGEMENT

The authors would like to express their appreciation to the support and contributions from those who assist in this research especially FRGS grant (9003-00387) that enabled the production of this article.

REFERENCES

[1] Anishaziela Azizan, S.A.Z. Murad and R.C. Ismail. 2014. A Review of LNA Topologies for Wireless Applications, 2nd International Conference on Elecronic Design 2014 (ICED 2014), 19-21 August, Penang, Malaysia.

[2] Murad S.A.Z., Ismail R.C., Isa M.N.M., Ahamd M.F. and Han W.B. 2013. High gain 2.4 GHz CMOS low noise amplifier for Wireless Sensor Network Applications 5th IEEE International RF and Microwave Conference (RFM 2013); pp. 39-41, 9-11 Dec, Penang; Malaysia.

[3] A. Dehqan, E. Kargaran, K. Mafinezhad and H. Nabovati. 2012. An ultra low voltage ultra low power CMOS UWB LNA using forward body biasing, IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Vol. 1, pp. 266-269.

[4] J. Wu, Y. Lin and Y. Tsai. 2012. A sub-mW CMOS LNA for WSN applications, Asia-Pacific Microwave Conference Proceedings (APMC), pp. 899-901.

[5] H. B. Kia, A. K. A'ain, I. Grout and I. Kamisian. 2013. A Reconfigurable Low-Noise Amplifier Using a Tunable Active Inductor for Multistandard Receivers, Circuits, Systems, and Signal Processing, Vol. 32, No. 3, pp. 979-992.

[6] I. Bastos, F. Querido, D. Amoêdo, and L. B. Oliveira. 2013. A 1. 2 V Low-Noise-Amplifier with Double Feedback for High Gain and Low Noise Figure, IFIP

Advances in Information and Communication Technology, Vol. 394, pp. 573-581.

[7] H. Rastegar and A. Hakimi. 2013. A High linearity CMOS low noise amplifier for 3.66 GHz applications using current-reused topology, Microelectronics Journal, Vol. 44, pp. 301–306.