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RF ENERGY HARVESTING WITH EFFICIENT MATCHING TECHNIQUE FOR LOW POWER LEVEL APPLICATION

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ABSTRACT

Development of energy harvesting and wireless power transfer have emerged batteryless and non-contact energy transfer. For optimum power transfer between antenna and the rectifier circuit, impedance of the antenna and rectifier should be match. This paper describes the design and implementation of the 7-stage multiplier in energy harvesting. A Modified dickson configuration is chosen, consists of two HSMS 2850 Schottky diodes and two capacitors for each stage. The aim of this paper is to analyze the performance of the designed rectifier together with matching network. Simulation results show an improvement for the multiplier circuit with a matching network compare to the multiplier alone. Maximum of 60% improvement in rectified output has been achieved at low input power.

Keywords: energy harvesting, wireless power transfer, dickson multiplier, matching network.

INTRODUCTION

Radio Frequency (RF) energy harvesting technology is not new, it has been studied years before by many researchers (Sogorb *et al.* 2008; Muramatsu & Koizumi, 2010; Jabbar *et al.* 2010; Kim, 2011; Matiko *et al.* 2014). Due to unpredictability of source like wind, light, vibration, piezoelectric and other sources, RF became a more popular source in harvesting energy for its availability and easy scavenging system. RF energy can be harvested either from ambient or from dedicated source. A device designed to collect the electromagnetic energy in the free space and transform into direct current (DC) is called rectenna. Typical RF energy harvester or rectenna is shown in Figure-1 where it is basically a combination of rectifier and antenna.
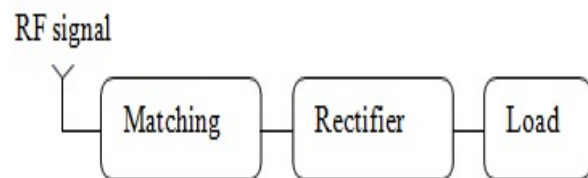
Figure-1. General block diagram of rectenna.

As depicted in Figure-1, a matching network is applied between the antenna and the rectifier circuit. The existence of matching circuit is crucial as it can improve the RF to DC efficiency of the rectenna. A good matching network will allow a maximum power transfer between the antenna and the rectifier circuit.

Availability of RF energy in the surrounding or areas close to transmission towers provides an an opportunity to harvest the unused energy, particularly in GSM and WLAN band. Despite this band, exploring the possibility in harvesting an energy form RF broadcasting wave is riveting research (Sogorb *et al.* 2008; Mikeka *et al.* 2011; Keyrouz *et al.*2012).

Harvesting RF ambient power from Digital Television (DTV) signals was first investigated by Intel where 60uW of energy was harvested at a distance of 4 km from the broadcasting TV station (Keyrouz *et al.* 2012). RF energy harvesting in the Digital TV (DTV) band is presented in (Mikeka *et al.* 2011), where the rectifying antenna, given a single tone excitation at 550 MHz, has a measured conversion efficiency of 0.4% for -40 dBm input and 18.2% for -20 dBm input, respectively. Power of +3 dBm and -44 dBm are measured from Tokyo tower TV broadcasting at 400 m and 4 km correspondingly.

In this paper, the possibility of harvesting energy from commercial RF broadcasting stations is investigated. Matching technique has been focus in this research as an alternative in increasing the efficiency. The designed circuit is targeted to harvesting energy from ultra-high frequency (UHF) channel 29 with centre frequency of 540 MHz. The designed multiplier in this paper is successfully covered the channel bandwidth from 535.5 MHz to 541.5 MHz.

DESIGN

Rectifier design

The rectifier presented is this paper is based on 7-stage Dickson multiplier with Schottky diode as stated in Figure-2. Each stage is consisting of two diodes and two capacitors. Typically, output from a single stage rectifier is very low since the captured energy is low, thus by cascading the circuit, a higher DC voltage can be obtained from an AC input. The cascaded circuit is called Dickson multiplier

This circuit is a Dickson multiplier that has been previously modified by Karthaus and Fischer in 2003, where it has fewer requirements than original Dickson topology. The circuit do not need of clock pulses to operate, so did the numbers of coupling and stray capacitors were reduced.

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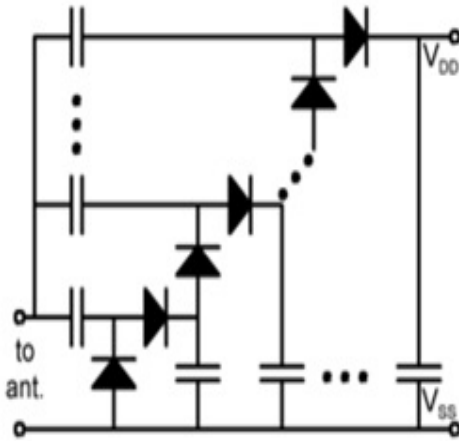
Figure-2. Dickson n-stage rectifier configuration
(Karthaus & Fischer, 2003).

The rectify elements in the circuit mainly determines the RF to DC conversion efficiency and Schottky diodes appeared to be a good candidate as they widely used (Zhang *et al.* 2013; Keyrouz *et al.* 2012; Jabbar *et al.* 2010; Devi *et al.* 2011). Due to high operating frequency and low input power, diodes should have a very fast switching time and the lowest possible turn on voltage (Merz. *et al.* 2014). Schottky diodes offer great advantages in terms of speed because it does not rely on holes or electrons recombining when they enter the opposite type of region as in the case of a conventional diode. Moreover, the diode has a much higher current density than an ordinary PN junction, means that low forward voltage drop, thus less energy is wasted as heat, making them the most efficient choice for applications sensitive to efficiency. Hence, HSMS2850 Schottky diodes were selected in this circuit as they have low turn on voltage and have been designed and optimized for use in small signal (for input power less than -20 dBm) applications at frequencies below 1.5 GHz (Avago Tech.). While, 4.7 nF capacitor is used in each stage capacitor.

The circuit has been simulated based on a low cost FR-*4* board (with dielectric constant, $\epsilon_r = 4.6$, and substrate thickness, $t = 1.6$ mm). The circuit dimension is 90 mm x 78 mm. All the design and results are simulated in Advanced Design System (ADS) software.

Matching network

To increase the conversion efficiency, the designed circuit should resonate at the targeted frequency. A matching circuit is designed to match the impedance of the multiplier circuit to the standard 50 Ω antenna in order to allow maximum power transfer from the antenna to the circuit.
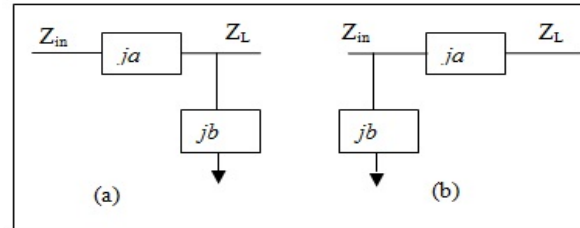

Figure-3. L matching configuration (a) Z_{in} less than Z_L
(b) Z_{in} greater than Z_L.

To keep the losses in the circuit as minimum as possible, L matching network is applied as it has only two lumped elements in the matching circuit as shown in Figure x. Configuration in Figure-3 (a) is for input impedance (Z_{in}) lower than load impedance (Z_L) and Figure-3 (b) is for Z_{in} greater than Z_L. Element *ja* and *jb* in the circuit are reactive component, can be either inductor or capacitor. For a single frequency, any positive-real complex impedance can be matched to any other positive-real complex impedance using no more than two reactive component (Rhea R., 2006).
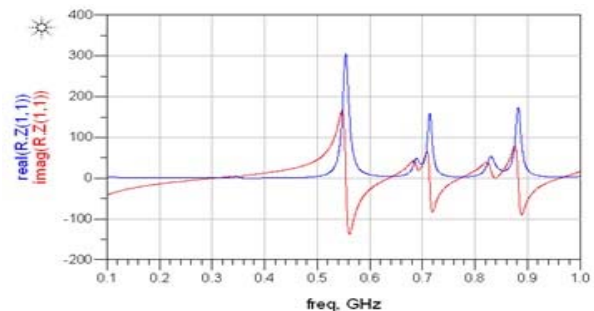
Figure-4. Impedance of the multiplier at 540 MHz.

In the designed multiplier circuit, the input impedance at 540 MHz is equal to 57.7 + j 132.9 Ω, which is complex impedance and greater than 50 Ω. Thus, configuration in Figure-3 (a) is chosen. To simplify the calculation, the circuit needs to be transform to a resistive load only. So, the siries load impedance is converted to parallel, where it new value is 364 Ω for R_{Lp} and $+j158$ Ω for X_{Lp} and negative reactance, X_c is added parallel with X_{Lp} to eliminate the positive reactance as can be seen in Figure-5.
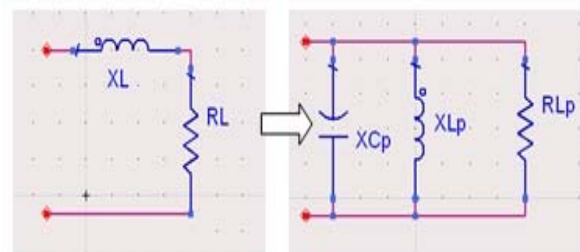

Figure-5. (a) Impdedance equivalent circuit, (b) parallel
impedance transformation.

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$$a = R_{in}\left(\sqrt{\frac{R_{Lp}}{R_{in}}-1}\right) \tag{1}$$

$$b = R_{Lp}\left(\sqrt{\frac{R_{Lp}}{R_{in}}-1}\right)^{-1} \tag{2}$$

By applying both formula (1) and (2), the reactance of a and b is calculated as 125 Ω and 145 Ω. Then, the value of L and C is determined as 36.9 nH and 4 pF, taking into account the value of XCp. The reflection coefficient is found at 540 MHz with -38.8 dB deep exhibit bandwidth of 106 MHz. It is clear from the Figure 6 that the calculated matching element will match the impedance of multiplier and the 50 Ω antenna.
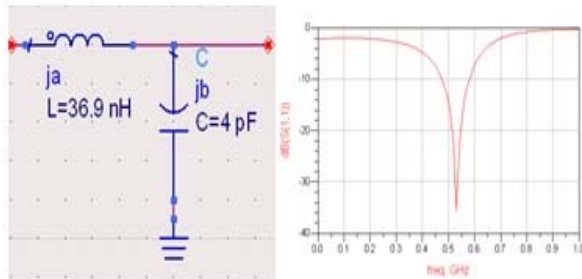
Figure-6. Proposed matching network (a) matching circuit, and (b) reflection coefficient of the matching circuit.

RESULTS AND DISCUSSION

All the results discuss here are simulated by using Advanced Design System 2013 (ADS). The rectified output voltage is simulated across 100 pF parallel with 100 kΩ loads. As can be seen in Figure-7, a good match is achieved when the matching network is combined to the multiplier circuit, where 9 MHz bandwidth was obtained with -36.6 dB deep at 539 MHz.
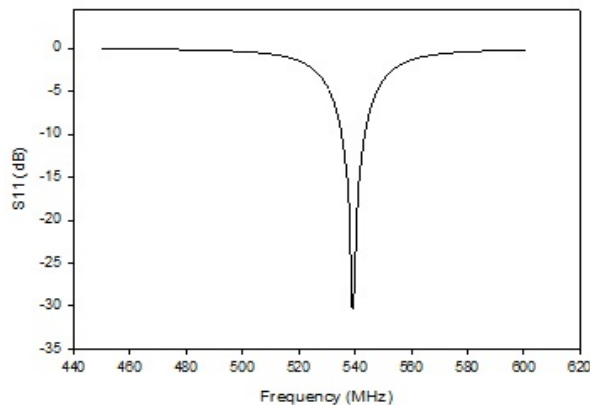
Figure-7. Reflection coefficient of the multiplier with the matching network.

The rectified output voltage of the circuit is then measured to verify the circuit performance without and with matching network. At the resonant frequency, which is 540 MHz, the result showed that there are improvements in the rectified output for an input power from -30 dBm to +5 dBm after the matching network is applied ahead of the circuit. 6.7 V is achieved at 0 dBm input power for circuit with matching, while 4.9 V for circuit without matching.
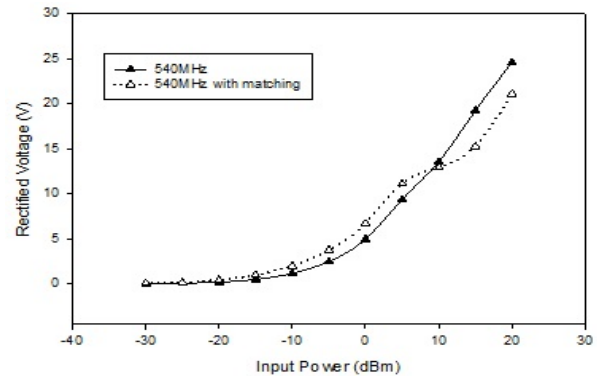
Figure-8. Rectified output voltage of the multiplier circuit at 540 MHz.

Data in Table-1 illustrated the rectified output voltage at 535 MHz and 545 MHz for multiplier with and without matching network. The ouput voltage follow the same trend as where it gives higher rectified voltage when the matching network is applied for low input power as compare to circuit without matching. Based on these results, it can be concluded that the circuit with matching network is optimized for lower input power.

Table-1. Simulated results with and without matching network for the proposed multiplier.

Pin (dBm)	535 MHz (Volt)		545 MHz (Volt)	
	No Match	Match	No Match	Match
-30	0.021	0.051	0.025	0.049
-25	0.062	0.144	0.073	0.147
-20	0.174	0.36	0.202	0.405
-15	0.452	0.82	0.52	0.99
-10	1.075	1.67	1.222	2.139
-5	2.31	3.15	2.619	4.196
0	4.68	5.69	5.208	7.686
5	8.89	9.98	9.84	11.59
10	13.46	12.78	13.62	12.36
15	19.19	15.34	19.36	15.33
20	24.54	21.20	24.83	21.07

CONCLUSIONS

A matching using L-network has been discussed in order to boost the efficiency of the multiplier circuit at low power level. Theoretical approach to obtain value of the inductance and capacitance for certain impedance has been presented. Simulation further verified that the

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multiplier circuit produces more rectified output voltage at low input power when the matching network is applied to the circuit.

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