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A 2.4 GHZ TWO STAGE CMOS CLASS-F POWER AMPLIFIER FOR WIRELESS APPLICATIONS

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ABSTRACT

The design of a 2.4-GHz CMOS class-F power amplifier (PA) for wireless applications is presented in this paper. The class- F PA design is implemented using 0.13-µm CMOS process. It utilizes two stages cascade topology and the transistors are arranged in parallel to reduce the transistor's on resistance which correspondingly increase the PA efficiency. The simulation results show that the PA delivers 12 dBm output power and 60% power added efficiency (PAE) into a 50 Ω load. The supply voltage is 1.3 V and the chip layout is 0.66 mm².

Keywords: class F, power amplifier, cascade, output power, power added efficiency.

INTRODUCTION

Recently, a modulation scheme for modern wireless systems such as 4G long term evaluation (LTE) and mobile worldwide interoperability for microwave access (MiMAX) utilize orthogonal frequency division multiplexing (OFDM) which has a high peak-to-average power ratio (PAPR) resulting in degradation of efficiency in transmitters [1]. Therefore, the high efficiency, low cost, compact and high integration power amplifier (PA) becoming an important issuein designing a circuit with relatively high power efficiency.

Over past years, the PA technology has emerged rapidly and has become highly integrated. The circuit design has involved several process technologies such as CMOS, GaN, GaAs and SiGe BiCMOS [2-5]. However, CMOS has become a good technology due to their high integration and low cost. Nevertheless, the main challenge in design PA using CMOS technology is the low breakdown voltage at deep sub-micron and thus limits the maximum drain to gate voltage. Normally, the supply voltage is two times lower than the drain voltage. Thus, the transistor has to work at a low supply results lower power and low efficient.

Generally, PAs are a last part in the transmitter front-end of RF transceivers. The role of a PA is to amplify a signal to a certain level of power which will ensure that the receiver will receive a transmitted signal across some distance. PA can be defined as an electronic amplifier used to convert a low signal power into a large signal power of radio frequency (RF) especially in order to drive the antenna in a transmitter [6]. Good gain, high efficiency, good input and output return loss, high linearity (P1dB) and low heat dissipation is a demanding PA.

This paper describes a two stage class-F PA at 2.4 GHz designed using 0.13-µm CMOS process. The proposed design consists of driver stage, amplifier stage and harmonics filtering to increase power efficiency of PA. The transistor's on resistance is decreased by arranging the transistors in parallel for high efficiency.

Circuit implementation

Figure-1 shows the complete schematic of the proposed class-F PA. The proposed PA consists of three stages which are the pre-amplifier stage, amplifier stage and output stage. The class-F PA uses multiple stages for sufficient power gain and efficiency. The first stage is known as pre amplifier stage is designed to provide sufficient input signal to the second stage for high efficiency. Therefore, pre amplifier is essential to be added at the input of the second stage to produce a very high half sinusoidal voltage swing. The second stage is known as amplifier stage which able to operate in the active region. It is also consider as the most power efficient when applied high overdrive input voltage. The last stage is the output stage appears at the final amplifier stage.

The first stage device is designed by four NMOS transistors which are connected in parallel in order to decrease the switch on-resistor for high current. All transistors have a maximum width and minimum length of 6.35-µm and 0.13-µm, respectively. The current is drawn about 0.81 mA. The input matching consists of Cin and Lin is used for circuit simplicity. The biasing voltage is 0.5 V.

The amplifier stage uses a common-source (CS) amplifier consists of twelve transistors in parallel to minimize the switch on-resistance. All transistors have a width of 6.52-µm and minimum length of 0.13-µm, it draws 0.83 mA current from 1.3 V supply voltage. The biasing voltage of 0.4 V is chosen for M2. The bias point is picked due to the small quiescent current through the transistor drain that showing the transistor is biased close to the cut off region.

The load network of output stage is designed base on the harmonic resonators to shape the drain wave forms in the time domain. Practically, only the first three harmonics are considered in realizations of microwave

class-F [4]. Therefore, the parallel network L4 and C4 is designed to be resonated at the fundamental frequency 2.4 GHz and open for other frequencies. Meanwhile, the parallel-resonant L3 and C3 is resonant at the third harmonic. The capacitors C1 and C2 are DC blocking capacitor and part of the overall matching network. The third harmonic represents a small inductance between the drain and the load which can be tuned out by adjusting the value of C2 to improve coupling to the load.

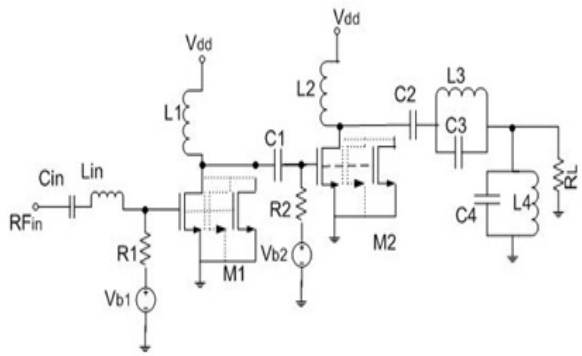

Figure-1. Schematic of the proposed LNA.

SIMULATION RESULTS

The circuit design of two stages class-F PA is simulated by Mentor Graphics software. All the components are implemented using 0.13-µm CMOS technology. The simulated drain voltage and drain current waveform of the power stage is shown in Figure-2. As can be seen, there are no overlapping with each other between drain voltage and drain current which mean that the maximum level of voltage and current are not same. Therefore, high efficiency can be obtained by minimizing the power dissipation of drain current and voltage. Non-zero of the minimum voltage is due to the effect of transistor's on-resistance.

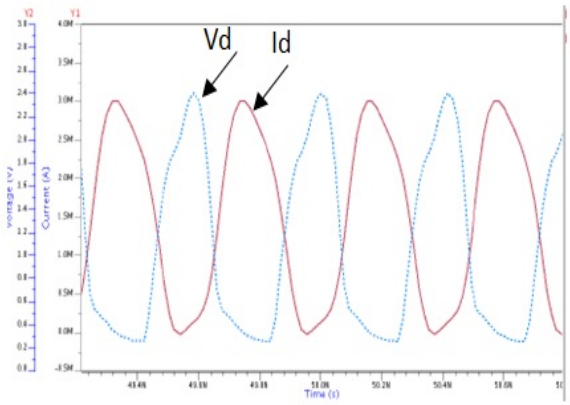

Figure-2. M2 drain current and drain voltage transient response.

The simulated result for the output power (Pout) and PAE versus input power (Pin) is shown in Figure-3. It can be seen that the output power is proportional to the input power. At 1.0 dBm input power, the amplifier delivers output power of 12 dBm with 60 % PAE. However, the PAE is degraded due to the parasitics' effects when the input power beyond 1.0 dBm.

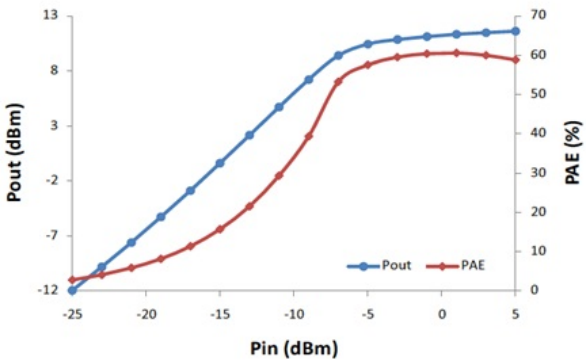

Figure-3. Relationship between output power, PAE and input power.

The relationship between gain, PAE and drain efficiency (PE) is shown in Figure-4 The maximum PAE of 60% and PE of 62.5% are reached at 1.0 dBm input power. However, beyond this point, drain efficiency still goes up while PAE starts decreasing. It means the signal is being clipped and the power amplifier becomes saturated. It can be seen from Figure-4 also that the maximum gain of 21.83 dB occurs at -8.49 dBm input power before it starts drop off at 1db compression point.

Finally, the simulated result of the output power and PAE as a function of frequency is depicted in Figure-5. The input power is setting at 0 dBm. The performance of the output power and PAE are fairly constant between 2.30–2.50 GHz frequencies' ranges, thus given the bandwidth of the PA is about 200 MHz.

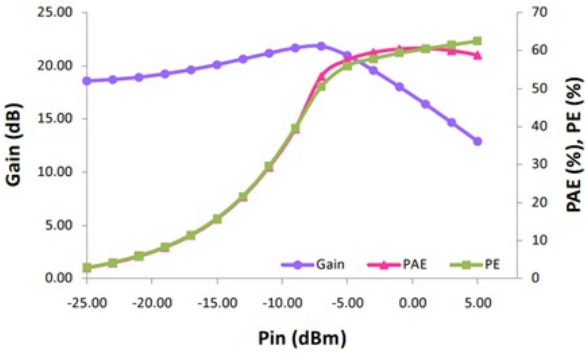

Figure-4. Gain, PAE and drain efficiency versus input power.

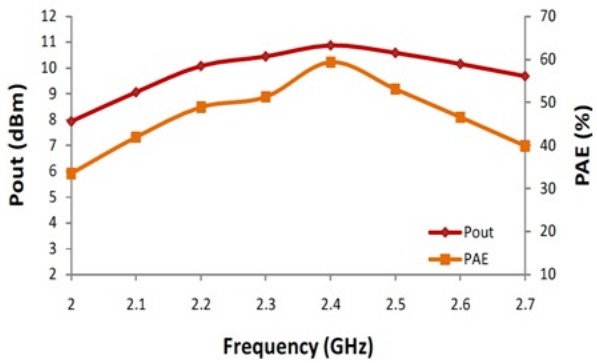

Figure-5. Output power and PAE as a function of frequency.

The comparison of the proposed class-F PA with previously reported PA is summarized in Table-1. The performance of the proposed PA demonstrates that the PAE and the chip are better than those reported PAs [4][9-11]. However, the output power of 12 dBm is low due to low supply voltage is used in this technology that should be improved in the future work. Figure-6 shows the layout of class-F PA with the chip area of 0.91 mm × 0.72 mm including the pads. This layout will be tape out for fabrication and testing in the future.

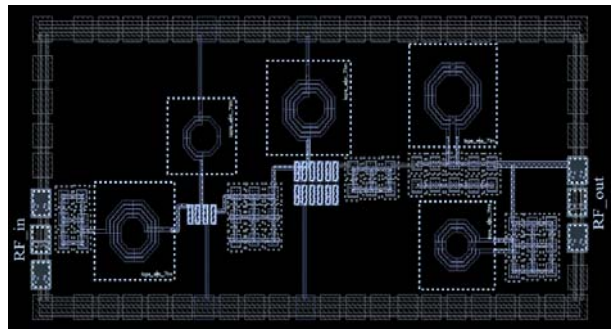

Figure-6. Layout of the proposed class-F PA on 0.13-µm CMOS process.

Table-1. Performances comparison of class-F power amplifier.

References	[4]	[9]	[10]	[11]	This Work
Process	CMOS 0.18- µm	GaAs pHEM	AMS 0.35-µm	CMOS 0.18- µm	CMOS
Frequency (GHz)	2.4	2.0	2.4	2.4	2.4
Vdd (V)	3.0	35	1.3	0.8	1.3
Pout (dBm)	19.3	38	14	20	12
PAE (%)	49.6	50	18	49	60
Chip Size (mm^2)	N/A	2.85	N/A	0.71	0.66

CONCLUSIONS

A 2.4 GHz two stage class-F PA with parallel transistors for wireless applications in the 0.13-µm CMOS technology is presented. The proposed design employed driver stage with amplifier stage structure to obtain high efficiency and high output power. Moreover both the input and the output matching network has been integrated on-chip. The high efficiency can be obtained by using the parallel transistors thus decrease the transistor switch on-resistance. The proposed PA obtains 12 dBm output power from the simulated results. In addition, the maximum PAE of 60% is achieved with low supply voltage. The proposed PA is suitable for low output power wireless communication systems such as Bluetooth's mobile phone. In addition, the PA can be integrated in a system on chip (SoC) with other RF transceivers.

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