VOL. 10, NO. 18, OCTOBER 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

DESIGN OF LOW POWER SINGLE STAGE FOLDED CASCODE CMOS OPERATIONAL AMPLIFIER FOR PIPELINE ANALOG-TO-DIGITAL CONVERTER

Izatul Syafina Ishak[1], Sohiful Anuar Zainol Murad[1] and Faizah Abu Bakar[2]
[1]School of Microelectronic Engineering, University Malaysia Perlis, Kangar, Perlis, Malaysia
[2]Department of Electronic Engineering, Faculty of Engineering Technology, Universiti Malaysia Perlis (UniMAP), Kampus Uniciti Alam, Sg. Chuchuh, Padang Besar, Malaysia
E-Mail: izatul_syafina@yahoo.com.my

ABSTRACT

This work presents a low power single stage folded cascode CMOS operational amplifier (op-amp) implemented in 0.13 µm CMOS Silterra technology. This op-amp will intended for pipeline analog-to-digital converter (ADC). The proposed op-amp is employed folded cascode topology for obtaining a high DC gain and fast settling with high unity gain. The NMOS input differential pair is used to obtain larger output gain. The simulation results show that the op-amp achieved DC gain of 64.5 dB and unity gain bandwidth (UGB) of 133.1 MHz at 1.8 V supply voltage. Moreover, the cut-off frequency of 95.62 MHz is attained. A 1 pF load capacitor is applied in performing a stable phase margin of 68.4°. The slew rate of 22.6 V/µs with 72.4 ns settling time is obtained with a 0.3 mW of power consumption.

Keywords: analog-to-digital converter, CMOS operational amplifier, folded cascode, single stage, pipeline.

INTRODUCTION

Analog-to-digital converter also known as ADC is a paramount block in analog or digital mixed signal application. Commonly, this block functions as an interface between analog circuits and digital sub-systems that indispensable for wireless telecommunications, instrumentations, medical applications and also audio and video processing [1]. ADC is classified in a variety of architecture such as delta-sigma, successive approximation, pipeline, folding/interpolating and flash [2]. The rapid growth of technologies which demand a high speed with high accuracy device, the pipeline ADC become an appropriate architecture which provided a small number of mega samples per second (MSPS) and up towards 100 MSPS of sampling and rates besides capable a medium to high resolution of 8 to 14 bits [1]. As shown in Figure-1, the pipeline structure basically constructs by a low resolution ADC, digital-to-analog converter (DAC) and an amplifier.

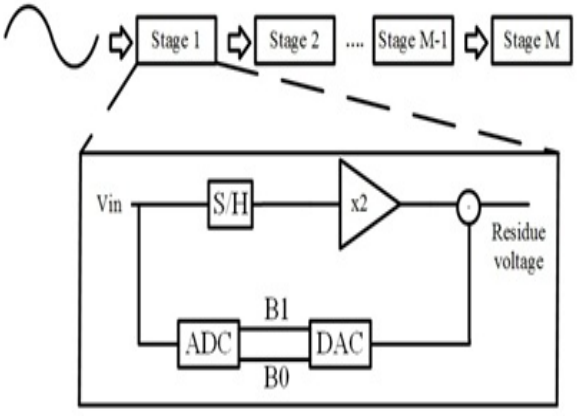

Figure-1. Conventional pipeline ADC architecture.

Amplifier or operational amplifier (op-amp) become an important role in ADC structure because it is an integral part for analog and mixed signal systems. Op-amp has been classified into two stages which are single stage and multi stage. Traditionally, the single stage op-amp is designate with two topologies which are telescopic and folded cascode while two-stage and gain boosting topologies is related to the multi stage op-amp. The design of single stage op-amp is vastly discussed because of the increasing demand for high performance op-amp with a high gain and low power consumption.

The telescopic topology is a simple structure and endorsed a high gain as well faster performance [3]. The term of 'telescopic' is referred to the cascades structure that attached between the voltage supply and the transistor in the differential pair which, occurs in a structure of each transistor branch that connected directly together in a straight line [1]. Generally, this structure consist lesser current legs thus produces a smaller swing. Meanwhile, the folded cascode structure is normally customized from the telescopic structure and provides higher gain and better performance [4] compared to the telescopic since the structure consists more currents leg. Generally, this structure is stated as 'folded cascode' because of small signal current is folded up or to down [1].

Op-amp circuit design

Figure-2 shows a schematic of the proposed op-amp design. The design is based on folded cascode topology since this topology has been used for obtaining a high DC gain and fast settling with high unity gain besides low power consumption [5]. As illustrates in Figure-2, the folded cascode is designed with using NMOS input differential pair because these input type can perform larger output gain compared to PMOS input type.

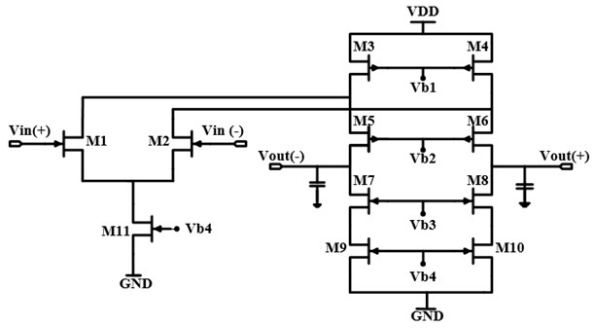

Figure-2. Schematic of the proposed folded cascode op-amp.

Based on the proposed op-amp schematic, the folded cascode configuration comprises of two structure which are differential amplifier that presents by transistors of M_1-M_2 and cascode structure presents by transistors of M_3 to M_{10}. However, this configuration is supplied by same V_{DD} value that is 1.8 V. The differential amplifier is operated by ±1.2 V of Vin while cascode structure is generated by a low-voltage cascode that works by connecting the nodes as stated as V_{b1}, V_{b2}, V_{b3} and V_{b4} to the DC bias voltage. The function of a 1 pF capacitor load in this circuit is to stabilize the phase that produce by the op-amp circuit.

SIMULATION RESULTS

The proposed single stage folded cascode op-amp as shows in Figure-2 is simulated using Cadence software to verify the op-amp behavioral such as DC gain, unity gain bandwidth, phase margin, and so on. Figure-3 illustrates the graph for gain and phase margin of op-amp. As plot in the graph, 64.5 dB of the DC gain is achieved with 68.4° of phase margin. Moreover, the unity gain bandwidth and cut-off frequency of op-amp is also obtained from this graph. The unity gain bandwidth is attained at 133.1 MHz while cut-off frequency is 95.62 MHz. Figure-4 shows the result of transient analysis that performs the slew rate and settling time. By referred to the graph as depicted in Figure-4, the slew rate is defined as 22.6 V/µs with 72.4 ns of settling time.

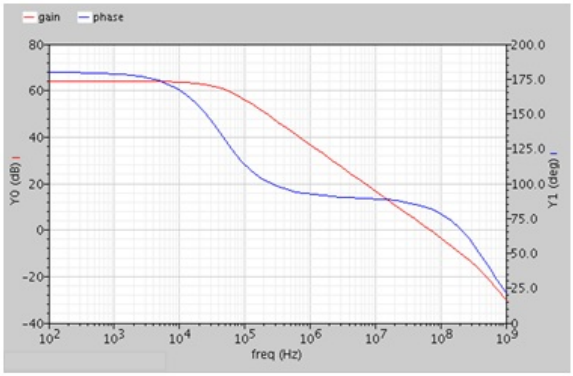

Figure-3. Gain and Phase margin.

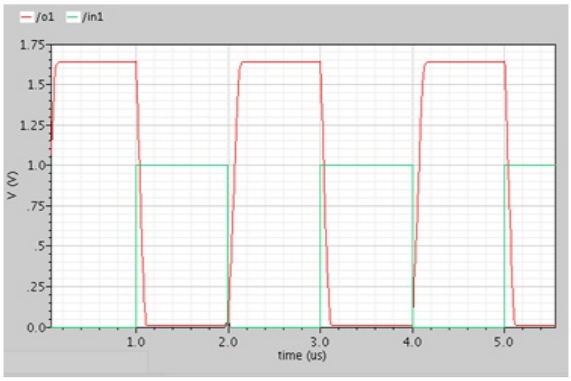

Figure-4. Slew rate and settling time.

Figure-5 shows the common mode rejection ration (CMMR) of op-amp that is performance 41.48 dB. This parameter measured the ability of an amplifier to reject common signals of both input. Meanwhile Figure-6 shows the plot of PSRR which is important in preventing the output being affected by noise or ripples at the voltage supply. As can be seen in Figure-6, the power supply rejection ration (PSRR) is 73.15 dB.

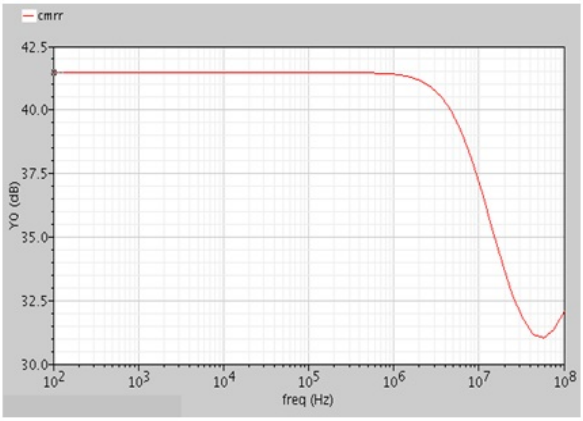

Figure-5. Common mode rejection ratio.

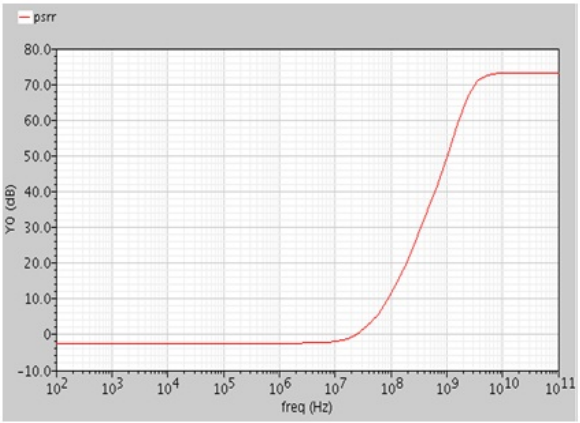

Figure-6. Power supply rejection ratio.

Table-1 shows the performance comparison of the proposed folded cascade op-amp with previously published works. It can be seen that the proposed op-amp obtains a very low power which is comparable to be implemented in a pipeline ADC application.

Table-1. Performances comparison of folded cascode op-amp design.

References	[6]	[7]	[8]	This work
CMOS Technology (µm)	0.18	0.18	0.18	0.13
Supply Voltage (V)	1.2	1.8	1.8	1.8
DC gain (dB)	63.9	90.39	80	64.5
Unity gain bandwidth (MHz)	114	700.7	1437	133.1
Phase margin (degree)	87.58	63.85	62.3	68.4
Slew rate (V/µs)	45.45	N/A	N/A	22.6
Settling time (ns)	63	0.84	N/A	72.4
ICMR (V)	1.2-1.8	0.5 – 1.2	0.49	0.5
CMRR (dB)	88.4	60	N/A	41.48
PSRR (dB)	103.2	N/A	N/A	73.15
Power consumption (mW)	1.38	3.24	88	0.3
Load capacitor (pF)	1.1	0.5	2.0	1.0

CONCLUSIONS

This paper presents design of a single stage op-amp that adopted the topology of folded cascode. The proposed op-amp is implemented in 0.13 µm CMOS Silterra process. The NMOS type for input differential pair is used to obtain larger output gain. The cascade topology is employed for achieving high DC gain and fast settling time with high unity gain. The simulation results indicate that the proposed op-amp is suitable to be implemented in analog-to-digital converter due to high DC gain and fast settling time with a very low power consumption.

REFERENCES

[1] Izatul Syafina Ishak, S.A.Z Murad and M.F Ahmad. 2014. "Low Power Folded Cascode CMOS Operational Amplifier with Common Mode Feedback for Pipeline ADC". International Integrated Engineering Summit (IIES2014), 1-4 December, Batu Pahat, Johor, Malaysia.

[2] D. Chaudhari and P. Gandhi. 2014. "A 1.8 V 8-bit 100MS/s Pipeline ADC in 0.18 µm CMOS Technology". International Journal of Science and Research (IJSR), Vol. 3 No.5, pp. 671-674, May.

[3] S. Kant and O.P Sahu. 2012. "Design of Low Voltage High Speed Operational Amplifier for Pipelined ADC in 90nm Standard CMOS Process". International Journal of Engineering Research and Technology (IJERT), Vol. 1 No. 4, June.

[4] X. Liu and J.F McDonald. 2012. "Design of Single-Stage Folded Cascode Gain Boost Amplifier for 14bit 12.5 Ms/S Pipelined Analog-to-Digital Converter" IEEE-ICSE, pp. 622-626.

[5] Z. Kun, W. Di and L. Zhangfa. 2011. "A High-performance Folded Cascode Amplifier". International Conference on Computer and Automation Engineering (ICCAE2011), pp. 41-44.

[6] Tushar Uttarwar, Sanket Jain and Anu Gupta. 2010. "Design of a High Performance, Low Power, Fully Differential Telescopic Cascode Amplifier using Common-Mode Feedback Circuit, Technological Developments in Education and Automation". Springer, pp. 249-252.

[7] M.K. Hati and T.K.Bhattacharyya. 2011. "Design of a Low Power, High Speed Complementary Input Folded Regulated Cascode OTA for a Pipeline ADC". IEEE Computer Society Annual Symposium on VLSI, pp.114-119.

[9] Gu Wei and Gao Wei. 2012. "Design of OTA with Common Drain and Folded Cascode Used in ADC". World Academy of Science Engineering and Technology, pp. 284-286.