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ENHANCE IMPLEMENTATION OF FPGA BASED LASER MISSILE FREQUENCY JAMMING SYSTEM USING SPATIAL PARALLELISM

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ABSTRACT

System performance, power consumption and cost are considered the key factor and criterion for the success or failure of any system. Increasing the system performance is a relative issue since that it can be done via multiple mechanism and approaches. In this paper, applying of spatial parallelism mechanism over the Field Programmable Gate Array (FPGA) platform is proposed to achieve this goal. The spatial parallelism can provide the ability for duplicating the tasks which can be processed via specific modules. System signals ranging from 1Hz to 200 MHz is covered. To avoid the limitation of the master clock of the Nios II Embedded Evaluation Kit (NEEK) board, Phase Locked Loop (PLL) is utilized to enable system from covering wide spectrum of signals. Laser missile frequency jamming system has the ability to process multiple frequencies per time. The multiple signals processing capability is handling the situation where multiple aircraft fighters are attacking a single target or even multiple targets. FPGA platform is used to be the implementation environment for this system which resulted in enriching proposed system with core features such as the low cost as well as decreasing the system complexity since the concurrent structure is used within this system. In this paper, a description of the system modules, the modules functionalities, the results obtained from each module, and the final results which have been shown on the touch screen of NEEK board. The results obtained in this research paper are accurate because of using PLL (200MHz) and the signal tolerance is equal to 5ns.

Keywords: embedded system design, FPGA system design, jamming system, spatial parallelism.

INTRODUCTION

The trend in any system development is to improve the performance as well as make the system responds in real-time way and this is requiring increase the number of processors. In some systems the technique to increase the system performance was done via increasing the frequency scaling and the drawback here will be the emitted amount of the power consumption as well as increasing the required memory size for such systems [1, 2].

For those systems which are implemented over the FPGA platforms, the techniques are more flexible. Field Programmable Gate Array is as the name implies an array of finite logical blocks that has distinguished characteristics. These blocks have the ability to be programmed and even re-programmed (in most cases) for the sake of keeping up with new functionalities of the design [3]. Each Logic block of an FPGA can be configured in such a way that it can perform a simple functionality and behave like a simple logic circuit or as complex functionality like microprocessor performance Where nowadays FPGA-based systems could combine the advantages of both of DSPs and ASIC which resulted in systems capable for rapid development cycles, high flexibility, high reliability, easy upgrading, and moderate costs [4]. One of these techniques is the spatial parallelism which can be harnessed to improve the performance and the throughput [5]. An improved laser missile frequency system design is proposed in this paper where the utilization of the system modules were increased since that the sub-functionalities of each of them have been distributed among those modules to be processed which resulting in increasing the system overall performance and also reducing the total time required for processing.

For the laser missile guidance systems, What-it called idiomatically Semi-Active Radar Homing (SARH) is considered as the most common guidance system used for laser missile technique. In fact, it's used mostly for longer range air to air and surface-to-air projectile systems. It can be thought that the missile itself is only a passive revealer of a radar signal - provided by an external ("off board") source as it reflects back from the target. The core principle of (SARH) is that there is no need for duplicating the use of radar on the missile itself since almost all the tracking systems consist of this hardware. Moreover, the radar resolution is closely related to the physical size of the antenna, and according to that there is no enough space to allocate guidance system in the missile cone to provide the required accuracy for guidance. Furthermore, multiple issues related to the core functionality of the system is handled, where signal emulator which has the signal generation task, address generator to store the processed data, and control module to direct the multiple diffused platforms.

The rest of the paper is organized as follows. Section 2 presents related work. Section 3 discusses key design modules in the system which performs the main functionality of the system. Section 4 presents the final

results obtained from the system which have been shown on the LCD touch screen of the (NEEK) board. Section 5 provides a brief conclusion and analysis about the results and the system performance.

RELATED WORK

The jamming system is a circuit used to disrupt communication between devices by prevents the destination device from receiving the sent signal. Laser missile jamming systems is a key tool in many aspects since it's considered as the hands of law enforcement, military, anti-terror applications and VIP protection. In the military field, the main purpose of jamming is to prevent communication among the enemy units. The main technique in the jamming system is to tune the jammer with the same frequency emitted from the transmitting station but with wrong information [6].

The core idea behind the frequency jammer is to increase the power associated with the noise signal which will be sent with the same frequencies of the original signal and in the same time decreasing the signal to noise ratio which will result in higher bit error rate. The (2-FSK) signals and the third-order Düffing oscillator model was used to be the enemy communication signals in the jamming system proposed by [7] which was based on chaotic nonlinear system. The signal is processed by the jamming guide unit and then its power will be amplified to be re-transmitted. The proposed system can be implemented using the TMS digital signal processing starter kit (DSK).

The infrared guided missile can be considered as a core weapon in the military field since it can use the reflected energy from the intended targets. [8] have proposed a scheme for jamming this kind of missiles. Where the IR missiles has tracking and missile guidance modules, the jamming module which was presented here is including signal processing unit and phase detector as well as tracking loop. Another mechanism has been introduced by [9] where researchers developed a jamming method for false target deceptive in order to facing the missile-born Synthetic-aperture radar (SAR). In this research, the proposed jammer unit functionality is to determine the phase signal of the missile-born SAR then modulating the Doppler frequency phase. After determining the signal phase, the proposed architecture calculated and modulated the Doppler frequency phase in azimuth direction to all of the ranges of the jamming signal bin phase as well as the delay corresponding time.

SYSTEM SPECIFICATIONS

The first part of the project includes associated function units which are required to accomplish the full functionality of this system; the second part consists of multiple functional modules that will detect in the beginning the frequencies which will be emitted from the transmission unit in general and specifically from the missiles launchers and continue processing the input data until passing these data to the LCD touch screen. The other proposed units within the first part are responsible for processing the detected frequencies until the result shown on LCD touch screen. The detected frequency will be distributed over many platforms to direct these frequencies away from their targets. In order to integrate the desired improvements aspects like efficiency and performance, some core concepts like spatial parallelism, locality and reuse in embedded application are harnessed. Figure-1 provides a conceptual illustration of the proposed system:

Figure-1 shows the top level design and the main system modules. As it can be seen, multiple signals have been provided to the input unit manager module which is responsible to distribute these signals over the multiple processing modules. On the other hand, the master on board clock which is (50 MHz) has been manipulated via the clock generator module to provide the system with frequency up to (200 MHz) using the PLL utilization. The following in this section will illustrate the design phases as well as the system modules and the functionality of these modules:

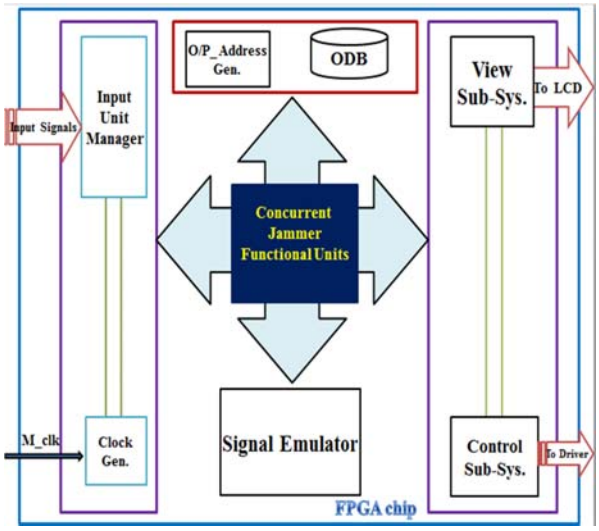

Figure-1. System top level design.

Signal emulator module

The first step in designing and implementation of this system was the signal emulator or signal generator module. In the cases when no input signals are available, the need to provide the test signals is required to check whether the system perform the functionality for which it is designed or not. The key functionality of this module is to generate known signals to compare with the proposed output of the system and this action is just for the demonstration purpose.

Jamming functional units

The next stage in this system design and implementation trip was the jamming module. This module in turn is including sub-modules and each of them has its own sub-functionality to be performed. The first required action is to detect the pulses embedded within the emitted signal from the laser missile launcher and this task was done via the pulse detection module and as follow:

a) Pulse detection module

The initial stage of this project was how to detect the frequencies emitted from the multiple missile launchers which is used to guide the missiles to its target. The frequencies will be detected by figure out how many pulses are included in this signal. The General Purpose Input / Output unit device (GPIO) is used to provide the system with the input signals in the normal cases. Master on board clock signal (50MHz) is used with the ability to increase that range by utilizing PLL to obtain up to 600 MHz which is the maximum value can be provided by the PLL [10]. The main principle of the circuit is to determine the width of the time period of the input signal and to do this, it first receives the input signal provided from the GPIO and counts the number of the pulses embedded within that input and then processing that signal depending on time period of the master clock of the board. With each clock cycle, the time period of the pulse will be calculated and an internal parameter will be increased then this parameter will be assigned at the end to the output. Once the number of the pulses is detected, the next is to convert this format to the frequency representation and this was done using the equation of time to frequency conversion and as below:

$$F = 1 / T \quad (1)$$

Where (F) represents the Frequency value which will be calculated and (T) represents the time period.

b) Signal conversion module

The detected frequency from the previous module will be in the binary format. In order to convert this format to the BCD format, this module is created for. The Double Dabble algorithm is used to perform this task. It is important issue to mention here that, proposed system is capable of detecting frequencies up to six digits. Temporal parameter is used to store both of the detected frequency in the binary form and the converted frequency to the BCD form also. The result of this algorithm will be a BCD representation and divided into ones, tens, 100s, 1000s, 10000s, and 100000s units. The key idea here is to shift the frequency in the binary form to the left with one bit for the first three time then we'll face two situation which are either the number in the binary form is (≤ 4)and in this case complete shifting the number to the left with one bit, or the value of the number is (≥ 5) then the next step is to add (3) to the shifted number and complete shifting to the left with one bit and so on until the entire input data shifted.

c) Distribution module

The 6-BCD digits which have been converted in the last stage will be multiplexed in this module to send a single digit at a time using 3-control signals. In the same time, the selected digit to be sent will be in the ASCII form in order to be viewed on the touch screen of the NEEK board. Now, the selected digits at each stated of the temporal signal will be assigned to the final output but in the ASCII form and not in the BCD form.

d) Touch screen view-sub system

First initialize the LCD touch screen itself. This action is required for preparing the LCD touch screen to receive the commands (Read or Write).the beginning of this preparation stage represented in enabling the LCD itself first using internal signal as well as initialize the LCD. The mechanism in viewing the characters which includes both letters and digits is all about the use of the finite state machine (FSM) whereas the module structure based on dividing the result shown on the LCD touch screen to three partial stages The first state machine used in this module was to control the LCD touch screen itself via four states. The second state machine was to display the first three characters of the word "Detected" where this module considered the letters (DET.) and the first four letters (FREQ) of the word "Frequency" and the special character (=) to have a final result like ("DET. FREQ= 83300 Hz"). The next state machine will begin to display the digits which represent the emitted frequency which is the result of the all previous stages. The last state machine is used to assign values to be shown in touch screen at each state of touch screen enabling state machine where the first four values is assigned to the control signals.

Concurrent jammer module

"We live in a parallel world", these words explain the constant pursuit of the designers and researchers to improve the performance by speeding up the computation and increase throughput. The ideal parallel computation architecture that can be used in systems is the one which has large logic blocks of independent computation which resulting in execution these blocks in a concurrent manner. To process more than a signal at a time, the spatial parallelism concept has been harnessed here. The main advantage of the spatial parallelism that there is multiple similar subtasks are executed in simultaneously manner [11]. The applied spatial parallelism over this system can be look at as a parallel composition of the data which results in partitioning the data spatially over the available processing units as well as duplicating the hardware would improve the performance through processing multiple

tasks at a specific period of time. The harnessing of this concept result in various benefits starting from capability of processing more than a signal per time, decreasing the FPGA used resources, improving the overall system performance, and increasing the system throughput. The mechanism of the spatial parallelism was used to split the multi-functional units of the system into several parts and each sub-functionality unit will be processed by different module.

Control sub-system

After the emitted frequency from the laser missile launcher is detected and been processed via the previous modules, the time to control multiple jamming platforms to be directed towards the attacking launchers has come. This module is responsible for directing four platforms towards the launchers in order to transfer the jamming frequency towards these launchers. The perfect way to control those multiple motor drivers is through the use of the pulse width modulation (PWM) which used digital signals to control motors rather than using continuously signals. The PWM input is in general is either 8-bits or 16-bits. For this proposed module, an 8-bits input have been used. The motors which are controlled by the pulse width modulation are guaranteed to have lower jitter time [12]. The behavior of the control unit will simulate four combat aircraft attack for single target from different directions of the target; these directions are the front, back, right, and left where this system proposes that the aircrafts will launch the laser missile towards the target only from these directions and otherwise there will be an overlap between the attacking aircrafts and it will be useless to attack the targets from more than these directions. Table-1 is showing the pulse width modulation effectiveness obtained from control sub-system.

Table-1. Pulse width modulation effectiveness.

Module states	Percentage of effectiveness
PWM 0	0 %
PWM 1	15 %
PWM 2	30 %
PWM 3	45 %
PWM 4	60 %
PWM 5	75 %
PWM 6	90 %
PWM 7	100 %

Address generation module

In order to store the processed data or the frequencies which was detected by the system, a memory unit has been created with (1 KB) size. In system design, it's obvious that accessing the memory is a costly issue in term of both time and power. Since the data access can be sometimes considered as vectors indexed access and these vectors are stored in memory, the functionality of the output address generator is to generate a memory address for each one of the processed data within the memory size with each clock cycle to ensure that each one of the frequencies has a unique memory address.

Output data buffer module

The core purpose of proposed system design was to improve the performance and the overall throughput by the use of spatial parallelism but whenever the I/O data will have the access to the memory; this will cause deterioration of the system speed. In order to avoid this situation, an output data buffer is used to temporarily store data and instructions which will result in allowing for several data transmission to be processed concurrently alongside with data processing. This module is using the dual channel technique to implement its functionality.

RESULT AND SYSTEM EVALUATION

In this section, the highlighting of the performance of the laser missile frequency jamming system and the results obtained from implementation over NEEK board are presented. The synthesized sub-functionality modules which were designed to construct this project are presented here accompanied by the results of each module. The system overall performance and the obtained results are introduced and analyzed to declare the Lurking strength of the system. First of all, for the results obtained from the verification volume which has been implemented via the simulation CAD tool (Quartus II web edition) presented by Altera will be outlined as follows respectively. the result obtained from signal generation module is illustrated in Figure-2. Also, the frequency which has been detected by the pulse detection module is shown in the Figure-3.

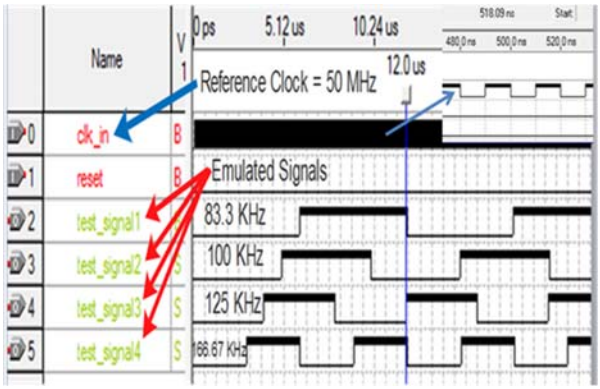

Figure-2. Emulated signals via signal emulator module.

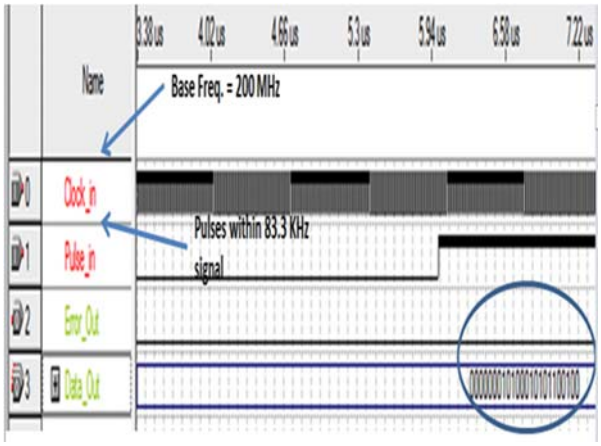

Figure-3. Detected frequency by pulse detection module.

As it can be noticed that the base frequency is (200 MHz) and the detected frequency is represented in the binary form. The result obtained from signal conversion module is shown in Figure-4.

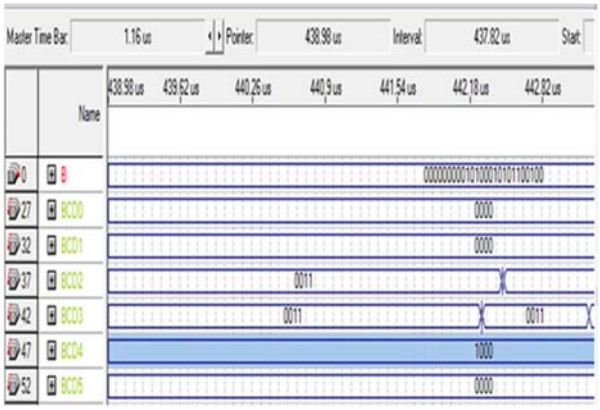

Figure-4. The converted frequency by signal conversion module.

The higher BCD digit which is (BCD5) is assigned to the last digit (8) and in the same way other digits assigned to the remaining digits (3, 3, 0, 0) respectively. For the modulated signal resulting from the control sub-system, the result is shown in Figure-5.

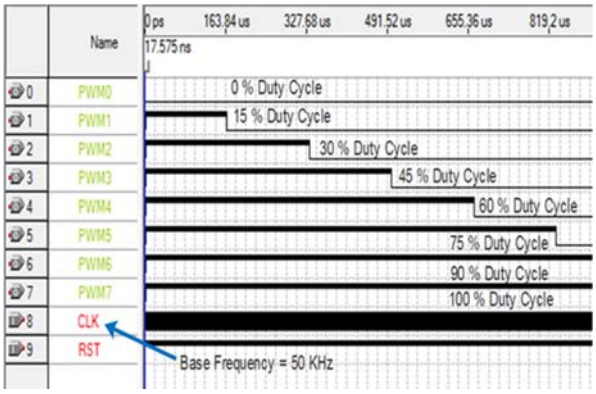

Figure-5. The modulated signals result.

Now, after showing the temporal results obtained from the modules separately; the final results which have been shown on the LCD touch screen of the (NEEK) board as well as the oscilloscope are shown in Figure-6.

Figure-6. LCD Touch screen display for (83.3 KHz) signal.

As it can be seen from the above figure, the Phase Locked-loop for the system is (200 MHz) and the detected frequency here in this case is (83.3 KHz). For the time, the result as shown above is 12 µs. Figures 7 and 8 show the results for the function generation and the oscilloscope for the same input signal (83.3 KHz).

Figure-7. Frequency generator result for signal (83.3 KHz).

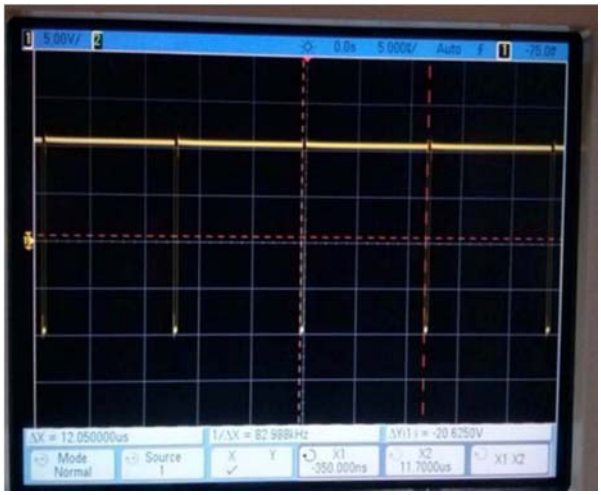

Figure-8. Oscilloscope view for signal (83.3 KHz).

CONCLUSIONS

Many features within the Altera® Nios II Embedded Evaluation Kit, Cyclone III Edition have been harnessed to implement this project such as the LCD touch screen alongside with the switch inputs and LEDs. The obtained results from the hardware implementation were much faster in compare with the results obtained from the software implementation of the system. The system performance had a quantum leap when the FPGA chip unique characteristics and spatial parallelism principle applied over the system. The FPGA chip provided the system with abilities comes in the forefront the flexibility, re-configurability, and reliability. Considering the obtained results, it's obviously can be concluded that applying the spatial parallelism principle enabled the system modules to process multiple data per time to perform multiple outputs and this decrease the overall system complexity as well as increasing the modules utilization. Depending on the results which were shown on the LCD touch screen, The exploitation of NEEK board has enhanced the system performance in many aspects like the speed as well as the flexibility in implementation the design whereas the NEEK shows the desired results even when there was a noise within the input signals. The research results show that the real time processing for multiple signals at a time can be done and here it can be concluded that the spatial parallelism can be considered as a solution for those embedded systems which requires real-time processing feature.

REFERENCES

IBM. 2009. Cell Broadband Engine Programming Tutorial. Retrieved. 05-06.

John Shalf. 2015. The New Landscape of Parallel Computer Architecture. Retrieved 2015-04-25.

Trimberger Stephen M. 1994. Field-Programmable Gate Array Technology.

Demler Michael. 2011. Dual ARM Cortex-A9 MPCore features 28-nm, low-power programmable logic for high-end embedded systems. K. Elissa. Title of paper if known. Unpublished.

Behera Ranjan Kumar, Kumar Deepak and Pandey K. S. 2013. Concept, Design and Performance Evaluation of VLVIW Processor. International Journal of Scientific Engineering and Technology. 2(7).

http://en.wikipedia.org/. 2012. Jammimng System.

Liu Meng, Mao Lingfeng, Zhu Canyan and Ji Aiming. 2013. Research on Application of Nonlinear System in Communication Jamming. Paper presented at the 2013 International Conference on Mechatronic Sciences, Electric Engineering and Computer (MEC), Shenyang, China.

Kim Ga-Young, Kim Byoung-Ik, Bae Tae-Wuk, Kim Young-Choon Ahn, Sang-Ho and Sohng Kyu-Ik. 2010. Implementation of a Reticle Seeker Missile Simulator for Jamming Effect Analysis IEEE Signal Processing Magazine.

He Xiaodong, Zhu Jun, Wang Jun, Du Dongping and Tang Bin. 2014. False Target Deceptive Jamming for Countering Missile-Borne SAR Paper presented at the 2014 IEEE 17th International Conference on Computational Science and Engineering.

Altera. 2014a. Altera Phase-Locked Loop (Altera PLL) IP Core User Guide.

Behera Ranjan Kumar, Kumar Deepak and Pandey K. S. 2013. Concept, Design and Performance Evaluation of VLVIW Processor. International Journal of Scientific Engineering and Technology. 2(7).

Horak Goran, Bilas Vedran and Vasic Darko. 2008. Noise Analysis of the Pulse-Width Modulator for Quasi-Digital Sensors. IEEE Trans. Comput. IEEE Transactions on Computers.

R. Nicole. Title of paper with only first word capitalized. J. Name Stand. Abbrev, in press.

Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa. 1982. Electron spectroscopy studies on magneto-optical media and plastic substrate interface. IEEE Transl. J. Magn. Japan, 2: 740-741, August 1987 [Digests 9th Annual Conf. Magnetics Japan. pp. 301, 1982].

M. Young. 1989. The Technical Writer's Handbook. Mill Valley, CA: University Science.