



DESIGN AND DEVELOPMENT OF HARVESTER RECTENNA AT GSM BAND FOR BATTERY CHARGING APPLICATIONS

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ABSTRACT

This paper describes the design of the harvester RECTENNA for charging mobile applications. A rectenna (RECTifying anTENNA) is a combination of a receiving antenna and a rectifying circuit which converts RF signal to into direct-current (DC) voltage. The design consists of microstrip patch antenna and Villard voltage doubler circuit which is designed at 900 MHz band. 3 stages of Schottky diode voltage doubler circuit are designed and simulated in this paper and matched to the antenna design. CST is used for modelling the antenna using transmission line method, and ADS used for the modelling and simulation of the rectifier. The output voltage of the rectifier is 5.014 V which indicates the suitability for charging mobile applications.

Keywords: battery charging, RECTENNA, microstrip patch, doubler circuit.

INTRODUCTION

Energy harvesting is the process of collecting energy which is available from different types of sources like Radio Frequency (RF) source, solar energy, piezoelectric etc. Energy harvesting of RF is the process of collecting ambient electromagnetic energy and converting it into DC power [1].

The concept of energy harvesting system is shown in Figure-1. It consists of antenna, matching network, RF-DC conversion and load circuits. The RF input signal is harvested using antenna with matching circuit. The matching circuit is used to decrease the reflected power from the source into the rectifier circuit. The rectifier circuit is used to convert the RF input into DC where it passes through to the DC output load used in different applications [2].

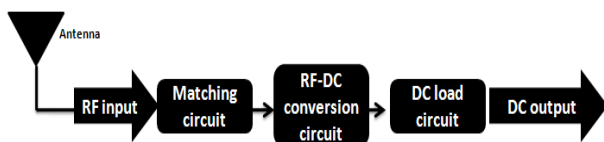


Figure-1. Schematic view of RF energy harvesting system.

In case of the power from ambient RF sources, the amount of the harvested energy is small. For this reason a single antenna configuration is not sufficient for harvesting the RF energy. An antenna array configuration is essential since it is able to produce low incident power [3, 4]. Some of the studies used the voltage multiplier method in rectifier stage to increase the harvested output from the antenna [5].

The rectifier circuit converts the input of RF signal received by the antenna into a DC voltage [6].

Voltage multiplier functions as charge pump and its basic circuit consists of a Villard voltage doubler known as Cockcroft-Walton voltage multiplier [7]. The design and testing of the RECTENNA have also been reported in the previous studies [8-14]. A DC voltage of twice the peak amplitude of the alternating current (AC) signal can be generated at the DC output [12].

In this paper, the work is focused on the design and analysis of the RECTENNA using Agilent ADS simulation and Microwave CST studio. In Agilent ADS simulation, the signal generator block is used to generate the RF AC signal into the RF harvester circuit. The AC voltage signal is converted to DC voltage signal by using a rectifier circuit. Several stages of the rectifier are cascaded in the design to increase the DC voltage level.

The contents of this paper are arranged as shown in Figure-2. Section 2 discusses on antenna design whilst the rectifier implemented using HSMS-285B Schottky diode is explained in Section 3. In Section 4, the results

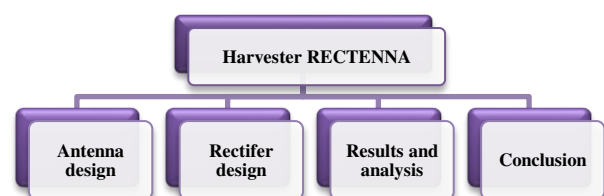


Figure-2. Block diagram for the sections of this research.

and discussions are explained accordingly. The final section concludes the findings.

Design of Microstrip patch antenna

The design of microstrip patch antenna consisting a flat rectangular patch of metal mounted over a larger



sheet of metal called a ground plane is shown in Figure 3. The typical structure of microstrip patch antenna includes the parameters such as L_p = length of the patch, W_p = width of the patch and h_p = height of dielectric substrate, where ϵ_r = dielectric constant.

The following equations (1-5) are used to compute parameters of patch antenna and they are based on the transmission line model [15-18]. The primary step in the design procedure is to determine the width of the patch (W_p) and the dimension cannot be too small to avoid excitation of transverse resonance mode. The width dimension is determined using Equation. (1);

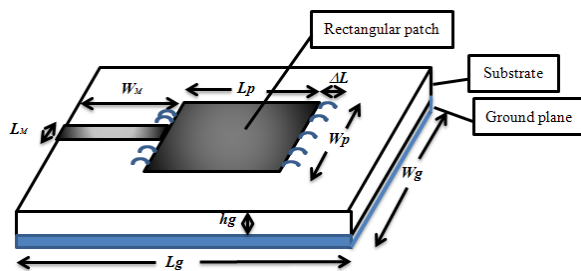


Figure-3. Layout of microstrip patch antenna.

$$W_p = \frac{c}{2f_r \sqrt{(\epsilon_r + 1)/2}} \quad (1)$$

Where;

c is the speed of light, (3×10^{11} m/s).

f_r is the operating frequency.

ϵ_r is the dielectric constant of the substrate.

With lower dielectric constant value, this provides better efficiency and wider impedance bandwidth. The antenna somehow contributes to a larger size by using higher dielectric constants. This leads to less efficient and relatively smaller bandwidths [16].

- a) Effective dielectric constant (ϵ_{eff}) can be determined using Equation. (2):

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(\frac{1}{\sqrt{1 + 10h_p/W_p}} \right) \quad (2)$$

Where;

h_p is the height of the patch in mm.

W_p is the width of the patch in mm.

Thicker substrates generate better efficiency whilst larger bandwidth and thinner substrates minimizes coupling with reduced efficiency and relatively smaller bandwidths.

- b) Equation (3) calculates the effective length of the patch (L_{eff}). Increasing its value leads to an increase of the patch size. Smaller frequency leads to larger L_{eff} , whilst larger frequency leads to smaller L_{eff} .

$$L_{eff} = \frac{c}{2f_r \sqrt{\epsilon_e}} \quad (3)$$

- c) The length extension (ΔL) is determined using Equation. (4):

$$\Delta L = 0.412h_p \times \frac{((\epsilon_e + 0.3) \times (\frac{W}{h_p} + 0.264))}{((\epsilon_e - 0.258) \times (\frac{W}{h_p} + 0.813))} \quad (4)$$

where ΔL is the extended patch length. Increasing its value leads to decreasing of the length and size of antenna, measured in mm.

- d) The actual length of the patch (L_p) is calculated using Eq. (5). This will determine the performance of antenna where by increasing its value gives an increase in its efficiency.

$$L_p = L_{eff} - 2\Delta L \quad (5)$$

The design parameters for the patch antenna using resonant frequency of 900 MHz are tabulated in Table-1. The dimension for each parameter is determined from equations (1- 5) accordingly.

Table-1. Parameters of microstrip patch antenna.

Parameter	Value
Resonance frequency	900 MHz
Dielectric constant ϵ_r	4.3
Patch dimensions (L_p, W_p, h_p)	90 mm, 90 mm, 0.34 mm
Microstrip dimensions (L_M, W_M, h_M)	34 mm, 8 mm, 0.34 mm
Ground dimensions (L_g, W_g, h_g)	180 mm, 146 mm, 0.34 mm

Simulation of microstrip patch antenna

The design is constructed with a ground plane layer that is located under the substrate of FR-4. The copper patch is mounted on the top layer. The simulation of the proposed microstrip patch antenna is carried out using CST Microwave Studio 2014. The simulated antenna return loss curve is plotted in Figure-4. The simulated result shows that the impedance bandwidth covers 0.82-0.93 GHz which is equivalent to 1.4% bandwidth that center frequency of 0.90471 GHz.

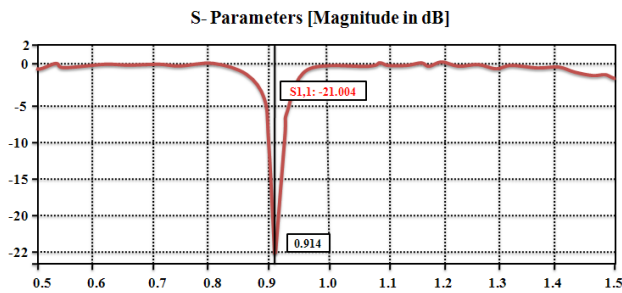


Figure-4. Return loss of microstrip patch antenna at frequency 0.9 GHz.

Figure-5 shows the simulated results for *H*- plane radiation pattern for resonance frequency of 0.9 GHz. It can be observed that *H*- plane radiation pattern is directional with main lobe directed at zero. The directives of the main lobe are found to be 6.5 dBi at frequency of 0.9 GHz.

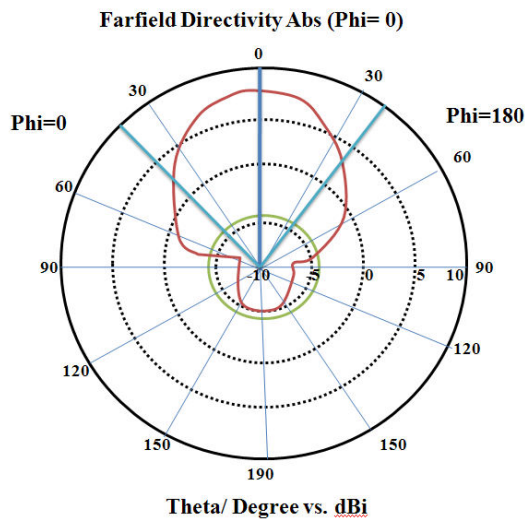


Figure-5. H-field of the microstrip patch antenna at frequency 0.9 GHz.

In Figure-6 the main lobe directions are at 0 and the magnitude of the *E*- plane directives is 6.5 dBi. The black lobe levels at frequency of 0.9 GHz is -7.8 dB.

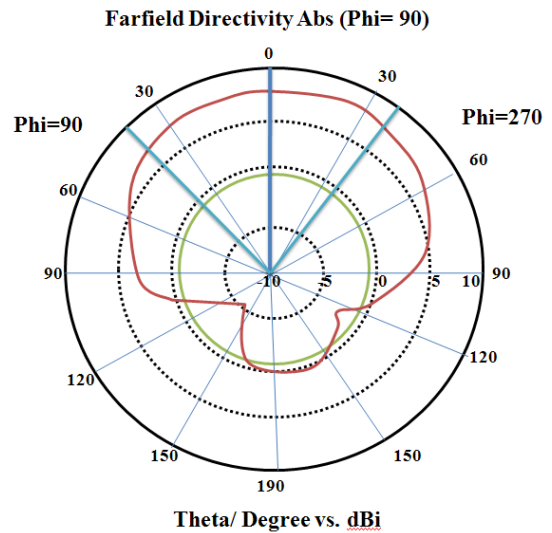


Figure-6. E-field of the microstrip patch antenna at frequency 0.9 GHz.

Figure-7 shows the Farfield pattern of microstrip patch antenna at frequency 0.9 GHz showing a directional beam toward 0.0 dBi. The color of the beam shows the value of the directivity gain with red color indicating the largest value and green color, the smallest value. The radiation pattern shows an efficient antenna design.

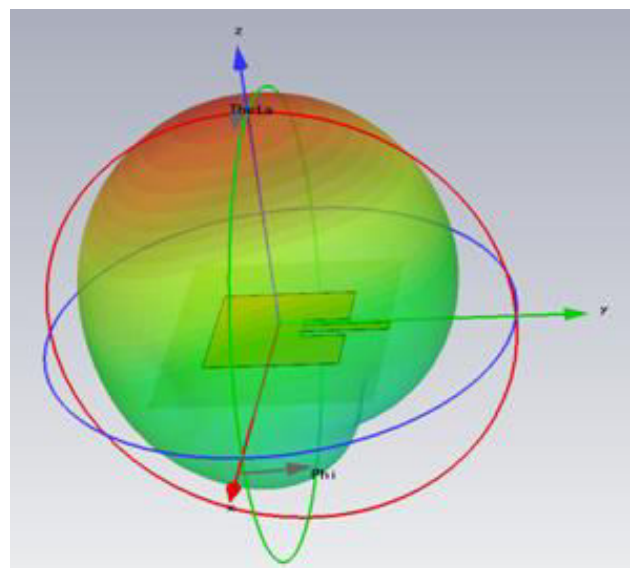


Figure-7. Far field of the microstrip patch antenna at frequency 0.9 GHz.

Design of the rectifier

Figure-8 shows the design of the rectifier circuit constructed from a three-stage voltage double circuit. This circuit contains 4 parts: signal source, matching circuit, rectifier circuit and DC load. Signal source generates 0.03 V to the rectifier circuit at frequency of 0.9 GHz.

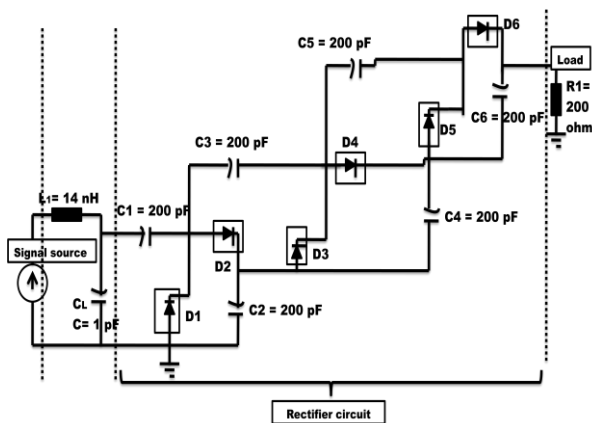


Figure-8. Three- stage voltage doubler using schottky diode HSMS 285B.

Matching circuit is placed between the source and the rectifier to reduce the dissipated power between the source and the rectifier. It will then increase the output voltage of the circuit. This circuit consists of inductor value of 14 nH and capacitor of 1 pF.

Rectifier circuit contains two capacitors and two diodes in every stage. It is used to generate DC voltage of twice the peak amplitude of the input AC signal. Increasing the stages of rectifier will increase the output voltage of the circuit. Capacitors used are 200 pF for each capacitor.

As for diodes, the multiplier circuit utilizes a Schottky diode HSMS 285B as shown in Figure-9. The output voltage across the load decreases during the negative half cycle of the AC input signal. The voltage is inversely proportional to the product of resistance and capacitance across the load. Without the load resistor in the circuit, the voltage would be held indefinitely in the capacitor behaving like a DC signal, assuming ideal components. The capacitors are charged to the peak value of the input RF signal and discharged to the series resistance (R_s) of the diode. Thus the output voltage across the capacitor of the first stage is approximately twice that of the input signal. As the signal swings from one stage to another, there is an additive resistance in the discharge path of the diode and increase of capacitance due to the stage capacitors [19].

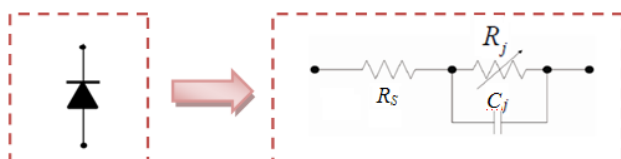


Figure-9. Schottky diode and its equivalent linear circuit model.

Design of the rectifier using Schottky diode

Villard voltage doubler circuit is designed and simulated by Advanced Design System (ADS) software. This circuit is optimized and achieved by using Schottky diode pair HSMS-285B for $R_s = 25 \Omega$, $C_j = 0.18 \text{ pF}$, $B_v = 3.8 \text{ V}$ which is chosen for applications below than 1.5 GHz. Table-2 shows the parameters value in the design [20]. The attractive features of this diode include: low forward voltage, low substrate leakage, fast switching and uses the non-symmetric properties of a diode to allow unidirectional flow of current under ideal situation.

The equivalent linear model can be used for the diode is shown in Figure-9. R_s is series resistance of the diode, C_j is the junction capacitance and R_j is the junction [21]. The parameter extractions are given in Equation. (6)-(11).

Table-2. Parameters of the diode HSMS-285b [20].

Parameters	Units	HSMS-285B
B_v	V	3.8
C_{Jo}	pF	0.18
E_G	Ev	0.69
I_{BV}	A	3E-4
I_s	A	3E-6
N	No unit	1.06
R_s	Ω	25
$P_B(V_J)$	V	0.35
$P_T(XTI)$	No unit	2
M	No unit	0.5

$$Y_z = Y_{Cj} + Y_{Rj} \quad (6)$$

Equation (6) related to the frequency of operation is given by

$$Y_z = j\omega C_j + \frac{1}{R_j} = \frac{j\omega C_j R_j + 1}{R_j} \quad (7)$$

The impedance Z of the linear model is given by

$$Z = \frac{R_j}{j\omega C_j R_j + 1} \quad (8)$$

The total impedance Z_T is given by

$$Z_T = R_s + \frac{R_j}{j\omega C_j R_j + 1} \quad (9)$$

R_s is the series resistance of the circuit and R_j is given by Equation. (10) [20].



$$R_j = \frac{8.33 \times 10^{-5} \times N \times T}{I_b + I_s} \quad (10)$$

Where:

I_b = Bias current in μA ;

I_s = saturation current in μA ;

T = temperature (K);

N = ideality factor.

In Equation (8), R_j and C_j are constants and the frequency of operation (ω) is the only variable parameter. As the frequency increases, the value of Z is almost negligible compared to the series resistance R_s of the diode. From this it concludes that the function of the diode is independent of the frequency of operation.

RESULTS AND DISCUSSIONS

Figure-10 shows the results of simulation the rectifier circuit without matching circuit. The red line illustrated the AC input signal, and the blue line illustrated the DC output after rectifier circuit. From this Figure it can be seen that the input voltage is 0.556 V and the output voltage is 2.705 V, while Figure 10, shows the results of simulation the rectifier circuit. The output is not exactly pure DC voltage; it is basically an AC signal with a DC offset voltage. It is clear after comparing results of Figures 9, 10 how is the matching circuit increased the output voltage, then better efficiency.

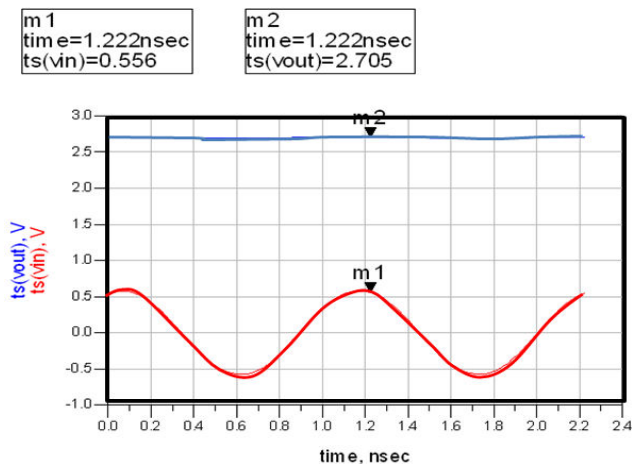


Figure-10. Simulation of three- stage voltage doubler circuit before adding matching circuit.

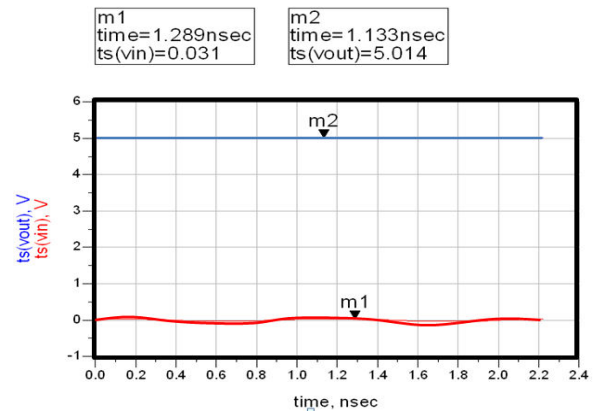


Figure-11. Simulation of three- stage voltage doubler circuit after adding matching circuit.

It is clear that from the rectifier circuit, each stage in voltage doubler circuit can be seen as a single battery with open circuit output voltage V_o , internal resistance R_o . With load resistance R_L , the output voltage, V_{out} is expressed as Equation. (11) [22].

$$V_{out} = \frac{V_o}{R_L + R_o} R_L \quad (11)$$

When n number of these circuits are put in series and connected to a load of R_L in Equation. (11) the output voltage V_{out} obtained is given by

$$V_{out} = \frac{nV_o}{nR_L + R_o} R_L = V_o \frac{1}{\frac{R_o}{R_L} + \frac{1}{n}} \quad (12)$$

The number of stages in the system has the greatest effect on the output voltage. The capacitors, affect the speed of the transient response and the stability of the output signal. The number of stages is essentially directly proportional to the amount of voltage obtained at the output of the system as shown in Figure-11. Figure-12 shows the prototyping of the rectifier first and second stage. The subsequent third stage and testing are under progress.

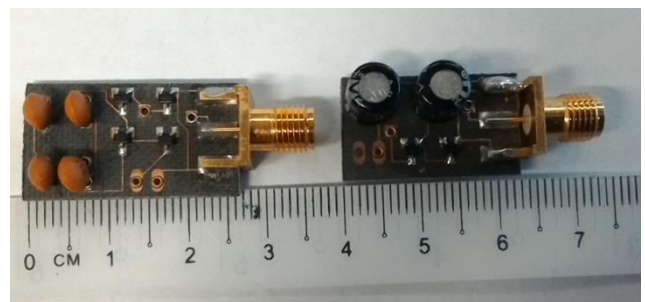


Figure-12. Prototyping of the rectifier circuit for first and second stage.



CONCLUSIONS

A 900 MHz RF energy harvesting system for charging mobile applications has been analyzed, discussed and designed. Lastly the energy conversion module that comprises of 3-stages voltage doubler circuit with zero bias Schottky diodes was successfully designed, implemented and found to be efficient in converting the RF signals captured by the antenna to the required DC output.

ACKNOWLEDGEMENT

The authors would like to thank Universiti Teknologi PETRONAS's Mission Oriented Research under Hybrid Energy System (HES) for giving the financial support to publish this work.

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