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# DESIGN OF MODIFIED EXPLICIT PULSE DATA-CLOSE-TO-OUTPUT FLIP-FLOP

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**ABSTRACT**

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in- first out. In this paper we proposed a low power consumed and less area pulse triggered flip-flop. This design uses 23 transistors this reduces the area complexity by 3 transistors comparing with existing ep-DCO. The new flip-flop can save up to 74% of the energy with the same speed as that for the existing ep-DCO and can save up to 69% of the energy with the same speed as that for the CDFF.

**Keywords:** pulse generator, flip flop, DCO, SEPFF.

## 1. INTRODUCTION

In the past decades, Moore's law drives the VLSI technology to continuously increase the transistor densities, there are hundreds millions of transistors on a chip today, which results in that the power consumption of VLSI chip has constantly been increasing. Although the capacitances and the power supply scale down meanwhile, the power consumption of the VLSI chip is still increasing continuously. In any synchronous system, Flip-Flop plays important role. They are not only responsible for the correct timing, functionality and performance of the chip, but also they and other clock distribution networks consume a significant portion of the total power of the circuit. It is estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%-45% of the total system power [1]. Comparing to different elements in the VLSI circuits, flip-flops are the primary source of the power consumption in synchronous system. Moreover, flip-flops have a large impact on circuit speed. The performance of the Flip-Flop is an important element to determine the performance of the whole circuit. For example, the Clock-to-Q delay, Setup time and Hold time, all these parameters of the flip-flops can affect the performance of the whole circuit. Therefore, the studies on Flip-Flop become more and more in recent years. With the increasing of the transistor densities and the technology scaling, the circuits are more and more sensitive to the externally induced phenomena, which we usually called soft-error. Due to the lower Vdd and the smaller node capacitance, the amount of charge stored on a circuit node is becoming increasingly smaller, the result of this is that the circuits have become more susceptible to spurious voltage variations caused by externally induced phenomena, the occurrence of this kind of faults will affect the integrity of the data, and the flip-flop will cause malfunction. In industry, the cost for avoiding the transient faults is significant every year. So how to design a circuit which can have a high soft-error tolerance is very popular today.

Power consumption and timing delays are the two important design parameters in high speed VLSI systems. In many digital very large scale integration (VLSI) designs, the clock system that includes clock distribution network and flip-flops is one of the most power consumption components. It accounts for 30% to 60% of the total system power, where 90% of which is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop [1], As clock frequency increases, the latency of the flip-flop or latch will play an even greater role in the overall cycle time. A Flip-Flop that synchronizes the state changes during a clock pulse transition is the edge-triggered flip-flop. When the clock pulse input exceeds a specific threshold level, the inputs are locked out and the flip-flop is not affected by further changes in the inputs until the clock pulse returns to 0 and another pulse occurs. As the clock frequency increase, pulse-triggered flip-flop tends to be popular as compared to conventional master-slave flip-flops. Because they employ time borrowing across cycle boundaries which results in zero or negative setup time. Moreover, the number of transistors we used in the pulse-triggered flip-flop is less than the number we used in the conventional master-slave flip-flops, so the simple structure of the pulse-triggered flip-flop leads to a better power efficiency. In recent years, there has been an increasing demand for high-speed digital circuits at low power consumption. Because the clock frequency is determined by system specifications, the clock signal is constantly active, it makes timing components (latches and

flip-flops) the most power consuming components in the VLSI system [2]. Like the single-edge triggered flip-flop, the output of the flip-flop will follow the input D at the edge of the clock, the difference is that the dual-edge triggered flip-flop will cause a transition on both the positive edge of the clock pulse and the negative edge of the clock pulse. On the rising edge of the clock and the falling edge of the clock, the output is given the value of the D input at that moment. The output can only change at the clock edge, and if the input changes at other times, the output will be unaffected. The used of dual edge-triggered flip-flops can help to reduce the clock frequency to half that of the single edge-triggered flip-flops while maintaining the same data throughput [3]. In other words, the dual-edge triggered flip-flop requires a lower clock frequency than the single-edge triggered flip-flop to achieve comparable performance [4-8]. Therefore, the dual edge triggered flip flop offers the same data throughput of single edge-trigger flip-flops at half of the clock frequency, this thereafter translates to better performance in terms of both power dissipation and speed.

A fundamentally different approach for constructing a FF uses pulse signals. The idea is to construct a short pulse around the rising (or falling) edge of the clock. This pulse acts as the clock input to a latch, sampling the input in a short window. The combination of a pulse-generation circuitry and a latch results in a positive edge triggered register. Pulse triggered FF's reduce the number of latch stages into a single stage. The logic complexity and number of stages are reduced in these pulse triggered FF's leading lesser D-to-Q delays. The main advantage of these pulse triggered FF's is that they allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Due to these advantages P-FF's has been considered a popular alternative for traditional master slave FF.

## 2. IMPLICIT PULSED DATA CLOSE TO OUTPUT

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. A state-of-the-art P-FF design, named ip-DCO, is given in Figure-1 [11]. It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, NMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X. controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

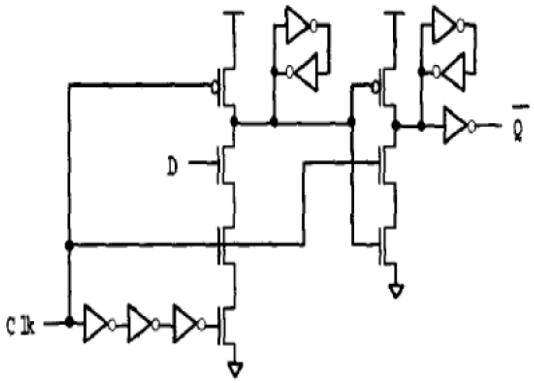


**Figure-1.** ip-DCO.

## 3. STATIC EXPLICIT PULSE TRIGGERED FLIP FLOP

Dynamic CMOS is recommended for high performance gates with large fan-ins. However, for small fan-in circuits in particular, dynamic logic does not provide area or performance advantage over static logic. The main structure of the SEPFF shown in Figure-2 [8] features two cascaded static latches. The internal node X follows the input D during the transparent interval. At the rising edge, N3 and N4 turn on for the short transparency duration, causing the input D to propagate to the output. The keeper maintains the output state. During the transparency period, when input D is stable high, X goes low, causing Q to go high. Node X remains low as long as D is high. The NMOS transistor driven by X is placed near the output Q. The number of clocked transistors in this flip flop are 3.

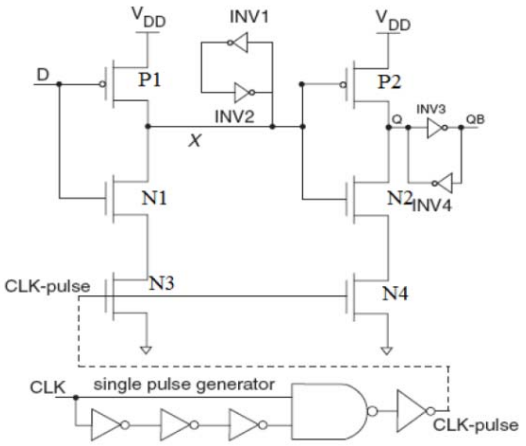


**Figure-2.** Static Explicit Pulse Triggered Flip Flop [SEPFF].

## 4. EXPLICIT-PULSE DATA-CLOSE-TO-OUTPUT FLIP-FLOP [9]

Figure-3 show the schematic of the Explicit-Pulse Data-Close-to-Output flip-flop (ep-DCO) which is considered as one of the fastest flip-flops due to its semi-dynamic nature [9]. Figure-1 is the pulse generator of the Explicit-Pulse Data-Close-to-Output flip-flop. It uses the delay of three inverters to generate the pulse at the double edge of the clock. In the ep-DCO, there are two stages, the first stage is dynamic and the second stage is static. The clock pulse drives three transistors-M1, M3 and M5. The input data is connected to M2 and the circuit captures the data through M2. When the flip-flop is transparent, the input data propagates to the output, after the transparent period, M3 and M5 will turn off because of the low voltage of the pulse, at the same time, point X change to the high voltage because that M1 is on at this time. So M4 is off after the transparent period. Hence, any change at the input cannot be passed to the output. Now, we begin to analyze the disadvantages of Explicit-Pulse Data-Close-to-Output flip-flop. The internal node X will be charged or discharged at every clock cycle especially when the input data does not change, a lot of power is consumed at this point. Moreover, while the output is high, the repeated charging/discharging of node X in each clock cycle causes glitches to appear at the output. These glitches propagate to the driven gates not only to increase their switching power consumption but also to cause noise problems that may lead to system malfunctioning [10].

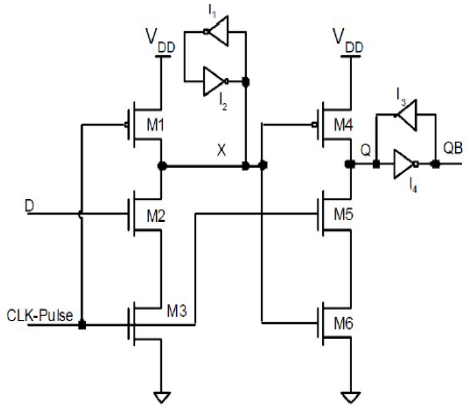


**Figure-3.** Explicit-Pulse Data-Close-to-Output flip-flop (ep- DCO).

## 5. PROPOSED FIVE INVERTER PULSE GENERATOR CIRCUIT

We proposed a pulse generator with pass transistor logic. The most commonly used method is to use the inverter to generate the clock delay and use this little difference of the clock to generate the pulse. This pulse generator has improved two disadvantages of the pulse generator in the [22]. The first improvement is that this pulse generator can produce narrower pulse at both the rising edge of the clock; this can help the flip-flop reduce the setup time and hold time effectively. The second improvement is that this pulse generator can produce a pulse which can get near to the Vdd. Now we begin to analyze this pulse generator and discuss how it works. The basic idea for pulse generation is AND operation of clock and delayed inverted clock. This will produce a small pulse for every rising edge of the clock. The symmetric inverters are designed using 180um technology and simulations are analyzed using Tspice EDA tool. The Figure-4 shows the proposed pulse generator circuit. The proposed puce generator circuit uses only 11 transistors instead of 12 transistor design in [9]. The one transistor can be reduced by the AND gate design using pass transistor logic.

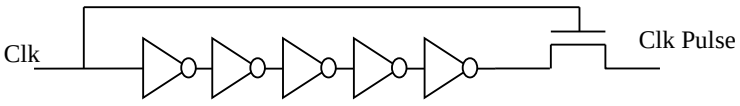


**Figure-4.** Proposed clock pulse generation.

## 6. PROPOSED MODIFIED EXPLICIT-PULSE DATA-CLOSE-TO-OUTPUT FLIP-FLOP

The disadvantages of Explicit-Pulse Data-Close-to-Output flip-flop [9] is the internal node X will be charged or discharged at every clock cycle especially when the input data does not change, a lot of power is consumed at this point. Moreover, while the output is high, the repeated charging/discharging of node X in each clock cycle causes glitches to appear at the output. These glitches propagate to the driven gates not only to increase their switching power consumption but also to cause noise problems that may lead to system malfunctioning [10].

This problem is removed in our proposed Explicit-Pulse Data-Close-to-Output flip-flop (Mep- DCO).Fig. shows the schematic of the modified Explicit-Pulse Data-Close-to-Output flip-flop (Mep- DCO) Figure-4 is the pulse generator of the modified Explicit-Pulse Data-Close-to-Output flip-flop. It uses the delay of five inverters to generate the pulse. In the Mep-DCO, there are two stages, the first stage is dynamic and the second stage is static. The clock pulse drives three transistors-M1, M3 and M5. The input data is connected to M2 and the circuit captures the data through M2. When the flip-flop is transparent, the input data propagates to the output, after the transparent period, M3 and M5 will turn off because of the low voltage of the pulse, at the same time, point X change to the high voltage because that M1 is on at this time. So M4 is off after the transparent period. Hence, any change at the input cannot be passed to the output. The contribution of X node back to back connected inverter in the result is very low. So this couple of inverter is removed. The drawback of glitches in the ep-DCO is reduced by adding a inverter in the output. The number of gate count for designing this proposed flip flop is 23. Figure-5 shows Proposed Modified Explicit-Pulse Data-Close-to-Output Flip flop.

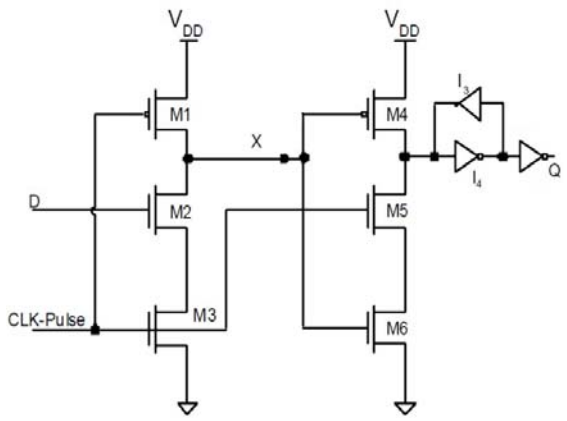


**Figure-5.** Proposed Modified Explicit-Pulse Data-Close-to-Output Flip-Flop.

## 7. SIMULATION RESULTS AND DISCUSSIONS

The simulation results for proposed flip-flop were obtained in a 0.18 CMOS technology at room temperature using TSPICE, the supply voltage is 1.8 V. In order to obtain occurate results, we have simulated the circuits in a real environment, which dictates that the flip-flops' inputs (clock, data) are driven by fixed input buffers, and the outputs are required to drive an output load. The Figure-6 shows the simulation result of Modified Explicit-Pulse Data-Close-to-Output flip-flop without additional inverter in output. The simulation shows that there is a glitch for every clock pulse transition. The amplitude depth of glitch is comparatively very less (0.3 volts). So this may used to drive any circuit inputs.

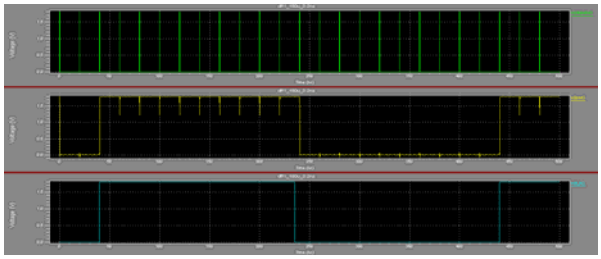

**Figure-6.** The simulation result of modified Ep DCO without back to back connected inverters at X node.

The Figure-7 shows the simulation result taken for measuring the clock to out delay. The proposed Modified Explicit-Pulse Data-Close-to-Output gives the clock to Q delay is 120.45 ps. This delay is very less Comparing to the existing EpDCO flipflop.

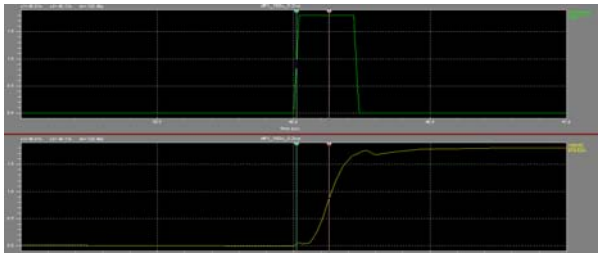

**Figure-7.** The simulation result of clock to q delay of modified Ep DCO.

Figure-8 shows the simulation result taken for measuring the D to out delay. The proposed Modified Explicit-Pulse Data-Close-to-Output gives the D to Q delay is 124.65 ps.

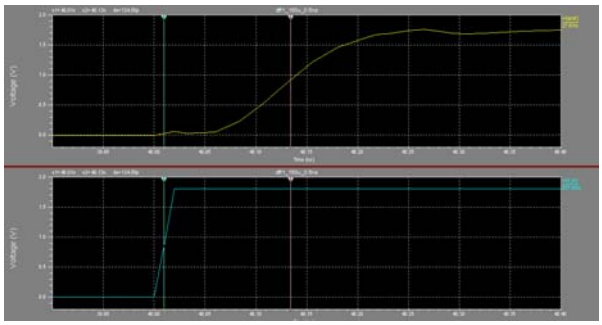

**Figure-8.** The simulation result of clock to Q delay of modified Ep DCO.

Figure-9 shows the simulation result glitch free output taken from Modified Explicit-Pulse Data-Close-to-Output flip-flop with additional inverter at output.

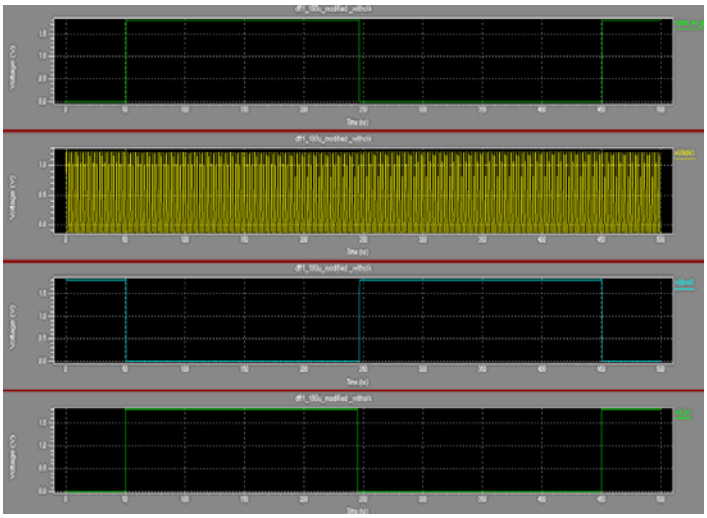

**Figure-9.** The simulation result of modified Ep DCO with additional inverter at output.

Table-1 shows the comparison chart for existing EP DCO and proposed EP DCO. From the table the power delay product of proposed design is 1.1 fJ.

**Table-1.** Comparing the flip-flop characteristics against 4 other flip-flops in terms of delay, power, and power delay product.

| **Type** | **No. of transistors** | **No of clocked transistors** | **DQ delay** (ps) | **Power** (uw) | **PDP** (fJ) |
|---|---|---|---|---|---|
| CCFF[18] | 26 | 13 | 206 | 22.6 | 4.66 |
| CPFF[14] | 23 | 12 | 189.2 | 22.4 | 4.24 |
| CDFF[12] | 28 | 15 | 185 | 20.2 | 3.74 |
| Ep-DCO[11] | 26 | 15 | 184 | 24.4 | 4.49 |
| Mep-DCO[proposed] | 23 | 14 | 124.5 | 8.85 | 1.10 |

## 8. CONCLUSIONS

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and Master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power Consumption of the clock tree system. In this paper we proposed a low power consumed and less area pulse triggered flipflop. This design reduces the area complexity by 11% comparing with existing ep-DCO. The new flip-flop can save up to 74% of the energy with the same speed as that for the existing ep-DCO and can save up to 69% of the energy with the same speed as that for the CDFF.

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