



DESIGN AND ANALYSIS OF INTERLEAVED NON-INVERTING BUCK BOOST CONVERTER FOR PV MODULE

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ABSTRACT

With the increasing focus on renewable energy especially solar energy, there is an ever increasing demand for cost effective and more efficient buck boost converters. This study presents the analysis and control design techniques for a Non Inverting Buck Boost Converter with Interleaved technique. The converter has been then integrated with a Photo-Voltaic (PV) module with varying output voltage to give fixed 24V DC converter output. The performance of the specified buck boost converter has been compared with conventional converters like Cuk and SEPIC converters.

Keywords: non inverting buck boost converter, interleaving technique, control.

1. INTRODUCTION

Global fossil fuel reserves are disappearing at alarming rates. Besides depleting fast, these conventional fuels also cause environmental pollution and global warming. This scenario has led us to consider renewable energy as a viable replacement for fulfilling our energy needs. Solar energy is the most abundant form of renewable energy and also the most feasible source of energy to meet the energy demands locally. But utilization of Solar energy comes with its own set of problems. The output voltage of PV panels is not fixed and can vary due to a number of reasons.

Shading is a major problem faced by the PV systems which tends to change the resistance of the solar cells and consequently the panel output voltage changes, which poses a serious control problem. Besides the change in output voltage yet another problem arises if just one of the cells is shaded because this results in an increase in resistance in that cell. The current from the other illuminated cells produces heat in this resistive cell which could irreparably damage it. To prevent this from happening, a bypass diode is placed in parallel with groups of cells. The output voltage of the PV panels also changes with the change in insolation levels.

Thus to provide a stable DC bus voltage, step-down and step-up DC/DC converters with proper control scheme are required. In this paper we have analyzed the performance and developed control strategies for a Non Inverting Buck Boost converter with interleaved technique [1]. This converter provides certain distinct advantages over the Conventional Buck Boost Converters. Due to its lesser number of switches and energy storage elements (inductors and capacitors), this converter is smaller in size, more efficient and causes significantly lesser switch stress when compared to conventional converters like Cuk and SEPIC.

A distinct feature of this converter is the use of interleaved technique which has the advantages of

reducing the filter inductance as well as the output ripple. It helps to improve upon the efficiency of the converter, improve the working characteristics without transitioning the operating modes and also helps simplify the control logic [2].

In order to obtain constant output voltage of 24 V the switches have to be triggered for specific time intervals depending on the input voltage which can vary between 20 - 30 V DC. An open loop control scheme has been developed in order to dynamically calculate the duty cycle for the switches and generate PWM pulses according to the changing input voltage.

The original converter [1] was designed to give a fixed DC output voltage of 28V but due to its limited applications, a control scheme was developed in order to get 24V DC output which has widespread applications such as in construction, railways, vehicles, commercial and marine vessels, military and defense equipments and forestry and agricultural applications.

2. INTERLEAVING TECHNIQUE

As has already been discussed interleaving technique helps in providing a significant improvement in the performance of the buck boost converter. In Figure-1 a simple boost converter which does not employ the interleaving technique has been shown. Here the output capacitor ripple current is very high I_{cout} . I_{cout} is actually the difference of the inductor current I_1 and the output DC current, I_{out} . Figure-2 presents the functional circuit diagram of a buck boost converter employing the interleaving technique.

It consists of two converters which are operating 180° out of phase with each other. The input current is consequently the sum of the currents of the two inductors I_{11} and I_{12} which helps in cancelling out each other's current ripple being out of phase with each other.

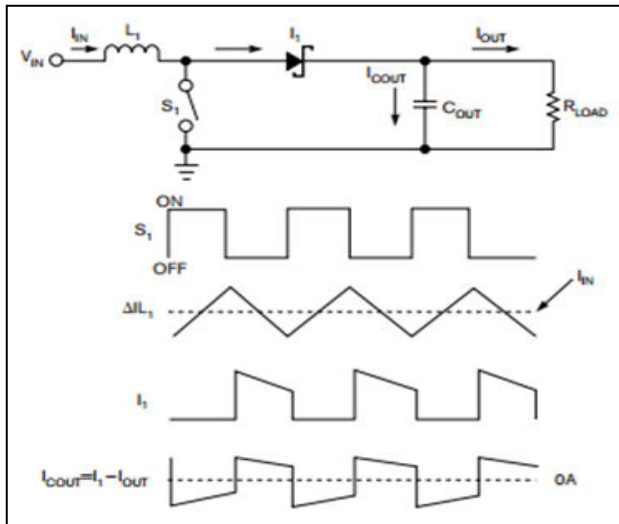


Figure-1. Boost converter without interleaving technique.

The output current i.e., I_{OUT} is then the sum of the two diode currents from which the DC-output current is then subtracted which thus helps in reducing the ripple in the output current.

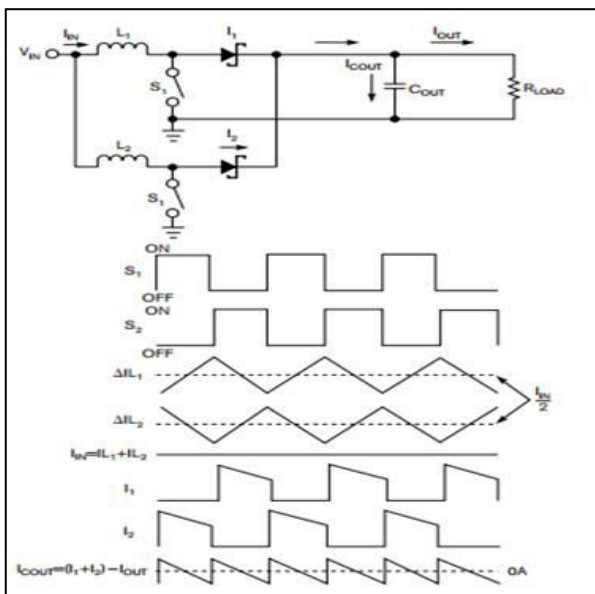


Figure-2. Boost converter using interleaving technique.

3. CONTROL TECHNIQUES

A. Operation principle

The circuit diagram of the Non Inverting Buck Boost converter has been shown in Figure-3. The circuit consists of 3 switches and 3 diodes along with two inductors and one output capacitor.

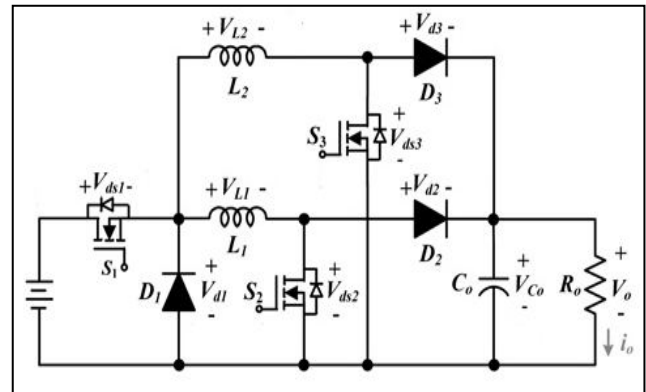


Figure-3. Non inverting buck boost interleaved converter [1].

The converter operates in four different modes [1] each of which has a different set of switches operating at a time. The triggering pulses to the switches can be determined by the switching sequence of the circuit as shown in Table-1.

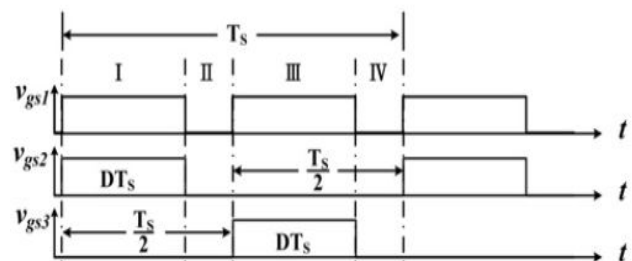


Figure-4. Switching sequence in one switching period. [1]

Upon doing the Steady State analysis the DC Voltage and Current gain of the Buck Boost converter can be found by the following relations.

$$\frac{V_o}{V_{in}} = \frac{2D}{1-D} \quad (1)$$

$$\frac{I_o}{I_{in}} = \frac{1-D}{2D} \quad (2)$$

Where V_o and V_{in} are converter Output and Input Voltages respectively whereas I_o and I_{in} are converter output and input currents respectively, and D is the Duty cycle.

To improve the efficiency of the converter, the topology can be modified where the diodes D_1 , D_2 and D_3 are replaced by switches S_4 , S_5 and S_6 respectively. This technique is called Synchronous Rectifier (SR) Technique. This technique helps in reducing the diode conduction losses but introduces some additional switching losses; however the overall converter efficiency increases. It also removes the problem of high frequency ringing. [1]



B. Switching table

Table-1. Switching patterns in different modes.

Modes -> Switch	I	II	III	IV
S1	ON	OFF	ON	OFF
S2	ON	OFF	OFF	OFF
S3	OFF	OFF	ON	OFF
S4	OFF	ON	OFF	ON
S5	OFF	ON	ON	ON
S6	ON	ON	OFF	ON

The switching frequency of S_1 is twice that of S_2 and S_3 .

C. Open loop control technique

The Duty Cycle for switches S_2 and S_3 can be calculated from the Output Voltage expression mentioned in equation (1). The duty cycle for S_1 will be twice that of S_2 and S_3 .

$$D = \frac{V_o}{V_o + 2V_{in}} \quad (3)$$

For calculating the duty cycle in order to achieve constant DC output voltage, V_o is kept constant at 24V. The value of the duty cycle will change according to the dynamically changing input voltage as generated by the PV panel.

The Duty cycle is fed to the pulse generation circuit and gate pulses corresponding to fixed 24V DC output are generated.

D. MATLAB/SIMULINK implementation of pulse Generation

In1 is the duty cycle of switches S_2 and S_3 which is being calculated dynamically with changing input voltage and fed to the Pulse generation logic circuit. The duty cycle is multiplied by 2 in order to get the duty cycle for switch 1. As the switching frequency of S_1 is twice that of S_2 and S_3 , the repeating sequence which acts as the reference signal for S_1 is also twice in frequency when compared to reference signal for S_2 and S_3 . The frequency of the reference signal for S_2 and S_3 is also the operating frequency of the converter.

To generate the pulses for S_1 "a greater than or equal to" operation is applied between the reference signal which is a Saw tooth waveform and a constant DC voltage equal in magnitude to the duty cycle for that switch.

Similarly for the pulses of switch S_2 the same operation as above is applied to the Saw tooth reference signal and the duty cycle for that switch.

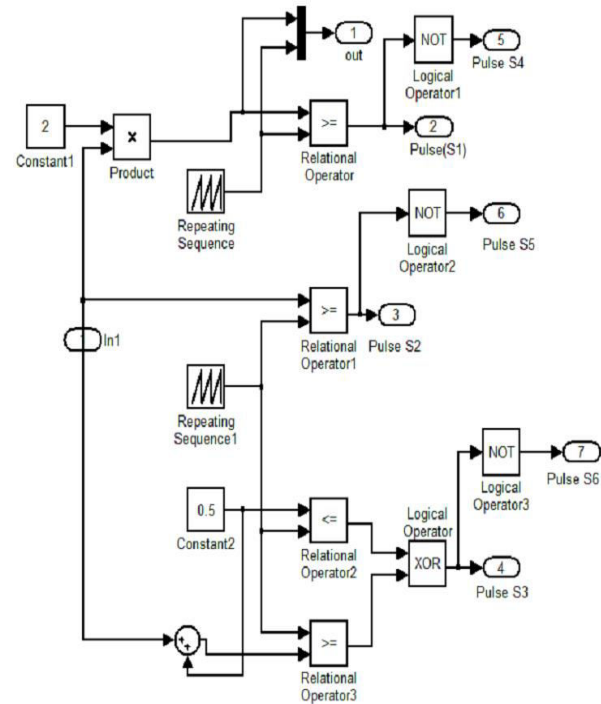


Figure-5. Pulse generation control logic.

From Figure-4 we can observe that the pulses for S_3 are shifted in phase by 180° to that of S_2 . 180° phase difference corresponds to duty cycle $D = 0.5$ which is thus added to the duty cycle for switch S_3 .

Using relational operators the time period for mode II and IV are calculated first which when added to time period of mode I give us the time for which S_3 is off in one switching period. The Gate pulse for S_3 can be obtained by applying XOR gate to the pulses covering time periods of modes (I + II) and IV as shown in Figure-6.

The Gate pulses for S_4 , S_5 and S_6 can be obtained by applying NOT gate after gate pulses for S_1 , S_2 and S_3 respectively. Figure-6 shows the pulses obtained after implementing the above described control circuit in SIMULINK software.

For hardware implementation of the Buck Boost converter, these pulses can be easily generated using dSPACE®. Together with dSPACE's real-time interface Simulink Coder provides a flawless transition from the Simulink model to real-time hardware.

Alternatively, the pulses can also be generated for real time applications using NI LABVIEW®

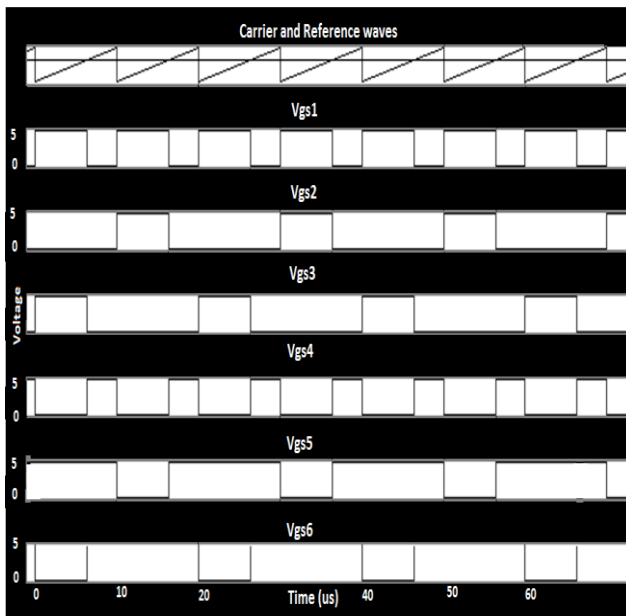


Figure-6. Gate pulses for all switches in sr technique implementation.

E. LABVIEW virtual interface for generating pulses

LABVIEW provides certain advantages over other software when dealing with real time hardware applications. Acquiring data (analog and digital) and generating signals for dynamic applications is comparatively simple.

Similar to the Simulink model of pulse generation a LABVIEW VI was developed. The duty cycle calculated using equation (3) was then given to the signal generators to generate the pulses of specified frequency.

By continuously acquiring the analog input voltage through the Data Acquisition unit (DAQ) and dynamically calculating the duty cycle the generated pulses can be obtained on the analog output terminals of the DAQ units for actual hardware applications.

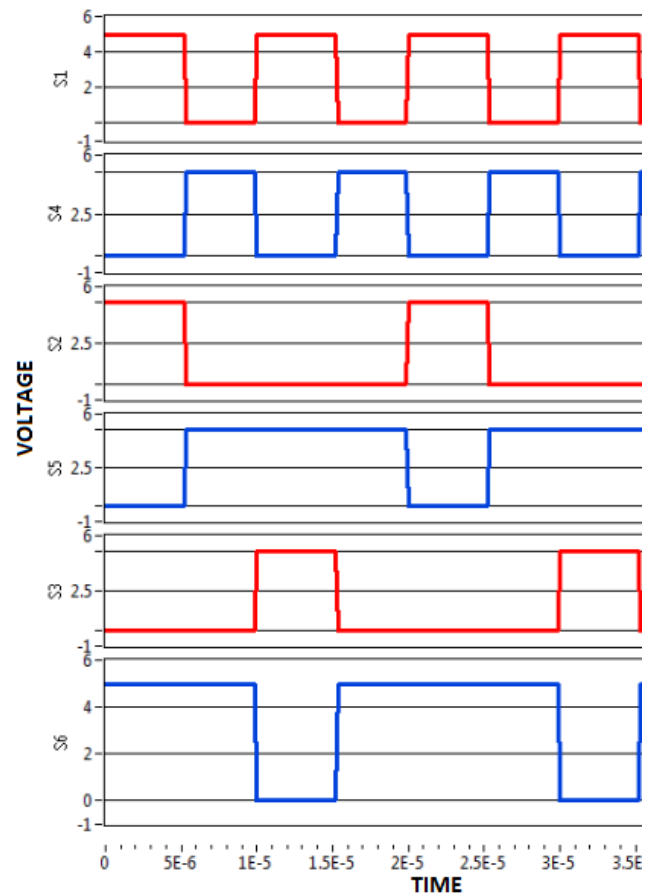


Figure-7. The pulses obtained using the LABVIEW VI.

Figure-8 shows the logic mentioned above implemented in a VI to generate real time pulses using LABVIEW. Input voltage V_{in} was acquired using DAQ through a voltage divider circuit to protect the DAQ unit from overvoltage. The acquired voltage was then multiplied by a factor of 5 (varies according to the potential divider circuit) in order to obtain the original voltage V_{in} . The factor of 100 is used to convert duty cycle into percentage value while factor of 200 was used to double the duty cycle for switches S_1 and S_4 .

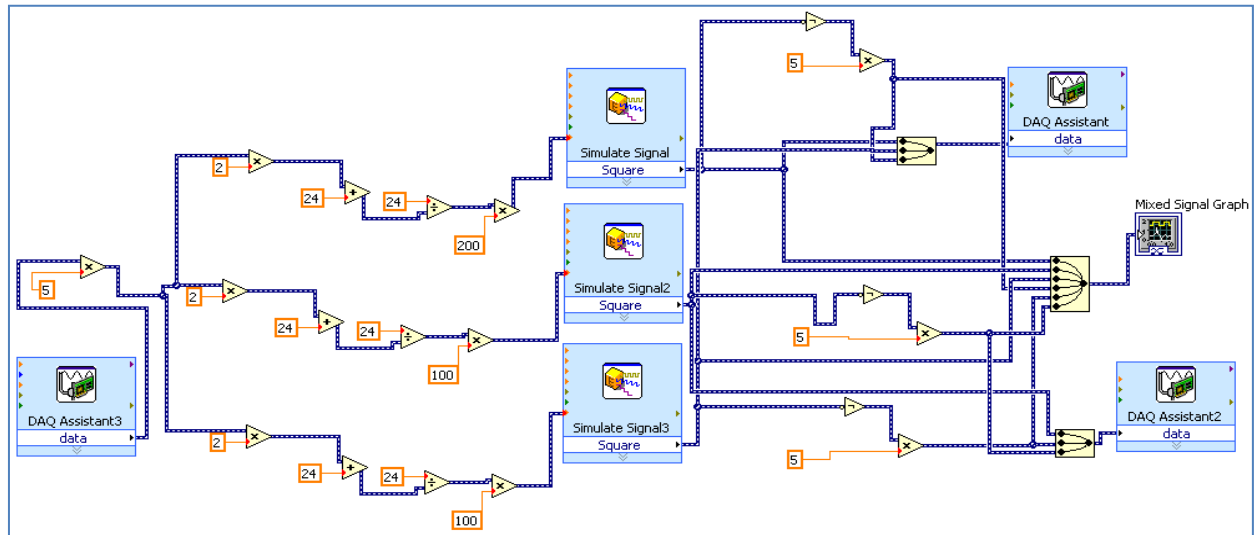


Figure-8. LABVIEW® VI for generating pulses.

4. MATLAB/SIMULINK MODEL OF BUCK BOOST CONVERTER WITH PV MODULE

The SR technique circuit of the Non Inverting Buck Boost converter was implemented in SIMULINK

and a PV module [3] was used as the DC input source. The input voltage was varied by changing the insolation input to the PV panel which was then used to calculate the corresponding duty cycle using equation (3).

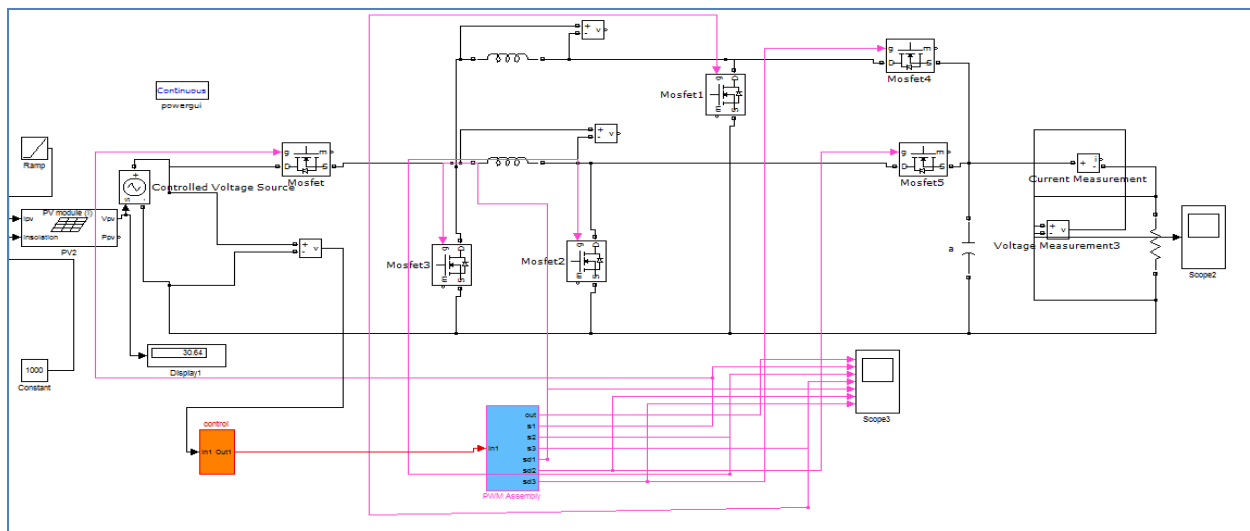


Figure-9. SIMULINK model of buck boost converter integrated with PV module.

The duty cycle was then given to the PWM assembly as explained in III.D to generate the pulses to get the desired output of 24V. The circuit and output waveforms are shown in Figure-9 and Figure-12 respectively.

5. COMPARISON WITH CONVENTIONAL BUCK BOOST CONVERTERS

Switch stress is a major concern while choosing the switches to be used in a converter. The greater the

voltage stress exerted on a switch the higher will be its required rating. A higher rated switch would not only be more costly but also bulkier and consequently the converter would become more cumbersome. The Non-Inverting Buck Boost converter discussed considerably reduces the switch stress when compared with Cuk and SEPIC converters. The following sub sections compare the voltage stress on the switches for identical output (24V) and input (20V) conditions.



A. Switch stress waveforms for non inverting buck boost converter

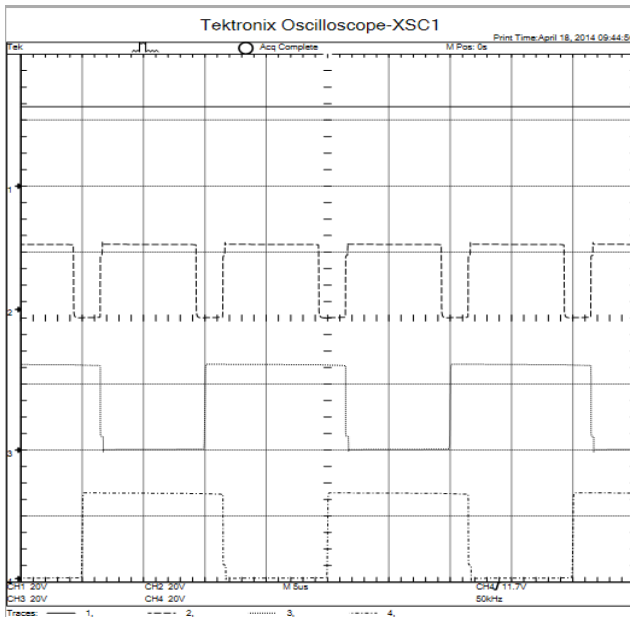


Figure-10. Output voltage and switch stresses for S1, S2 and S3 respectively.

In this section the performance of the Non-inverting Buck Boost Converter has been compared with conventional converters, by comparing their respective switch stresses. The percentage ripple in the output voltage of the Non Inverting Buck Boost converter with interleaved technique was found to be less than 0.5%. The switch stress on different switches is given in following equations.

$$V_{ds1, \max} = V_{ds4, \max} = V_{in, \max} \quad (4)$$

$$V_{ds2, \max} = V_{ds3, \max} = V_o \quad (5)$$

$$V_{ds5, \max} = V_{ds6, \max} = -V_o \quad (6)$$

Figure-10 shows switch stresses across S1, S2 and S3 along with the output DC voltage of 24V. It can be seen that the stresses comply with the relations mentioned in equations (4) and (5).

Figure-10 shows the output voltage of 24V DC in channel 1. Channel 2 shows switch stress across S₁ which is equal to V_{in} (20V) as given in eq. (4). Channel 3 and 4 show the switch stress across S₂ and S₃ respectively which are both equal to V_o (24V) as mentioned in eq.(5)

B. Switch stress waveforms for cuk converter.

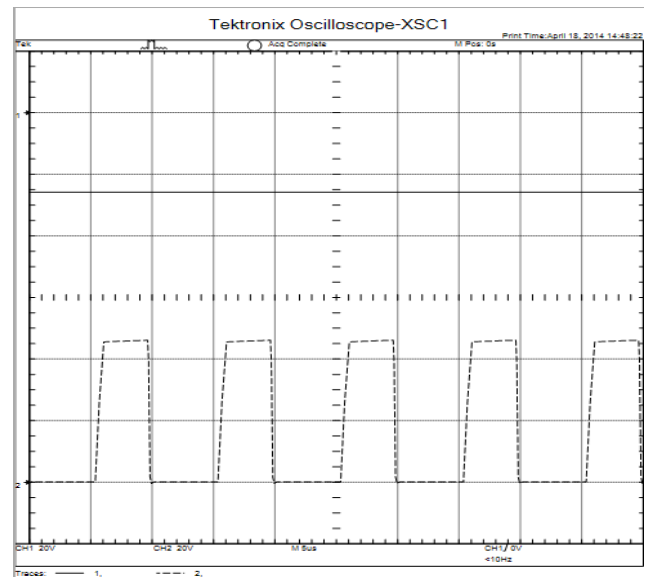


Figure-11. Output voltage and switch stress for cuk converter.

Figure-11 shows the output voltage and Switch stress for conventional CUK converter. As shown, for the same output voltage of -24V DC (Channel 1) the stress across the switch is equal to $2V_o = 48V$ (Channel 2) which is comparatively much higher than the switch stress for Non Inverting Buck Boost Converter. Also the output voltage of Cuk converter is inverting in nature which is rectified in the Non Inverting Buck Boost converter.

C. Switch stress and output waveform for SEPIC converter

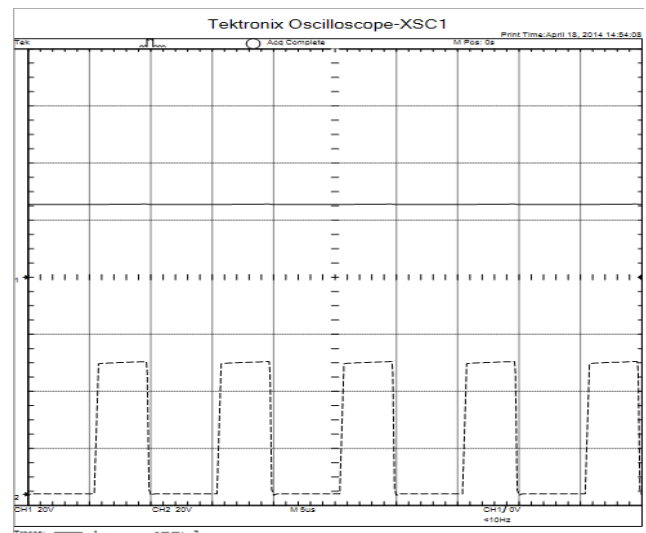


Figure-12. Output voltage and switch stress for sepic converter.



Figure-12 shows the Output Voltage in channel 1 of 24V DC and the switch stress in channel 2. As shown in the figure, the switch stress is equal to a very high value of 48V DC. Although SEPIC converter solves the problem of inverting output as seen in Cuk and other conventional converters, the voltage stress across the switch is still very high when compared to the Non Inverting Buck Boost converter.

6. CONCLUSIONS

The Non Inverting Buck Boost Converter with interleaved technique was designed to achieve low output current ripple and high power. In this paper several control techniques are presented to achieve a constant DC output voltage of 24V using the varying DC output of the PV panel as the input to the converter. A MATLAB/SIMULINK model of the given Non Inverting Buck Boost Converter with Interleaved Technique, integrated with a PV panel is presented. The control technique implemented in the model successfully maintained the output voltage of the converter constant at 24V with changing input DC voltage fed by the PV model with different insolation values. The switch stresses in the Non Inverting Buck Boost Converter were found to be considerably lesser than conventional converters like Cuk and SEPIC thus leading to decreased cost and size and increased durability and longevity.

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