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# SINGLE PHASE THIRTEEN LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES USING DIFFERENT MODULATION TECHNIQUES

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**ABSTRACT**

The main objective of proposal of this topology is to get the output with reduced Harmonics and to improve the efficiency with reduced number of switches. Multi-Level Inverter (MLI) Performance has been evaluated for three different modulation technique Trapezoidal pulse width modulation (TPWM), Sinusoidal Pulse width modulation (SPWM), $1/6^{th}$ Third order Harmonic injection technique ($1/6^{th}$ THIPWM). The parameters Total Harmonic distortion (THD), Efficiency, power utilisation is compared for all three techniques using MATLAB/Simulink and to identify the best suitable modulation technique.

**Keyword:** THD, inverter, voltage stress, conduction loss.

## 1. INTRODUCTION

In an ideal power system, the voltage supplied to customer equipment, and the resulting load current is perfect sine waves. However in reality, the conditions are never ideal, so these waveforms are often quite distorted. This deviation from perfect sinusoidal is usually expressed in terms of harmonic distortion of the voltage and current waveforms. Power system harmonic distortion is not a new phenomenon. Efforts to limit THD proportions are always been a challenge for power engineers. The biggest disadvantage in the conventional H-bridge inverter is that the output voltage will have desirable harmonics and the output wave is not sinusoidal. This will leads to generation of excess heat due to which the efficiency will be reduced and also in a long run it may damage the insulation level of the equipment.

In general, multilevel inverters are effective means of reducing harmonic distortion and dv/dt stress of the output voltages, which makes this technology suitable to utility interface and drives

MLI is used in high power applications due to their advantages of reduced Harmonics, less Electromagnetic interference.

Multilevel inverter topologies can be divided into three categories.

a) Diode clamped [9]

b) Flying capacitor [2]

c) H-bridge cascade [6]

In many high power applications these inverters have been playing an important role. However they also have considerable disadvantages. In a diode clamp MLI, the design is complicated if the levels are increased more than three, also there is an issue in maintaining charge in the capacitor and there will be considerable voltage drop if series of diodes are used .The drawbacks are well described in [5, 7]. Even in case of flying capacitor MLI maintaining capacitor voltage is an issue [7]. In the case of CMLI we can get the desired output i.e. boosted output voltage with reduced THD [6]. However separate DC sources are required for each module and number of switches will be more due to which switching losses will be more.

In recent years, numerous new multilevel inverter topologies have been developed to overcome the disadvantages of traditional inverters mentioned above.

To overcome the problem of CMLI a new sub multilevel inverter topology has been developed [12]. These sub multilevel inverters are classified as symmetric and Asymmetric based on the amplitude of DC sources. In symmetric topology the voltage of all the DC source will be equal, However in the Asymmetric topology the required output voltage levels are increased by selecting the different voltage levels of DC sources.

The sub multilevel inverter requires n number of DC sources. To overcome these drawbacks nowadays, many MLIs topologies have been developed. In order to generate more stepped voltage output and also to enhance the quality of waveforms, more isolated dc power supplies should be envisaged in the circuit. This will result to more cost and less flexibility of system. One of the suitable solutions is to provide the virtual dc sources i.e. to use the capacitors. However, in this case, to prevent the discharging problem, the charge balancing control circuits for capacitors are needed which make more complexity and less reliability. This restriction for capacitors leads to introduce the switched capacitor multilevel inverter [13]. However number of switches is more which will lead to increase in losses, complex in circuit and more expensive.

Subsequently a topology with reduced number of switches has been developed. The operation of switched capacitor 11level Inverter is elaborated in [1]. In Continuation to that we propose for the increase in levels by two to make the MLI more efficient.

In this 13level proposed topology analysis has been carried out with different modulation technique like TPWM, SPWM, and THIPWM.

## 2. OPERATION OF PROPOSED 13LEVEL SWITCHED CAPACITOR MLI

In the proposed topology there will be a single DC voltage source and the output voltage is increased by almost six times based on the Switched capacitor cells which are connected in cascade as shown in the fig. and this is called as DC-DC conversion section.

The input voltage $V_{in}$ shall be 24V DC, all the capacitors $C_1$ to $C_5$ are charged by the input power source $V_{in}$ though diodes $D_i$ and $D_i'$ (i=1, 2,…5) when the switch $Q_0$ is turned ON and the other switches $Q_1$ to $Q_5$ is kept OFF, In the H-bridge, only the switch $S_1$ is turned ON and the others are in OFF. During this time there is no voltage and the output voltage shall be equal to zero. One more zero level is achieved by turning ON $S_2$ when other switches are OFF.

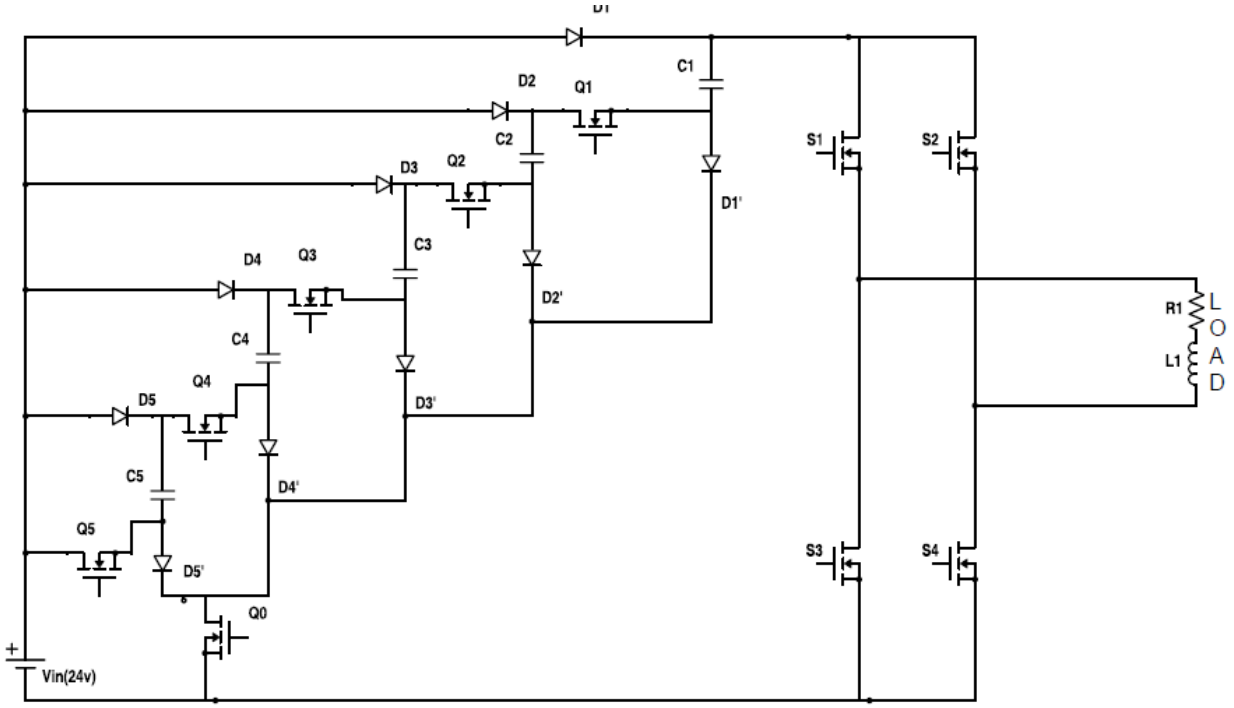


**Figure-1.** Proposed switched capacitor MLI.

The operating state is that $Q_0$ will be in ON condition while other switches are in OFF condition. The voltages across capacitors $C_1$ to $C_5$ are almost equal to the input voltage $V_{in}$. In the H-bridge, switches $S_1$ and $S_4$ are turned ON simultaneously whereas $S_2$ and $S_3$ maintain OFF state. Similarly, the level of $-V_{in}$ can be developed by turning ON switches $S_2$ and $S_3$ whereas $S_1$ and $S_4$ are OFF.

When the switch $Q_0$ is turned OFF, the voltage level $i \times V_{in}$ is developed in the DC-DC conversion section by turning ON switches $Q_1$ to $Q_{i-1.}$ (i=2, 3, …, 5) whereas $Q_i$ to $Q_5$ are OFF. In this case, the capacitors $C_1$ to $C_5$ are connected in series with the input source $V_{in}$ and the total voltage level Produced is represented as

$$V_{out}=V_{in}+V_{C1}+V_{C2}+\ldots\ldots+V_{C5} \quad (1)$$

Assuming that the voltages across all capacitors are the same as the input voltage $V_{in}$. Then the total voltage level will be $6 \times V_{in}$. By operating the full bridge, turning ON $S_1$ and $S_4$ keeping $S_2$ and $S_3$ in OFF, the voltage will be developed at the load. The level of $-6 \times V_{in}$ will be developed at the load by operating the full bridge in opposite manner.

**Table-1.** Switching sequence of proposed topology.

| Time interval | S1 | S2 | S3 | S4 | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 3 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 4 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 5 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 6 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 7 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 10 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 11 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 12 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 13 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 14 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 15 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 16 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 17 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 18 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 19 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 20 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 21 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 22 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 23 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 24 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 25 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 26 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

## 3. MODULATION TECHNIQUE

The general opinion of a multilevel power converter is that the large number of switches which may lead to complex pulse-width modulation (PWM) switching logics. However, in recent days many modulation techniques were developed to make the logics simple.

The switching sequence for the proposed topology can be achieved by using different modulation technique. Modulation techniques can be classified based on the carrier frequency and also based on the modulating signal.

Based on frequency it can be subdivided into i) High Frequency modulation(HFM) ii) Fundamental frequency modulation (FFM). Based on the topology proposed in [1] FFM is more efficient than the HFM. Hence we have considered FFM in our case analysis with three modulations as listed below and the results were compared.

a) Sinusoidal PWM technique

b) Trapezoidal PWM technique

c) $1/6^{th}$ Third Harmonic injection PWM technique.

In these above techniques DC reference signals are used to generate the pule output for the each switch.

### A. Sinusoidal PWM

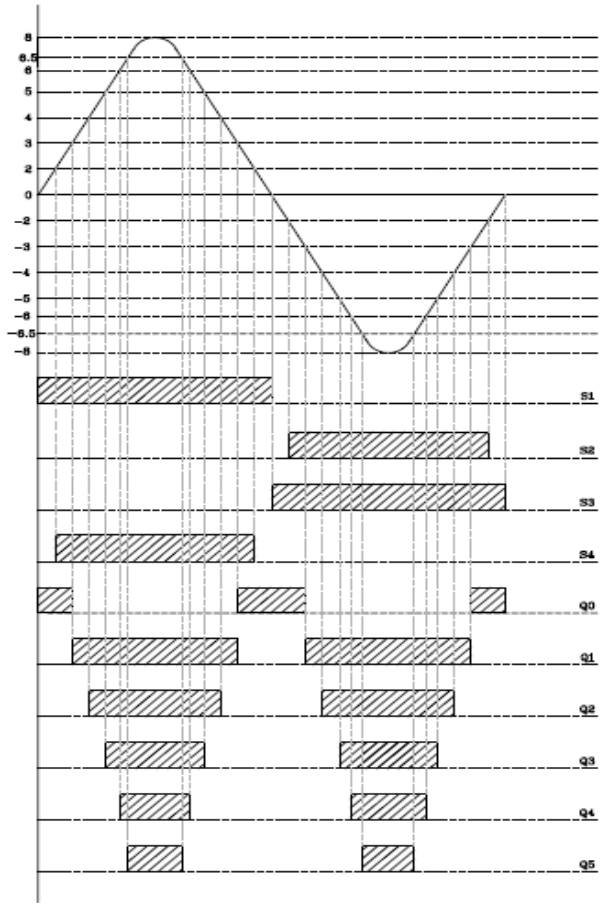


**Figure-2.** PWM Generation for sine modulation.

The SPWM schemes are more flexible and simple to implement, but the maximum peak of the fundamental component in the output voltage is limited to 50% of the DC link voltage and the extension of the SPWM schemes into over-modulation range is difficult

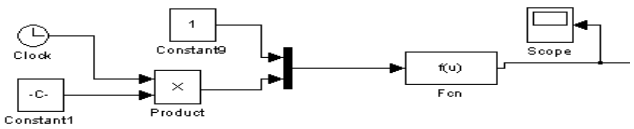


**Figure-3.** Generation of sine wave.

The above Figure-3 represents the simulation block which is used to generate the sine wave.

The amplitude value of the sine wave is entered in the function block and we receive the required amplitude sine wave at the output side where the scope is connected. Total thirteen Constant DC reference signals are provided with difference voltages. Six constant DC reference signals with the voltage level e1,e2,e3,e4,e5,e6 are provided on the positive half cycle and e1',e2',e3',e4',e5',e6' are provided on the negative half cycle and also a Zero reference signals.

### B. Trapezoidal PWM

Similar to the SPWM instead of Sine wave trapezoidal wave is used for generating the pulse.

### C. 1/6th Third harmonic injection PWM

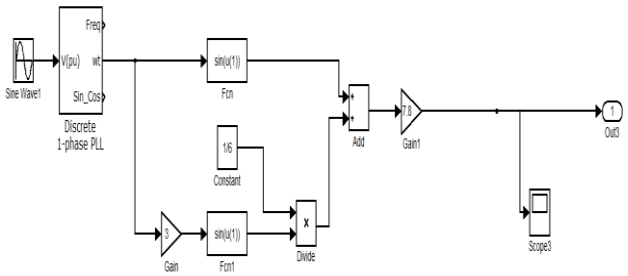


**Figure-4.** Generation of modulation signal for 1/6th third harmonic.

The above Figure-4 represents the simulation block used for 1/6th Third Harmonic wave.

A method to improve the gain of the pulse width modulator in a multilevel inverter is to inject a third harmonic. This technique is derived from conventional sinusoidal PWM with the addition of a 17% third harmonic component to the sine reference waveform as shown in above Figure-4. It should be noted that the 15% increase in gain over the SPWM technique is achieved at the expense of introducing third harmonics on the line to neutral waveforms. However for a balanced load with a floating neutral point, third harmonic current cannot flow and therefore third harmonic voltages are not present on

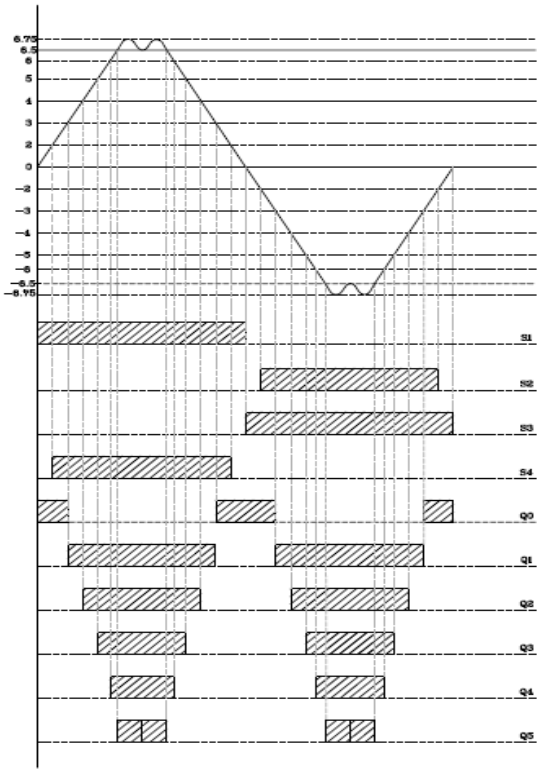


**Figure-5.** PWM Generation for 1/6$^{th}$THI modulation.

the line to line waveforms**.** Although, the above mentioned switching patterns for PWM converters provide increased gain compared with the conventional SPWM technique, the modulating waveforms have to be continuous regardless of their shape. As a result they do not provide any reduction in switching frequency compared with the SPWM. For third harmonic injection PWM, the reference waveform is defined as

$$\sin(\omega t)+1/6^{th}\sin(3\omega t) \quad (2)$$

## 4. SIMULATION SPECIFICATION

- Input Voltage : 24Volt
- Output Voltage :144Volt
- Switching Frequency:

H bridge -50Hz, DC-DC converter section =2*$f_m$

- Switch MOSFET :N-Channel
- RL Load :500+J0.314Ohms
- THD :10.17%
- Modulation :TPWM,SPWM

  1/6$^{th}$ THIPWM

### A. Simulation results

### i) Triangular PWM

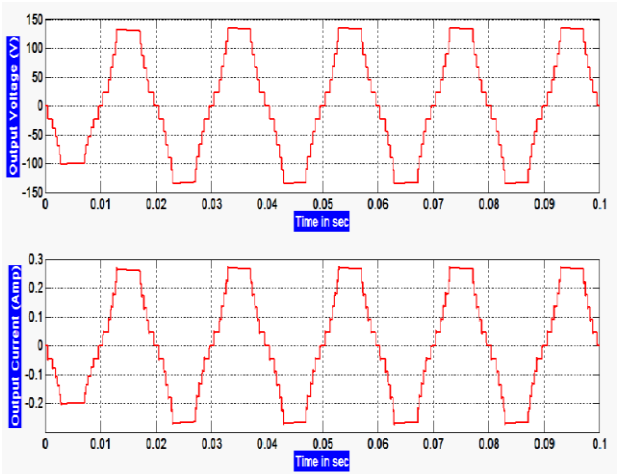


**Figure-6(a).** Output voltage and current waveform for TPWM.

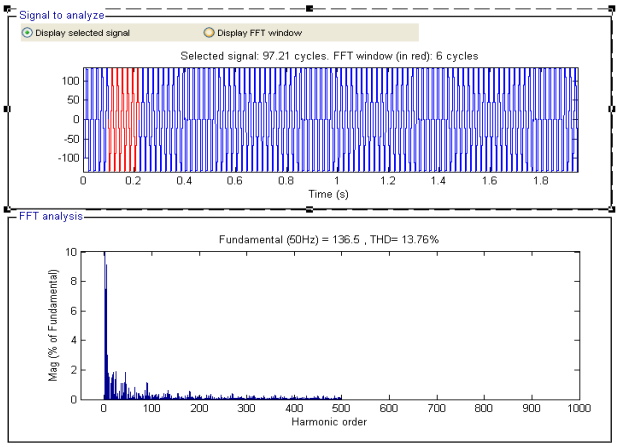


**Figure-6(b).** THD in % for TPWM.

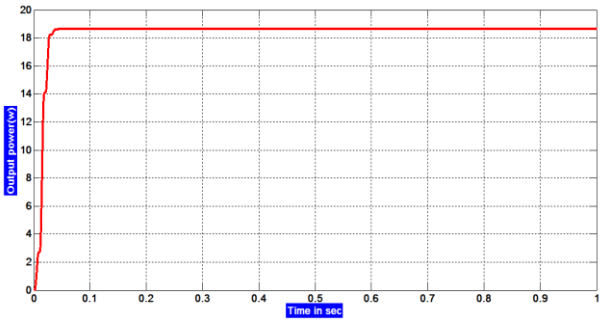


**Figure-6(c).** Output power waveform for TPWM.

The above Figure-6(a) represents the output voltage and current waveform. From the wave form it is observed that the output voltage is 135V and the voltage

stress across the switches in converter section is measured as 22V which is almost 6times less than the output voltage From the Figure-6(b) it is observed THD% as 13.76.The Figure-6(c) represents the output power waveform and it is observed 18.65Watts.

### i. Sinusoidal PWM

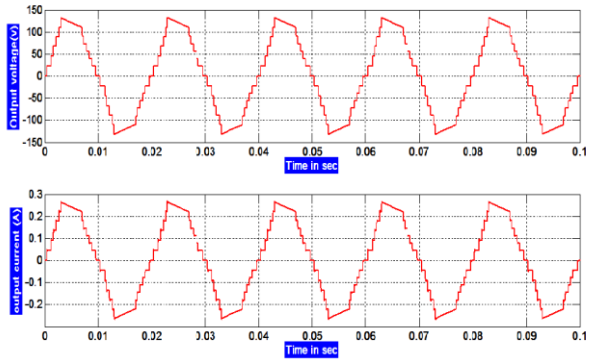


**Figure-7(a).** Output voltage and current waveform for SPWM.

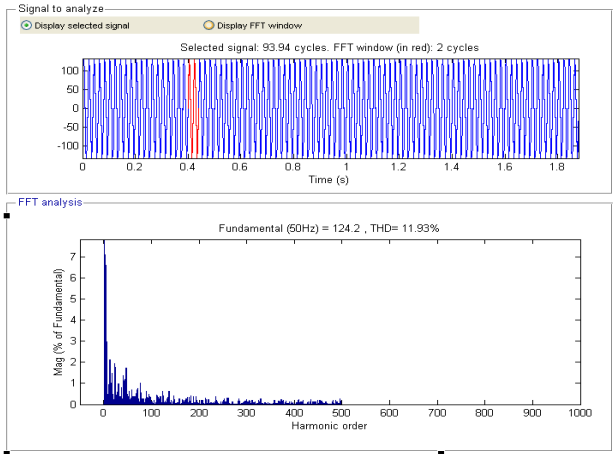


**Figure-7(b).** THD for SPWM.

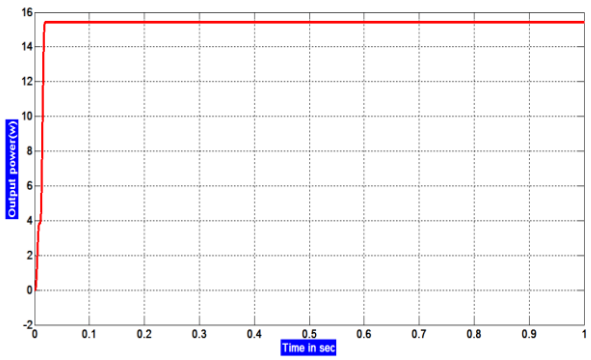


**Figure-7(c).** Output power waveform for SPWM.

The above Figure-7(a) represents the output voltage and current waveform. From the wave form it is observed that the output voltage is 132.5V and the voltage stress across the switches in converter section is measured as 21.5V which is almost 6times less than the output voltage. From the Figure-7(b) it is observed THD% as 11.93. The Figure-7(c) represents the output power waveform and it is observed 15.42Watts. Though the output power utilisation is reduced the THD reduction is observed around 13.3% w.r.t to TPWM technique.

### ii. 1/6$^{TH}$Third harmonic injection PWM

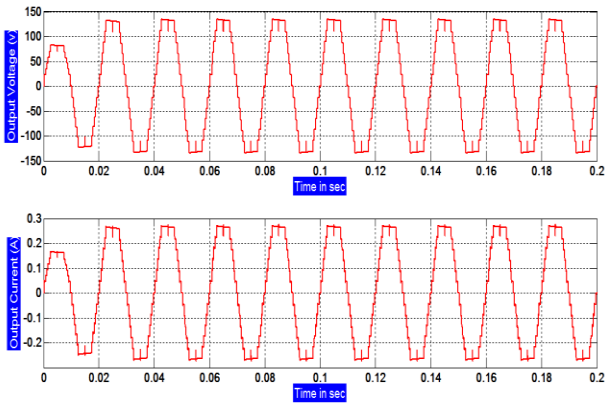


Fig8(a)

**Figure-8(a).** Output voltage and Current waveform for 1/6$^{th}$ THIPWM.

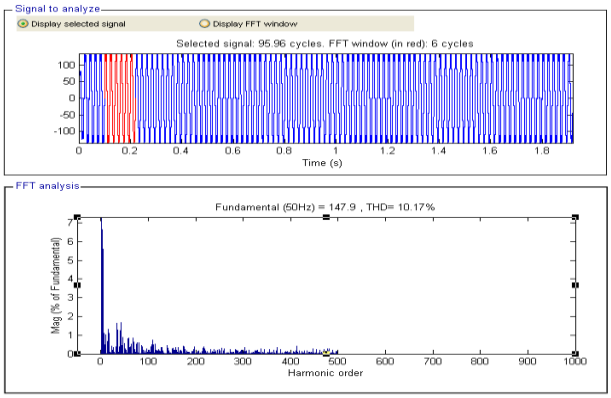


**Figure-8(b).** THD for 1/6$^{th}$ THIPWM.

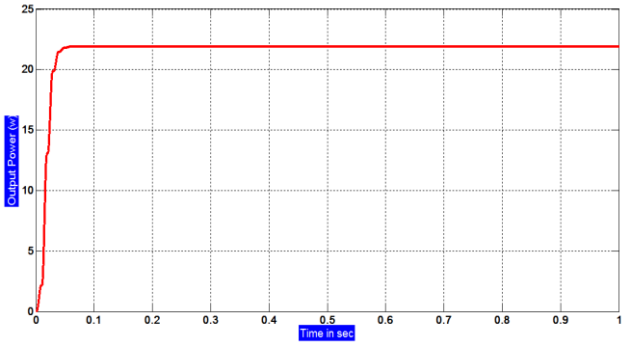


Fig.8(c)

**Figure-8(c).** Output power waveform for 1/6th THIPWM.

The above Figure-8(a) represents the output voltage and current waveform. From the wave form it is observed that the output voltage is 134.5V and the voltage stress across the switches in converter section is measured as 22V which is almost 6times less than the output voltage. From the Figure-8(b) it is observed THD% as 10.17. The Figure-8(c) represents the output power waveform and it is observed 21.8 Watts. The output power utilisation is increased and the THD reduction is observed around 14.75% w.r.t to SPWM technique.

### i. Conduction loss analysis

In the simulation results it is observed that the output voltage obtained is less than the desired output due to the conduction losses as detailed below.

### ii. Voltage drop

Upon switching on $Q_0$, the capacitor $C_1$ to $C_5$ is charged by the input voltage $V_{in}$ through diode as shown in Fig.1.Due to the internal resistance of diode pair ($R_D$) there will be a voltage drop ($V_{d1}$) which is represented as ($I*R_D$).Since there are 'n' parallel paths, to obtain the total voltage drop in capacitor charging cycle will be represented as mentioned below. In our topology n=5

$$V_{d1} = n* (I*R_D) \quad (3)$$

In capacitor discharging process the number of capacitor connected in series with $V_{in}$ are varied to provide different voltage levels to the RL load. During this period only one diode will be in the circuit, hence we can consider only Rd for the voltage drop and $R_Q$ is the internal resistance of the switch which will also contribute to the voltage drop due to the internal resistance. The total voltage drop during discharging cycle is represented as

$$V_{d2}=n*((i*R_d)+(i*R_Q)) \quad (4)$$

### iii. Power loss

Due to the internal resistance of diode and switches there will be a power loss.

The power loss in charging and discharging cycle is represented as

$$P_D = n * (Irms^2 * R_D) \quad (5)$$

$$P_C = n * (Irms^2 * R_Q) \quad (6)$$

Total conduction Power loss $P_T=P_D+P_C$ (7)

## 5. EXPERIMENTAL RESULT ANALYSIS

The analysis has been done with various Load resistances. The Load resistance has been varied like 100Ω, 500 Ω, 700 Ω, 1K Ω and various parameters discussed above for each resistance is noted and found the optimum result in the load resistance 500Ω.

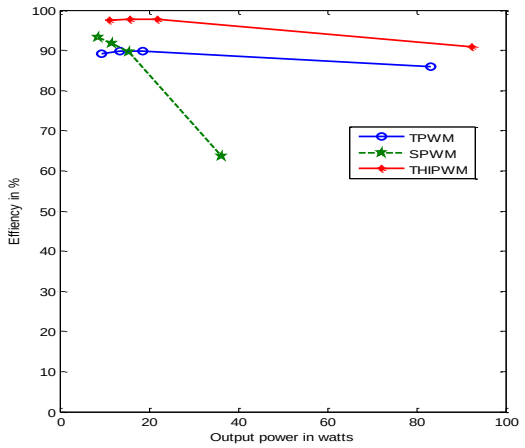


**Figure-9.** Load analysis for TPWM, SPWM, THIPWM.

The above Figure-9 represents the output power Vs efficiency curve for all the three modulation techniques. From this we can understand the efficiency of the topology when the output power changes.

**Table-2.** Simulation results.

| **Simulation results- RL Load** (R-500 ohms, L-1mH) | | | | |
|---|---|---|---|---|
| **S. No.** | **Parameter** | **TPWM** | **SPWM** | **1/6$^{th}$ THIPWM** |
| 1 | Output Power(W) | 18.65 | 15.42 | 21.88 |
| 2 | Efficiency %(W) | 89.88 | 89.6 | 97.74 |
| 3 | THD%(W) | 13.76 | 11.93 | 10.17 |
| 4 | Output Voltage(W) | 135 | 132.5 | 134.5 |
| 5 | Conduction loss(W) | 0.0254 | 0.0298 | 0.0412 |
| 6 | Voltage stress (V) | 22 | 21.5 | 22 |

## 6. CONCLUSIONS

The main advantage in the proposed topology is that the harmonics contents are reduced by increasing the level and also switches. Since the Switches are operated at lower frequency, the losses and switching stress is reduced. The logics involved for switching is very simpler and in this topology there is no issues of capacitor voltage balancing. Various parameters were noted from simulation (Table-2) using MATLAB for all the three modulation techniques and the analysis has been carried out for voltage stress and conduction losses and the results were compared. It is observed that in 1/6$^{th}$THIPWM technique the output power utilisation, efficiency is improved and THD% is reduced compared to other two techniques.

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