



COMPARISON OF VARIOUS RIPPLE CARRY ADDERS: A REVIEW

Jimin Cheon

School of Electronic Engineering, Kumoh National Institute of Technology, 61 Daehak-ro, Gumi, Korea

E-Mail: jimin.cheon@kumoh.ac.kr

ABSTRACT

As portable multimedia and communications applications emerge, the need for low power, small area, and low delay time digital circuits becomes more prominent. Addition process is the most used operation in any DSP because addition is involved in all other mathematical operations. Therefore, adders design is considered critical because it influences the performance of the system in terms of power and delay. In this paper, we introduce various ripple carry adder in terms of static CMOS logic, dynamic CMOS logic, and others.

Keywords: ripple carry adder, static CMOS logic, dynamic CMOS logic, normal process complementary pass transistor logic (NPCPL).

INTRODUCTION

Low power, small area, and fast logic design became significant due to the spread of wireless communication and portable computing systems. Adders construct a major block in any DSP since all the arithmetic operations (subtraction, multiplication and division) rely on addition. There are many kinds of adder structure, but ripple carry adder (RCA) is the most low power, and small area design among them. However, even if same RCA, there are lots of design logics which have different performances. In this paper, we analyze various RCA in terms of static CMOS logic, dynamic CMOS logic, and others.

This paper organized as follows. Section II introduces operation and characteristic of simple basic RCA. Section III describes various kind of the RCA in terms of static CMOS logic, dynamic CMOS logic, and others and also compares and analyzes performance of each RCA. Section IV concludes the paper.

BASIC ANALYSIS OF RCA

Basic unit of RCA

The basic unit of a RCA is a full adder (FA). An FA adds two binary numbers with a carry-in. The Structure representation of the conventional CMOS FA appears in Figure-1. There are a total of three inputs for the FA, two for the input numbers A and B, and one for the carry-in, C_{in} . The outputs are the Sum and carry-out C_{out} [1].

The logic functions corresponding to terminals Sum and C_{out} are as follows:

$$Sum = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = (A \oplus B) \cdot C_{in} + A \cdot B \quad (2)$$

Basic theory and operation

The basic unit of a RCA is an FA. It can be extended indefinitely to any number by connecting the carry -out of the previous 1-bit FA to the carry-in of the next 1- bit FA. An n-bit RCA consisting of n single-bit FAs is described in Figure-2. The figure clearly shows that the carry bit ripples through the chain of the cascaded FAs, from a lower bit to the next higher order FA [2, 3].

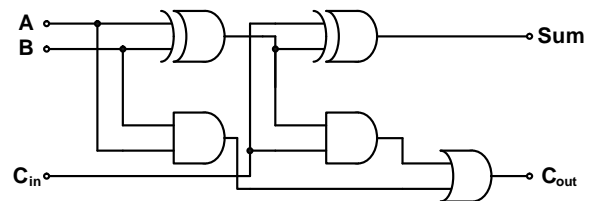


Figure-1. Structure of an FA.

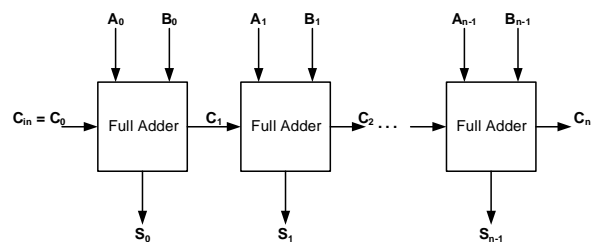


Figure-2. Structure of an RCA.

Table-1. Comparison between different adders [3].

Types	Power	Delay	Area
Ripple Carry Adder	1	1	1
Carry Look-ahead Adder	1.7	0.21	2.1
Conditional Sum Adder	2.4	0.16	2.9
Carry Skip Adder	1.2	0.25	1.6



Comparison between different type adders

In order to compare the performance of the different adders, a 16 bit adder was used as a test vehicle for each type in [3]. The designs are implemented using standard CMOS cells in 0.5- μm technology. All the designs are optimized for power-delay product. Table 1 shows the comparison results between the RCA, carry look ahead adder (CLA adder), conditional sum adder, and carry skip adder in terms of power, delay and area. The comparison result shows that RCA has the smallest power and area [3].

Advantage and disadvantage

RCA occupies the smallest area and dissipates the lowest power. Also it offers good performance for random input data [4]. In this case, average energy consumed by the

RCA is $E_{\text{avg}} = O(W)$ where W is the word-length of the operands. For word-length $W \geq 16$, the error in the theoretical estimates is around 15% [5]. Nonetheless, its delay characteristics depend heavily on the length of the carry propagation path, thus making it a relatively unfavorable choice for circuits with nonrandom input operands. The worst case delay increases linearly with the length of the carry propagation path, which depends on the number of bits processed by the operands, n . Also, the area of the adder is proportional to n [3]. Therefore, in situations when high speed performance is crucial and the minimum amount of hardware is underperforming, using an RCA in the arithmetic operation would be detrimental.

VARIOUS KIND OF RCAs

Changing an FA structure is necessary to improve performance of an RCA. There are lots of FA structures, but it can classify static CMOS logic, dynamic CMOS logic, and others.

Static CMOS Logic

The simple structure of conventional FA cell is based on static CMOS logic. One FA cells design using a total of 32 transistors [6]. Therefore, the conventional structure has not only large power but also long delay time.

A FA can be designed to use multiplexers and XORs. While this is impractical in a complementary CMOS implementation, it becomes attractive when the multiplexers and XORs are implemented as transmission gates [7].

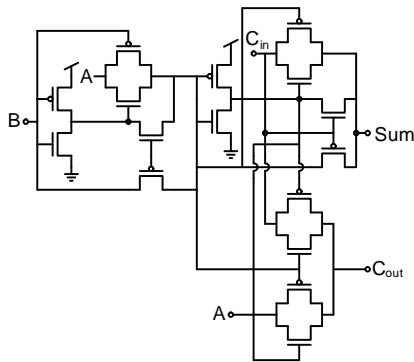


Figure-3. Transmission function full adder (TFA).

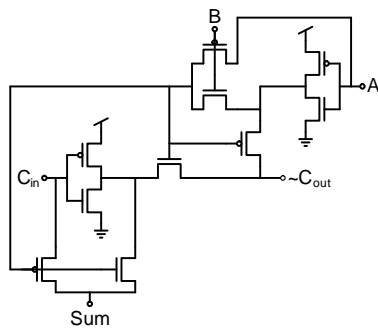


Figure-4. 10-transistor full adder (10-T FA).

Table-2. Comparison between the two FA cells.

@ 1 GHz at 3.3 V	Power	Delay
Power	170 μW	81 μW
Critical Path Delay	0.120 ns	0.086 ns
Number of Transistors	16	10

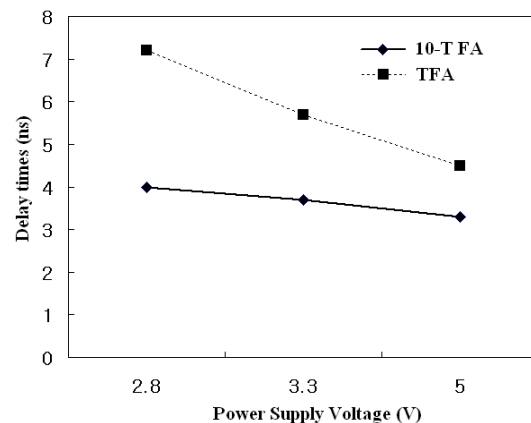


Figure-5. Delay time versus power supply voltage.

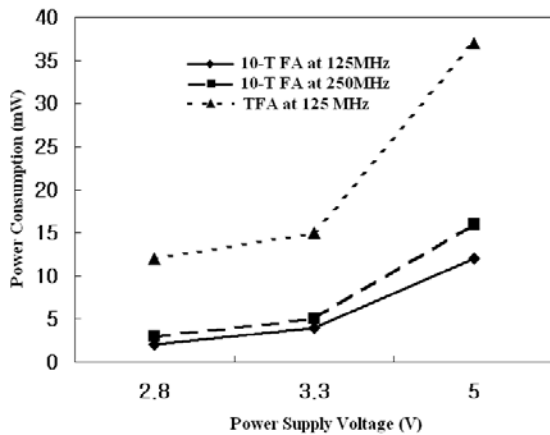


Figure-6. Power dissipation versus power supply voltage.

One of the FAs based on this approach is shown in Figure-3, the transmission function FA (TFA). The TFA consists of 16 transistors and dissipates less power than conventional CMOS FAs [8]. This structure has meaning of CMOS FA designed by transmission function theory.

A better performance of FA structure is Figure-4, the 10-transistor low power high speed FA (10-T FA) cell [9]. The critical path consists of an XOR gate; an inverter and one pass transistor. In a n-bit adder circuit, the new adder cell will give alternate polarity for the carryout in the odd and even positions. The inverters in the structure of the 10-T FA cell act as drivers. Therefore, each stage will not suffer from degradation in its deriving capabilities. The saves power, area and time. Table-2 shows 10-T FA has much better performance than TFA.

Two prototypes of 32-bits ripple carry adder are constructed. One prototype uses a TFA, whereas the other prototype, which uses a 10-T FA, is constructed with a two-transistor inverter driver. Figure 5 shows the delay time and Figure 6 shows power dissipation of 32-bit RCA of each prototype. At a power supply voltage of 2.8 V, the critical path delay time for a 32-bit RCA that uses the TFA prototype is 7.2 ns, while it is observed to be 4.1 ns for the 10-T FA prototype, thereby exhibiting a speed improvement of 44 percent over the former. Clearly, the 10-T FA prototype outperforms the TFA prototype throughout the entire operating range. For the power consumption consideration, it is observed that the 10-T FA prototype dissipates 2.1 mW, which is 81 percent less than the 11 mW dissipated by the TFA prototype. Both of the 32-bit RCAs were simulated at a supply voltage of 2.8 V and a clock

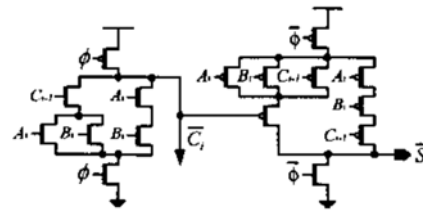


Figure-7. 1 bit dynamic FA.

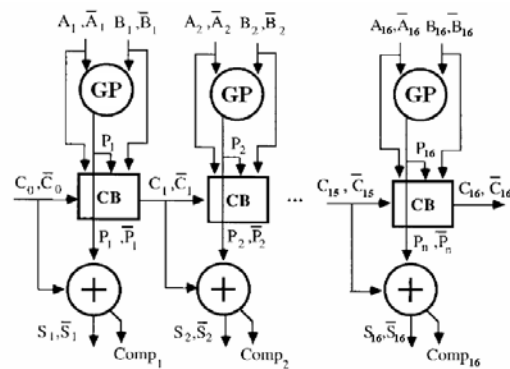


Figure-8. 16 bit DRCA using DCVS logic.

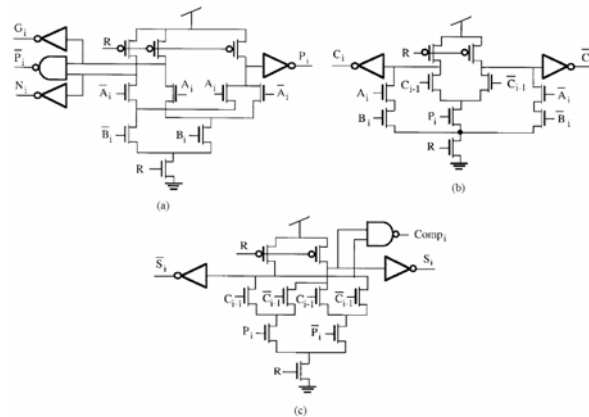


Figure-9. DCVS DRCA components (a) carry generate and propagate (GP) block (b) carry bypass (CB) block and (c) EXOR block.

frequency of 125 MHz. It is clear that the 10-transistor prototype displays enhanced power dissipation over the TFA for the operating range of 2.8 V to 5 V. It can operate satisfactorily at frequency up to 350 MHz at a supply voltage of 5 V. This means that large architectures can be built to operate at very high frequencies without compromising the small-area and low-power characteristics, which are the main criteria for today's evolving technology.



Dynamic CMOS logic

Dynamic logic is an alternative logic style which obtains a similar result to static logic, while avoiding static power consumption. With the addition of a clock input, it uses a sequence of precharge and conditional evaluation phases [7]. Dynamic CMOS logic contains lower number of transistors and faster speed than static CMOS logic. Also it only consumes dynamic power, but overall power dissipation can be significantly higher compared with a static logic gate. Therefore, using dynamic logic can have merit of area, and delay time than static logic on special condition. Figure 7 shows 1-bit dynamic full adder.

Figure-8 shows the 16-bit dynamic RCA (DRCA) using differential cascode switch voltage (DCVS). DCVS logic is a differential logic style derived from domino logic made up of two complementary NMOS logic trees. This logic requires true and complementary input signals to switch the two outputs to different logic states. In self-timed circuits, its dual-rail property can be used to generate completion signals for combinational logic in a general way [4]. The mathematical formulation of DCVS logic of DRCA is given below [10]. Let A_i and B_i be the i^{th} bits of the input data and C_{i-1} the carry-in for stage i . Then we have

$$C_i = G_i + P_i C_{i-1} \quad (3)$$

$$S_i = C_{i-1} \oplus A_i \oplus B_i = C_{i-1} \oplus P_i \quad (4)$$

$$P_i = A_i \oplus B_i \quad (5)$$

$$G_i = A_i B_i \quad (6)$$

where P_i is the carry propagate signal and G_i is the carry generate signal. In adapting (3) and (6) to differential signal, it is necessary to define their complements, which are expressed as

$$\overline{C_i} = \overline{A_i B_i} + P_i \overline{C_{i-1}} \quad (7)$$

$$\overline{S_i} = \overline{C_{i-1}} \oplus P_i \quad (8)$$

Figure-9 shows the each slice of 1-bit is made up of a carry generate and propagate block (GP) which computes the signals P_i and $\overline{P_i}$ in parallel, a carry bypass block (CB), and an EXOR output stage. This structure has low delay time but greatest power and area penalty.

Figure-10 shows DRCA using race-free NP CMOS logic [10]. Conventional NP CMOS DRCA has inherent race problems, but this logic eliminates race

problems by including 4 transistors. It has not only low delay time but also small number of transistors than DCVS DRCA.

Figure-11 is saving the area by replacing as many as PMOS transistor in NP CMOS DRCA with the NMOS transistors. The resultant structure is called All-N DRCA. Note that an inverter is required between the carry logic and sum logic.

Figure-12 intends to eliminate the need of negative inputs. To achieve this, however it is necessary to have a all-PMOS composition of the sum logic. As will be seen in simulation results part, the all-PMOS structure has made the design slowest among these several DRCAs [10].

In order to maintain the advantage of positive inputs of the all-PMOS logic (Figure-12), it needs to replace the static inverter of all-PMOS logic with a dynamic one (Figure-13). The fast response time of the dynamic inverter compensates the speed lost in the all-PMOS sum logic and makes the design the fastest among all the proposed DRCAs.

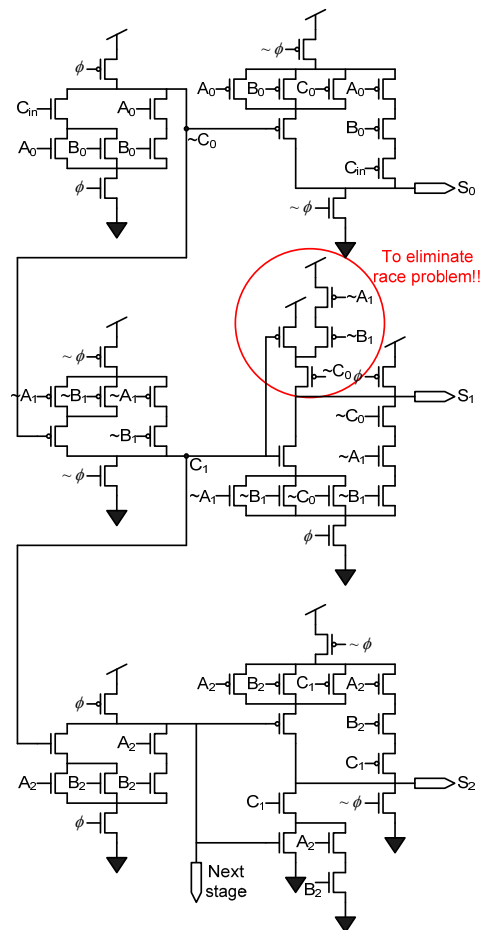


Figure-10. Race-Free NP CMOS DRCA.

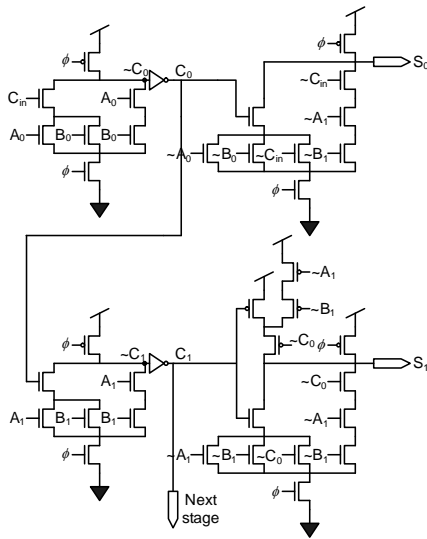


Figure-11. All-N (AN) dynamic CMOS logic of DRCA.

Table-3 shows the transistor count, the total transistor width, the worst-case delay of 16-bit DRCA's using different cells, as well as those of the static RCA (SRCA). The power dissipation is measured for each circuit with the worst-case delay. The DCVS DRCA, though much faster than the SRCA, as the worst delay among all DRCA's. Further, it has the greatest power and area penalty. The

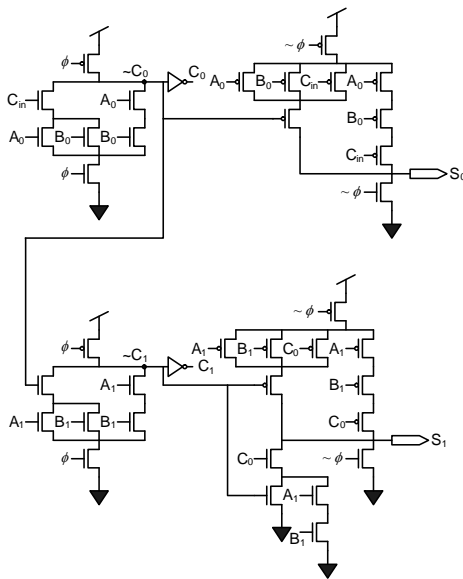


Figure-12. Primary input of DRCA becomes positive logic.

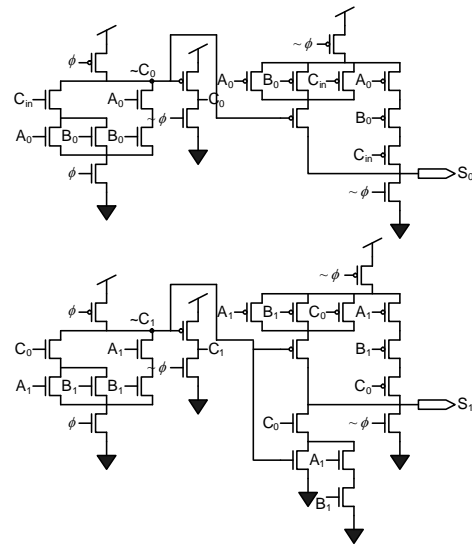


Figure-13. Using dynamic inverter in Figure 12's logic.

Table-3. Features of various 16-bit RCA [10].

Designs	Delay (ns)	Power (mW)	PDF	Width (μm)	# of TRs
SRCA	2.327	2.23	4.98	901.84	448
DCVS DRCA	1.483	13.26	19.66	3334.58	802
NP DRCA	1.015	7.79	7.91	1784.94	380
AN DRCA	1.189	4.06	4.78	843.18	430
PL DRCA	1.248	4.83	6.21	957.04	396
DI DRCA	1.013	7.93	8.03	1108.96	396

dynamic inverter (DI) DRCA is the fastest among all RCAs. It is 2.3 times faster than the SRCA and 1.46 times faster than the DCVS DRCA. The AN DRCA has the lowest power and area penalty among all DRCA's. It is even smaller than the SRCA. Although it consumes more power than the SRCA, its power-delay product (PDP) is superior to that of the SRCA [10].

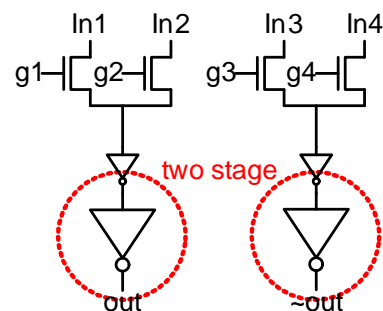


Figure-14. New basic NPCPL cell.

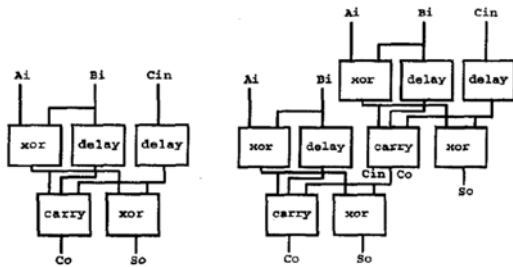


Figure-15. 1 bit FA and 2 bits FA using NPCPL cell.

Table-4. New input combination.

Function	In1	G1	G2	In2	In3	G3	G4	In4
AND/NAND	A	$\sim A$	A	B	$\sim A$	B	$\sim B$	$\sim B$
OR/NOR	A	A	$\sim A$	B	$\sim A$	$\sim B$	B	$\sim B$
XOR/XNOR	A	B	$\sim B$	$\sim A$	B	$\sim A$	A	$\sim B$
DELAY	A	H	L	A	$\sim A$	H	L	$\sim A$

Others

Wave pipelining is a very efficient way to design high-throughput RCA, but it requires accurate delay control. Hence, CMOS normal process complementary pass transistor logic (NPCPL) has been used in place of static CMOS logic which suffers delay variation depending on input combinations. The most important advantage of using NPCPL is that all kinds of gates can be implemented with the same basic structure, hence the delays of all kinds of gates can be kept the same. However, conventional NPCPL has two major problems for high speed wave pipelined design. One is the insufficient driving capability, and the other is the unbalanced loading.

In [11], new basic NPCPL cell solve the two problems of conventional NPCPL cell. The load unbalancing problem has been solved by a new input combination and the problem of insufficient driving capability has been overcome by a two-stage buffer. Table 4 shows new input combination and Figure 14 shows new basic NPCPL cell which contains two stage buffers. In [11], experimental results obtained from 16-bit RCA using new NPCPL cell in 0.8- μ m technology shows 900 MHz throughput.

CONCLUSIONS

In this paper, we analyze and compare various RCAs in terms of static CMOS logic, dynamic CMOS logic, and others. As we analyzed above, static CMOS logic can operate in low power dissipation, whereas dynamic CMOS logic can operate much less delay time. By using NPCPL cell, 16-bit RCA provides throughput of 900MHz which is the fastest among introduced RCAs.

ACKNOWLEDGEMENT

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REFERENCES

- [1] K. S. Yeo and K. Roy. 2005. Low-Voltage Low-Power VLSI Subsystems, Mc Graw Hill.
- [2] I. Koren. 1993. Computer Arithmetic Algorithms, Englewood Cliffs, New Jersey: Prentice Hall.
- [3] M. W. Allam and M.I. Elmasry. 1998. Low-power implementation of fast addition algorithms. IEEE Canadian Conf. Electrical and Computer Engineering. pp. 645-647.
- [4] G.A. Ruiz. 1998. Evaluation of three 32-bit CMOS adders in DCVS logic for self-timed circuits. IEEE J. Solid-State Circuits. 13(4): 604-613.
- [5] L. Montalvo and K.K. Parhi. 1996. Estimation of Average Energy Consumption of Ripple-Carry Adder Based on Average Length Carry Chains. In: proc. 11th Design of Integrated Circuits and Systems Conference (DCIS'96), Barcelona, Spain.
- [6] N.H.E Weste and K. Eshraghian. 1993. Principles of CMOS VLSI design: A Systems Perspective, Reading, Massachusetts: Addison-Wesley.
- [7] J. Rabaey. 2003. Digital Integrated Circuits: A Design Perspective, Englewood Cliffs, NJ: Prentice Hall.
- [8] N. Zhaung and H. Wu. 1992. A New Design of the CMOS Full Adder. IEEE J. Solid-State Circuits. 27(5): 840-844.
- [9] H.A. Mahmoud and M.A. Bayoumi. 1999. A 10-transistor low-power high-speed full adder cel. In: IEEE Int. Symp. Circuit and Systems, pp. 43-46.
- [10] C.J. Fang, C.H. Huang, J.S. Wang, C.W. Yeh. 2002. Fast and compact dynamic ripple carry adder design. In: Proc. IEEE Asia-Pacific Conference. pp. 25-28.
- [11] H. Choi, S.H. Hwang. 1996. Design of wave-pipelined 900MHz 16b ripple-carry adder using modified NPCPL. In: IEEE Int. Symp. Circuit and Systems. pp. 182-184.