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PROTECTION TECHNIQUE FOR TRANSIENT OVERVOLTAGE DUE TO CAPACITOR BANK SWITCHING IN DISTRIBUTION SYSTEMS USING HIGH PASS FILTER

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ABSTRACT

Switching transients, generated during energizing and de-energizing operations of capacitor banks can damage the capacitor itself and other sensitive components in the network. To reduce such effects, this study suggests a High Pass Filter (HPF) transient limiter to provide low impedance at the instant of capacitor energizing, thus, allowing the switching transients to decrease effectively. In addition, this study covers different operational cases to find suitable methods or techniques that can be used to limit the impact of capacitor transient switching. The simulation which was based on an electrical network model in low voltage (LV) power systems (0.415 kV) was modelled using Power System Computer-Aided Design (PSCAD) software, focused on the peak transient magnitude, event duration and switching frequency. The results are presented in detail. The outcome of this study can serve as an essential guidance for manufacturing technologists as well as electrical engineers in addressing and developing capacitor banks, thus solving transient switching issues for low voltage systems.

Keywords: capacitor banks, transients' overvoltage, high pass filter.

INTRODUCTION

Capacitor banks are widely utilized as a part of both transmission and distribution systems, to boost system capacity, decrease power losses, and improve voltage conditions and performance of transformers at different parts in the grid. However, despite all significant features of connecting capacitors in the field, they can also contribute to power quality problems. The switching process to energize and de-energize these capacitor banks happen often because of the system load variation or voltage fluctuation. These switching operations lead to transient overvoltage, which may damage the switching appliances termed as "striking" or "re-striking" of the switching device. The energizing of the capacitor bank causes high in rush current and transient voltage oscillation at the capacitor bank station [1]. Generally, the decline in service power, cost and release of system capacity are the major motivators, with loss reduction and upgrading of voltage level stability being additional benefits of lesser importance. With the trend towards a higher cost of electric power bills and lowering of system capacity, it is expected that there will be many more opportunities for capacitor applications at the medium voltage level [2] in the future. In low voltage (LV) systems, capacitor banks may reduce and totally prevent power factor penalties [3]. Transients are microsecond to lower order millisecond scale fluctuations, in the steady condition voltage or current waveform. There is no obvious similarity between transients and dip or swells, though, for the plurality fraction discussion, any instance with a duration less than half a cycle is apparently called a transient [4]. At present, there are no concrete solutions in general for these transient issues. In this paper, we analyze the issues of capacitor banks during the switching operations, and propose solutions to reduce such.

TRANSIENT OVERVOLTAGE MITIGATION TECHNIQUES

The current devices which are used for transient overvoltage control make an effort to reduce the transient overvoltage or overcurrent at the time it is generated or limit the overvoltage at local and remote locations; these devices are illustrated below. Preceding research has recommended that the efficiency of such control procedures depends on the system and that close analysis is needed to choose the ideal control project. Analysis of distribution system capacitor applications is not often adequately done, and generally banks are fitted with no control of transient overvoltage. All these procedures have several pros and cons in relation to reducing transient overvoltage, cost, requirements for installation, and operational maintenance and reliability. There are several methods of limiting transient overvoltage during capacitor bank switching. They try to reduce the overvoltage transient while the capacitor bank is energized at the point of application. There are numerous technologies obtainable that help in reducing capacitor overvoltage and inrush current transients. The devices of transient mitigation are classified as follow [5].

Pre-insertion resistor

This is a very effective way of minimizing the degree of surge caused by capacitor switching transients [6]. The addition of pre-insertion resistors helps to minimize the severity of the transient by temporarily providing greater losses in the circuit, which lead to a reduction in the peak values of the voltage and current transients [7]. However, synchronizing the resistor and the main contacts is needed, and improperly sized resistor may produce higher transient when the resistor is by passed and therefore in many applications thorough maintenance is

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needed when there is excessive insertion time in replacement process [8].

Pre-insertion Inductors

The Advantages of adding extra inductance to the supply during the energizing is that it reduces voltage transients at the utilization voltage bus [9]. Hence disadvantages of pre-insertion inductors are; limitation of ideal values because of the dissipation of energy is constrained, peak inrush current, bypass transient magnitude and physical size and weight.

Control of voltage closing zero

This method uses a complex electronic control and the Zero Voltage Closing (ZVC) control closes or energizes the bus capacitor near voltage zero to reduce overvoltage and inrush current transient. The applications of ZVCs are boosted by the fact that, the timing reference of such could be repeated by using new microprocessor technology to control supervision of ZVC devices, closing tolerance of ±2 ms is effective, transients are most effectively limited by this method and there is no need for field timing adjustment with the attractive automatic calibration. Disadvantages of this method are the possible occurrence of restrikes on some ZVC devices, sophisticated electronic control can be expensive and effectiveness of ZVC control is system dependent.

Metal oxide varistor (MOV)

Application of MOV may limit the transient overvoltage to the protective level at the point of application. The MOV switch from high impedance to low impedance mode as the transient voltage exceeds a certain threshold value, clamping the voltage output. The voltage protection level of the MOV should be selected in a way that it is lower than the impulse withstanding voltage of the equipment to be protected. However in LV systems, customer application may be subjected to severe energy duty if voltage magnification occurs.

Symmetrical structure transient limiter (SSTL)

The SSTL, a series connected device, is characterised by the following features; A high impedance appears immediately following the energizing of the capacitor, there is practically zero effect on the control of energizing transients following the injection of the harmonic; the steady state is quickly recovered following the switching transients and the in the steady state SSTL has almost zero impedance [10].

High pass filter

The importance of this technique is that the filter provides low impedance bypassing to reduce the overvoltage transients without leading to nuisance tripping.

METHODOLOGY

The isolated capacitor bank under consideration is connected to the low voltage system (LV) 0.415 kV, 50.0 kvar, five steps. Utilities frequently use capacitor banks for the maintenance of the distribution voltage level under different loads. The utility capacitor banks switching event is a rather common power-system phenomenon. Figure-1. shows a single-line diagram of a characteristic utility capacitor bank switching event in a power-distribution system. To assess the impact of utility capacitor switching transient on LV system, Figure-2. provides a simplified depiction and an equally similar circuit of the power system. The simplified representation for a capacitor switching transient events limiter in a standard power system is discussed. The analysis can be made simple by presenting the power system as an LC circuit as shown in Figure-2. for the transient response [11]. The determination of this simulation is to determine the highest degree of overvoltage transient, and inrush current generated when energizing 0.440 kV capacitor banks, and these models use several runs in PSCAD /EMTDC, to differ close time of a circuit breaker of the capacitor bank in time period 0. 005s (one cycle of sine-wave frequency equals 50Hz) and then increases of the time step obtained results are illustrated below and also the system load varies from 20, 40, 60, 80 kW, while the power factor is changed from 0.7 - 0.9 the obtained results are illustrated below . Several cases were simulated using PSCAD/ EMTDC in order to evaluate the devices used in limiting transient overvoltage. [12]

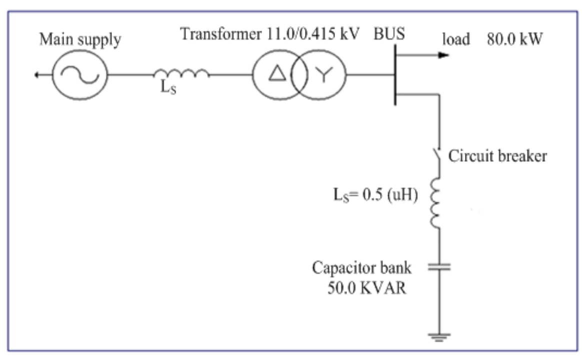

Figure-1. Model of single line isolated capacitor banks 50.0 kvar, 5.0 steps.

From Figure-2 the differential equation can be written as follows:

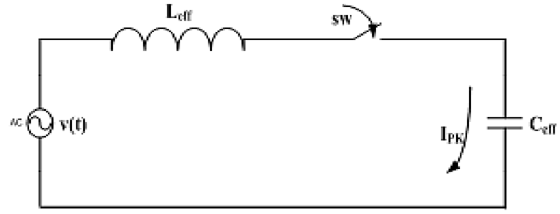

Figure-2. Equivalent circuit of isolated capacitor banks.

$$L_{eff}\frac{d}{dt}i(t)+\frac{1}{C_{eff}}\int i(t)dt = v(t) \quad (1)$$

Where L_{eff} is the effective line inductance and C_{eff} is the effective capacitance.

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The characteristic impedance Z_0

$$Z_0 = \frac{L_{eff}}{C_{eff}} \tag{2}$$

And the resonant frequency,

$$\omega_n = \frac{1}{\sqrt{L_{eff} C_{eff}}} = n = \frac{\omega_n}{\omega} \tag{3}$$

Where *n* is the per-unit natural frequency and ω is the fundamental power system frequency the peak current

$$I_{peak} = \frac{V_{pk}}{Z_0} \tag{4}$$

The peak value of the capacitor voltage *Vpk* can be expressed as

$$V_{Peak} = I_{pk} Z_0 \left(\frac{n^2}{n^2 - 1} \right) \tag{5}$$

The worst case of the voltage peak may happen on restriking the voltage across the contact if the switch is twice the supply voltage as follows [13]

$$V_{P.critical} = V_{peak} - \left(-V_{Ceff}\right) = 2V_{peak} \tag{6}$$

The instantaneous current above can be said to be

$$I_{peak} = \frac{2V_{peak}}{Z_0} \tag{7}$$

Figure-3 illustrates the model circuit of isolated capacitor banks with high pass filter, in high pass filter frequency, optimal factor m, and MVAR are required. The capacitor capacitance is given by

$$MVAR_C = \frac{kV^2}{X_C} \tag{8}$$

The output *MVAR* of the filter

$$= \frac{kV^2}{\left(X_C - X_L\right)} \tag{9}$$

Where X_L is th

The resonant frequency f_0 of the filter is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{10}$$

Where *L* and *C* the inductance and capacitance of the filter, the induct L

$$= \frac{1}{(2\pi)^2 (f_0)^2 (C)} \tag{11}$$

The fundamental current through a harmonic filter is given by

$$I_F = \frac{V\left(Line - Line\right)}{\sqrt{3}\left(X_C - X_L\right)} \tag{12}$$

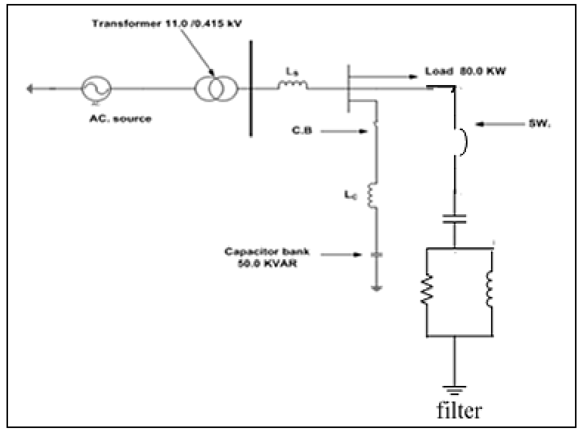

Figure-3. Model circuit of isolated capacitor bank with high pass filters.

$$L = \frac{1}{(2\pi)^2 (f_0)^2 (C)} \tag{11}$$

The fundamental current through a harmonic filter is given by

$$I_F = \frac{V\left(Line - Line\right)}{\sqrt{3}\left(X_C - X_L\right)} \tag{12}$$

The nth harmonic current through the filter can be calculated by $I_{FLITER}(n) = \frac{I_F}{n}$ n impedance harmonic number of frequency[14].

The optimal factor *m* is given by

$$m = \frac{L}{R^2 C} \tag{13}$$

The filter reveals the following characteristic:

1- it offers low harmonic impedance during transients switching
2- The filter is accomplished for different values of frequencies.

A High Pass filter can effectively dampen higher frequency resonances produced by system capacitance. Although this capacitance cannot be eliminated, High-Pass Filters can be beneficial in several ways. High-Pass Filter Resistors can give a low impedance path around a standard notch harmonic filter because its impedance shows no increase with frequency. Figure-4 illustrates how the impedance of the High-Pass Filter at high frequency is minimized by applying a High-Pass Resistor[15].

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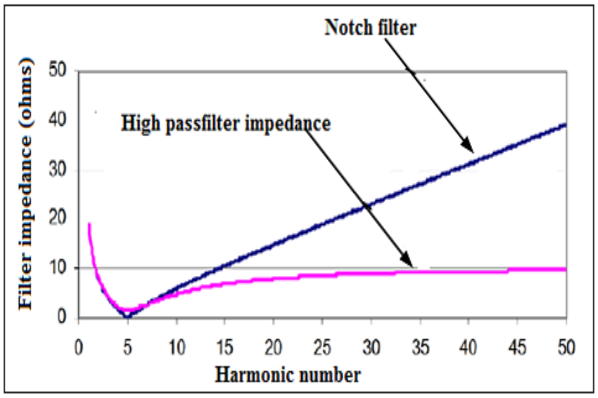

Figure-4. High - pass filter compared to standard notch-tuned filter [16].

SIMULATED RESULTS AND DISCUSSION

For the switching of isolated capacitor bank, several cases were simulated using PSCAD software. Simulation model of the low voltage distribution capacitor bank 50.0 KAR five steps, 0.415 kV was established to determine the effects of capacitor bank energization and de-energization in low voltage system. Specifically, we concentrated on the peak transient overvoltage, transient duration, transient overvoltage and harmonic order, and high frequency inrush currents that are a result of this switching operation of capacitor at different loads. Figure-1 is a simplified model of single line isolated capacitor banks 50.0 kvar, 5.0 steps, and Figure-3. illustrates the proposed high pass damping filter.

Table-1. shows the peak transient overvoltage line–to-line when it is energized by 0.415kV. The line voltage reaches about 2.22 pu at four step switching. Figure-5 illustrates the graph showing the pu. Peak voltage magnitude when switching the isolated capacitor bank in low voltage system (LV). Figure-5 explain transient overvoltage duration during the switching**.**

Table-2 shows that the peak inrush current grows in relation to the number of steps switched into the system because the large energy storage in the bank at the instant of steady frequency oscillations. The increasing of the number of the steps increases the capacitance of the system that leads to lower Therefore the magnitude of the oscillating voltage decreases as the shared common voltage among capacitor banks is increased. It can clearly be seen that the transient overvoltage can be as high as 512 V for the phase voltage, which is approximately 2.19 pu as shown in Figure-6. When energizing 15.0 Kvar with load of 80.0 kW.

Several load conditions were considered for capacitor energization which are summarized in Table-3. The simulation of transient inrush overvoltage waveforms during the switching of 15.0 Kvar step with load 80.0 kW reached 2.19 pu and frequency about 2.93 kHz as shown in Figure-7.

Table-1. Peak transient overvoltages when energizing the 0.415 kV, 50 kVAR capacitor banks in LV. Systems.

Capacitor banks steps	Capacitor steps in kvar	Capacitor switching sequences	Regulator switching program	Switching capacitor kvar	Peak line -to line voltage at 0.415 (kV)	
					(kV)	Per unit
1	5.0	5.0	1	5.0	0.677	1.63
2	5.0	5.0	1	10.0	0.678	1.63
3	10.0	10	2	15.0	0.904	2.17
4	15.0	30	3	30.0	0.925	2.22
5	15.0	Total =50	-	50.0	0.835	2.01

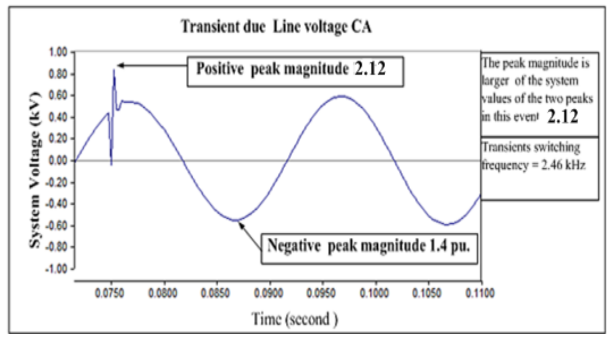

Figure-5. The pu. Peak voltage magnitude when switching the isolated capacitor bank in low voltage system (LV).

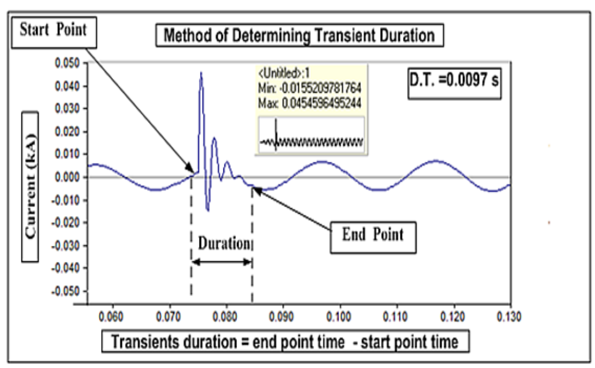

Figure-6. Transient duration during the energization of the isolated capacitor banks 0.415kV.

Figure-9 explains the pu transient overvoltage due to capacitor bank switching steps. Due to the large energy storage in the bank at the instant of steady state operation, the peak inrush current raises with the number of switching steps. Moreover, increasing the number of the steps increases the capacitance of the system which leads to lower frequency oscillations. While the lower inductance and capacitance will fast the magnitude of frequency. Therefore, the magnitude of oscillating voltage decreases due to the shared common voltage among the capacitor banks. Figure-8 explained the transient per unit in (kV) due to capacitor banks.

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Table-2. Simulation results of peak transient overvoltage when energizing capacitor banks by steps sequence.

Bank steps	Capacitor steps kVAR	Phase Voltage (kV)		per unit voltage	Frequency (kHz)	Duration of transients Time (s)
		Max. values	Min. values			
1	5.0	0.515	0.339	2.15	1.678	0.0006
2	10.0	0.472	0.339	1.97	1.468	0.0007
3	15.0	0.525	0.339	2.19	2.937	0.0003
4	30.0	0.512	0.340	2.13	2.349	0.0004
5	50.0	0.508	0.342	2.12	1.958	0.0005

Table-3. Transient overvoltage steps at different loads.

Capacitor steps(kvar)	5.0kvar		10.0 kvar		15.0 kvar		30.0 kvar		50.0 kvar	
Bank load (Kw)	Voltage (kV)		Voltage (kV)		Voltage (kV)		Voltage (kV)		Voltage (kV)	
	Phase voltage	Per unit volt.	Phase volt.	Per unit volt	Phase volt	Per unit volt	Phase volt	Per unit volt	Phase volt	Per unit volt
10	0.559	1.93	0.470	1.51	0.557	1.86	0.536	1.73	0.518	1.67
20	0.529	1.71	0.460	1.48	0.538	1.73	0.522	1.68	0.509	1.64
30	0.502	1.62	0.450	1.45	0.520	1.67	0.511	1.65	0.501	1.62
40	0.477	1.54	0.441	1.42	0.504	1.62	0.499	1.61	0.493	1.59
50	0.456	1.47	0.432	1.40	0.488	1.57	0.489	1.58	0.487	1.57
60	0436	1.41	0.424	1.37	0.474	1.53	0.478	1.54	0.480	1.55
70	0.419	1.35	0.416	1.34	0.461	1.49	0.469	1.51	0.473	1.52
80	0.403	1.30	0.408	1.32	0.449	1.45	0.460	1.48	0.467	1.51

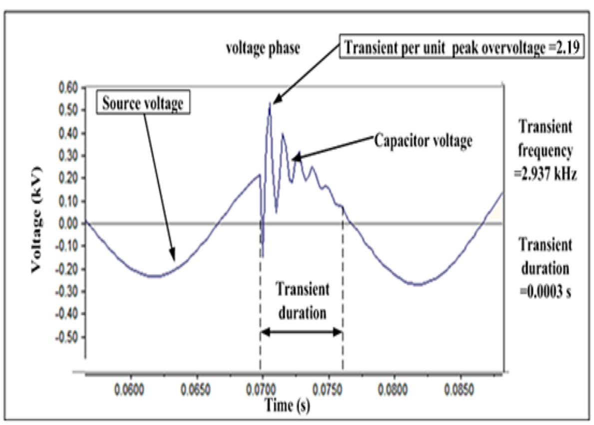

Figure-7. Step 3 Transient inrush over voltages when energizing 15.0 Kvar with load 80.0kilowatt.

With the energizing of the isolated capacitor banks without the proposed high pass filter, the calculated waveforms of the transient overvoltage and harmonic orders are presented in Table-4 and the block diagram in Figure-9. It is also clear that the transient overvoltage can rise to 395 V and the 3rd order harmonic is 0.0591 for phase voltage.

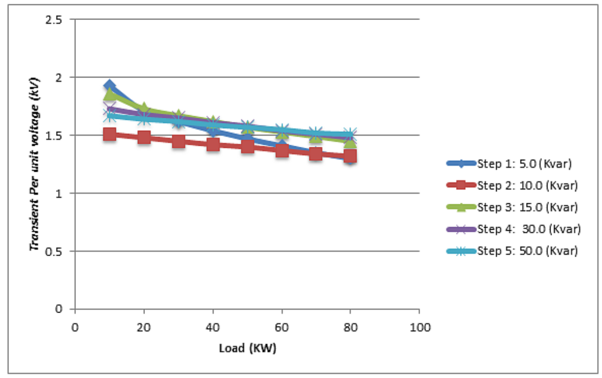

Figure-8. Transient over voltages due to capacitor bank steps.

It is clear that the degree of transient overvoltage harmonic order for the simulation outcome has been significantly minimized to 364 V, and 3rd.order harmonic is 0.049 respectively. Table-5 and Figure-10 illustrate the situation, after controlling the switching transients, with the application of the high pass damping filter.

Table-4. Transient overvoltage and harmonic order without insertion of the high pass damping filter.

Harmonic order	Magnitude(%of fundamental	Maximum oscillating voltage (kV)
1	100%	0.395
2	1.12	
3	5.31	
4	3.58	
5	2.86	
6	2.722	
7	3.60	

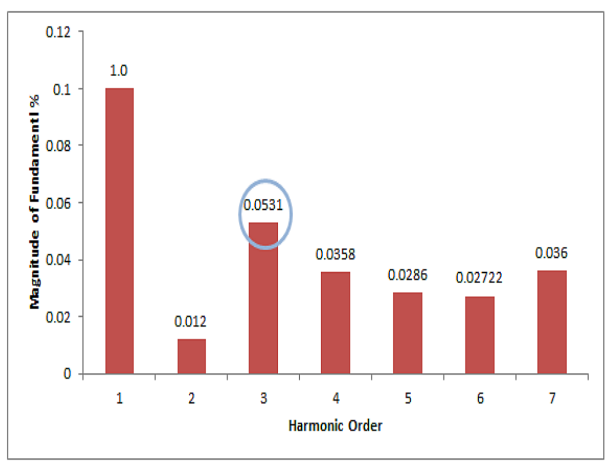

Figure-9. Transient's overvoltage and harmonics order without insertion of high pass damping filter.

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Table-5. Transient's overvoltage and harmonics order with insertion high pass damping filter**.**

Harmonic order	Magnitude(%of fundamental	Maximum oscillating voltage (kV)
1	100%	0.364
2	1.04	
3	4.93	
4	3.34	
5	2.67	
6	2.55	
7	3.37	

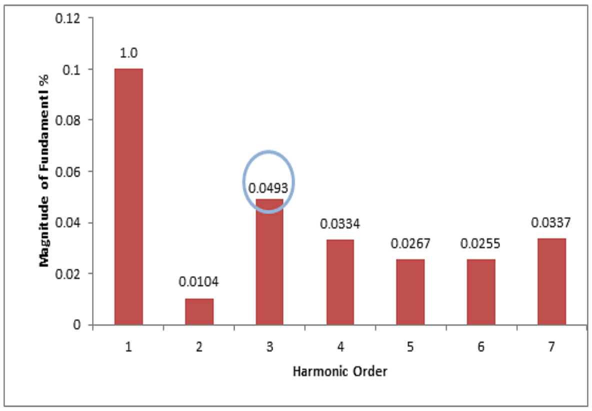

Figure-10. Transient's overvoltage and harmonics order with insertion high pass damping filter.

CONCLUSIONS

There are several considerations involved in the mitigation of transients generated by capacitor banks. As the initial peak of the capacitor switching transients normally causes most of the damage following the energizing, there is a need to choose a suitable limiting device to reduce these transients to the levels that can be accepted. This study has proposed the theoretical analysis and simulation results to show how capable the proposed high pass damping filter is in restraining the capacitor switching transients. The suggested limiter has a simple configuration and there is no requirement to add any control circuit. The high pass damping can automatically be inserted into the circuit and give low impedance to minimize the switching transients following the energizing of the capacitor. Harmonic filtering is the best way to eliminate this distortion from the power system. High Pass Filter (HPF) represented the optimum solution to distortion problems created by transient switching of capacitor banks. Pre-insertion high pass damping filter offers a cost-effective solution for reducing capacitor switching transients. Filter circuit offers a low impedance route to reduce harmonic distortion to required levels.

The simulation results have confirmed that the proposed high pass damping filter can effectively cope up with the transient phenomena, without affecting the performance of the capacitor in the steady state.

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