



DEVELOPMENT OF A GATE DRIVE WITH OVERCURRENT PROTECTION CIRCUIT USING IR2110 FOR FAST SWITCHING HALF-BRIDGE CONVERTER

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ABSTRACT

This paper presents a gate drive with overcurrent protection circuit using IR2110 for MOSFETs and IGBTs, which have fast switching capability and simple control scheme. The proposed gate drive circuit is able to achieve fast switching thanks to high speed operation devices with lower reverse recovery time. Apart of fast switching operation capability, an overcurrent protection circuit is also implemented for the power switches, hence ensuring reliability and high robustness of the proposed circuit. This paper also evaluates a dead-time circuit that is used to prevent commutation problem during high side and low side switches transitions. The advantages of the proposed gate drive circuit are; it is capable to drive two power switches using a single driver circuit, while providing an isolation between high side and low side power switches. A test prototype circuits for a single-phase half-bridge DC to AC converter with the proposed gate drive circuit was developed to investigate its operation and behaviour. Experimental results are shown to verify the effectiveness of the proposed circuit.

Keywords: Gate drive circuit, IR2110 and overcurrent protection circuit.

INTRODUCTION

The demand for reliable and high robustness gate driver for power switches is increasing worldwide [1]. It is concomitant with the development of power electronics domain which plays important role for technological enhancement [2]. Most of the conventional gate drive circuit utilize a direct connection between the pulse width modulation (PWM) signal and the gate terminal of the power switches. A lot of advantages such as high speed and high dv/dt immunity have been claimed. However, when dealing with high-power converters and motor drive applications, isolation is usually required for separation of low-voltage side from high-voltage side [1]. On the other hand, the conventional gate drive circuit do not provide a comprehensive protection due to the overcurrent or overvoltage faults, hence leads to gate drive components or power supply failure.

The implementation of gate drive circuit with overcurrent and overvoltage protection circuit have been presented in [6] and [7]. It provides excellent device switching performance with protection against induced coupled noise hence, limit the drain to source overvoltage and overcurrent. Unfortunately, the shoot through fault can still occur if the logic unit, driving circuit or power supply is malfunction. Another protection approach to solve the existing overcurrent and overvoltage protection problem in order to secure gate drive has been explicitly described in [8] complete with their advantages and disadvantage.

Other than that, in [8] the author proposed a standalone AC coupled gate drive built with normally ON Silicon Carbide (SiC) JFETs integrating protection functions against overcurrent and shoot-through faults. The proposed technique used a variation of the common RCD network in the output stage in order to reduce induced coupled noise at gate-to-drain interactions, hence

preventing overcurrent fault. However, such technique only offers to drive a single power switch for a single driver circuit.

From a technical viewpoint, due to the increase of switching frequency, and Si-based power devices (i.e: insulated gate bipolar transistors (IGBTs) and metal oxide semiconductor field effect transistors (MOSFETs)) are still major components of power electronic converters, considerable attempts are being made to develop a more straightforward approach for MOSFETs and IGBTs whilst providing low side and high side switches isolation, hence ensuring high robustness gate driver for the related power switches, i.e., by using over current and over voltage protection circuits.

Recent developments on gate drive circuit focused on the power loss but non on the comprehensive gate drive protection circuits [3] [4] [5] [9]. This paper focuses on the overcurrent protection for a gate drive circuit with minimized power losses. A gate drive with overcurrent protection circuit using IR2110 for MOSFETs and IGBTs, which have fast switching capability and simple control scheme is proposed. This can improve reliability and provide high robustness of the gate drive circuit. The overcurrent protection circuit is formed using a current transducer that is used to sense the overcurrent flow through the switching leg. Then, a high frequency comparator is used to compare the signal with a maximum current limit. It will shut down IR2110 driver circuit when the current exceed the maximum current limit. A prototype circuit demonstrates applicability of overcurrent and overvoltage protection of the proposed gate drive circuit. Among advantages of the proposed gate drive circuit are:

A single gate drive circuit with the capability to drive two power switches.



The circuit provides isolation between high voltage side and low voltage side of two power switches for half-bridge converter circuit.

PROPOSED GATE DRIVE CIRCUIT DESCRIPTION AND OPERATION

The proposed gate driver circuit of MOSFETs and IGBTs includes a number of protection features apart from the basic drive requirements such as overcurrent protection circuit. In order to simplify the implementation of this work, only the power MOSFETs are considered for experimental test rig.

Figure-1 shows circuit configuration of the proposed gate drive circuit using IR2110 with overcurrent protection circuit for MOSFETs and IGBTs whilst Figure-2 shows the pulse width modulation (PWM) generator and dead time control circuits. The proposed gate-drive circuit consists of a single International Rectifier IR2110 High and Low side driver, overcurrent protection circuit, PWM generator circuit and a dead time control circuit. The connection of the power MOSFETs for the high side and low side connection is as shown in Figure-3. The DC power supply for the gate drive circuit is isolated by using Murata Power Solution Isolated 1W Dual Output DC-DC Converters (NMA0515), resulting in the supreme isolation performance.

The operating principle of the proposed gate drive circuit is organized as: (A) IR2110 gate drive (B) overcurrent protection (C) PWM generator and dead time control and (D) power MOSFETs connection.

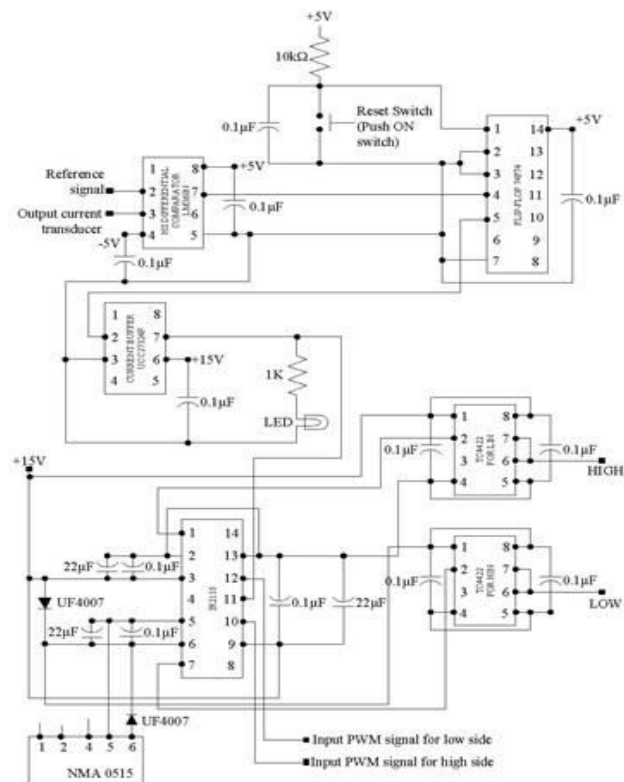


Figure-1. Proposed gate drive with overcurrent protection circuit.

IR2110 gate drive

An international Rectifier IR2110 high and low side driver device is the key element of the proposed gate drive circuit. This component presents features that are suitable for high speed power MOSFET control, such as: it has floating channel designed for bootstrap operation, while being able to withstand up to +500V or +600V. It is also immune to negative transient voltage dv/dt . Furthermore, it consists of a built-in logic input SD terminal for shutdown. The gate drive circuit can therefore be turned OFF simply by triggering the SD terminal. The high current buffer TC4422 is then connected to the IR2110 gate driver in order to provide noise immunity and to allow the device to be driven from slowly rising or falling waveforms. In addition, the use of TC4422 will also protect the gate drive circuit from any form of upset except direct overvoltage or over-dissipation.

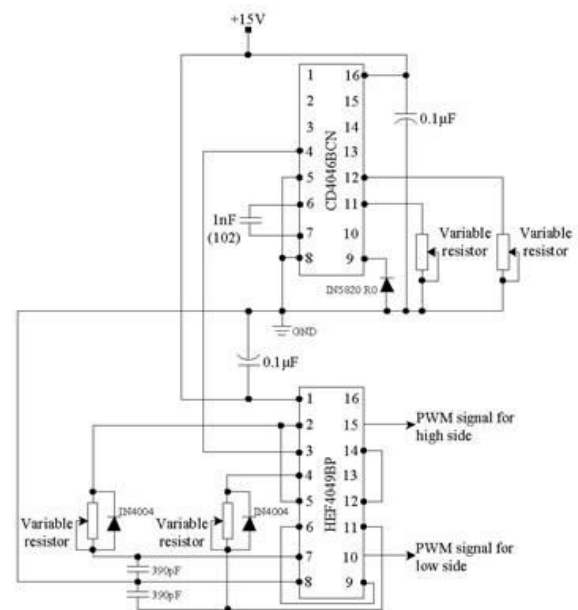


Figure-2. PWM generator and dead time circuit.

Overcurrent protection

Overcurrent protection circuit is provided to the proposed gate drive circuit using a high speed current transducer CSNT651 Honeywell, which is connected in series with the source terminal of the lower power MOSFET. Then, the output of the current transducer is connected to the high speed differential comparator LM360N. This device is used to compare the output signal from the current transducer with the maximum current limit, which is set as a reference signal. The LM360 will trigger when the value of sensed current exceed the maximum current limit that is defined by a reference signal (V_{ref}).

$$V_{ref} = \frac{I_M + 10\%}{N} \times R_M \quad (1)$$

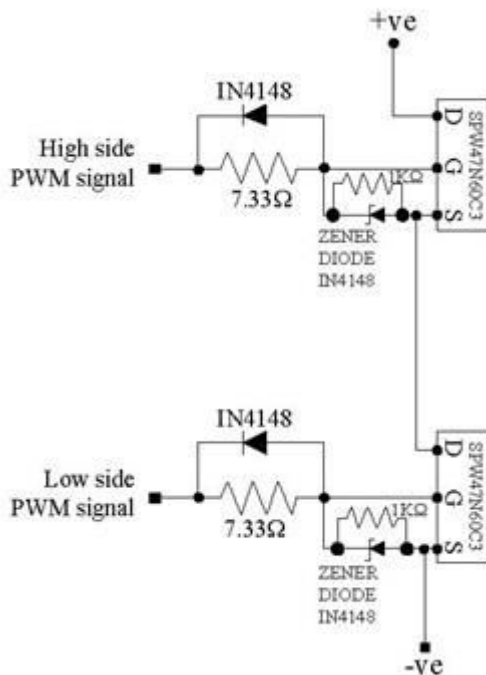


Figure-3. Power switches connection.

Where, I_M is the current flowing through the MOSFET, N is the current transducer turns ratio and R_M is the range of resistor for current transducer. The reference current can be set according to the equation (1). The output of LM360 is connected to the Dual D-Type Positive Edge-Triggered Flip-Flop 74F74 fed with a reset switch (push ON switch). The 74F74 is used to reset the triggered signal of LM360, which in turn, will further reset the SD terminal via UCC27324P. The UCC27324P is a high speed dual MOSFET drivers, which delivers a large peak currents into the capacitive loads. In this work, the push-ON switch is used as an input reset button of the 74F74 flip flop. When, the SD terminal of IR2110 device is triggered, the output signal at the LO and HO terminal will be cut OFF, resulting in the power switches to turn OFF. As a result, the power devices will be safe and protected.

PWM generator and dead-time control

The PWM signal is generated using CMOS Micropower Phase-Locked Loop CD4046B types device. An external components such as capacitor, diode and variable resistor are used to determine the required switching frequency. In this work, the PWM switching frequency of 20 kHz is generated by adjusting the variable resistor. The HEF4049B is used to split the PWM signal from CD4046B into two forms; PWM signal for HIN and PWM signal for LIN. On the other hand, the HEF4049B is also used to provide inverting buffers with high current output capability, which is suitable for driving TTL or high capacitive loads and to convert logic levels up to standard TTL levels with guaranteed fan-out into common bipolar logic elements. Again, an external components such as capacitors and variable resistors are used to control the dead time of the PWM signal between the HIN and LIN.

The dead time can be easily control by adjusting the variable resistor. The generated PWM signal with a dead time is then connected to the HIN and LIN terminal of the IR2110 gate drive circuit.

Power MOSFET connection

Figure-3 shows the Cool MOS Power Transistor SPW47N60C3 MOSFETs connection for the proposed gate drive circuit. A resistor of 7.3 Ω is used in series with each MOSFET gate terminal to damp any oscillation in the gate voltage and dynamic current sharing. A Zener diode 1N4148 is also connected in parallel with the 7.3 Ω resistor to speed up the voltage dissipation. In addition, both diode and resistor configuration also function to minimize delay time during switch turn OFF, hence prevent short circuit during high side and low side switches transitions. To further protect the power MOSFET gate, a 15 V, 0.4 W zener diode is connected across the gate and source terminals of each MOSFETs. This diode functions to stabilize gate-to-source voltage, V_{gs} , so that the voltage do not exceed +15 V, hence providing overvoltage protection to the power switches.

OVERCURRENT PROTECTION TEST-RIG

Implementation of overcurrent protection for the proposed gate-drive circuit uses a DC power supply to represent signal of the actual current sensor. The voltage of the DC power supply is slowly increased up to the level of the reference signal. Since the voltage of the DC power supply exceeds the reference signal, then comparator of LM360N will be triggered, hence the light emitting diode (LED) is turn ON to show that the overcurrent protection circuit was activated. Details on the process of shut down of the IR2110 gate drive PWM signal are as discussed in the previous sections.

EXPERIMENTAL RESULTS

In order to verify the proposed gate drive circuit, a test prototype circuit for a single-phase half-bridge DC to AC converter was developed to investigate the effectiveness of the proposed circuit as shown in Figure-4 and Figure-5. The dead time was set at $t_d = 1.4 \mu s$. A DC power supply of $V_s = 40V$ is connected to the source of the DC to AC converter with load resistor of 50Ω, to investigate the behaviour of the output voltage waveform, which is driven by the proposed gate drive circuit. Figure-6 shows the V_{gs} waveforms of the MOSFETs for the proposed gate drive circuit. It is observed that V_{gs} is immune to coupled noise and gate punch-through fault. The overshoots in V_{gs} is nearly eliminated. It is also shown that V_{gs} rise and fall times are 200ns and 118ns respectively. A close-up of the device turn ON and turn OFF transitions is presented in Figure-7. Figure-8 shows experimental input and output voltage waveforms of DC to AC converter including the high side and low side MOSFETs PWM signal. It is observed that the proposed gate drive circuit can drive two MOSFETs using a single



gate drive whilst providing voltage isolation between high side and low side power MOSFETs.

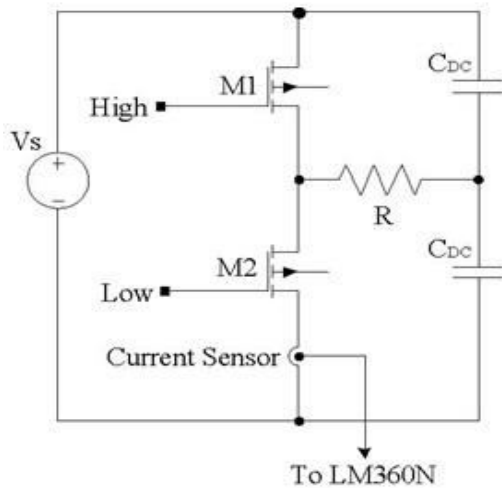


Figure-4. Test prototype circuits for a single-phase half-bridge DC to AC converter.

CONCLUSION AND FUTURE RECOMMENDATION

A gate-drive circuit using IR2110 with overcurrent protection for fast switching half-bridge converter has been presented. The operating performance and the circuit operation of the proposed gate-drive circuit has been discussed, and validated through experiments using MOSFET switching circuits. The proposed gate drive circuit offers possibility to provide overcurrent and overvoltage protection with high side MOSFET and low side MOSFET isolation, an obvious advantage compared to conventional gate drive circuits. The proposed gate drive circuit also presents fast rise and fall times, which are suitable for the next generation power converters composed of fast-switching, high-voltage power semiconductor devices, complete with comprehensive protection.

Future work may include the insertion of an optocoupler to a gate driver to provide an isolation between the electronics circuit with the power circuit.

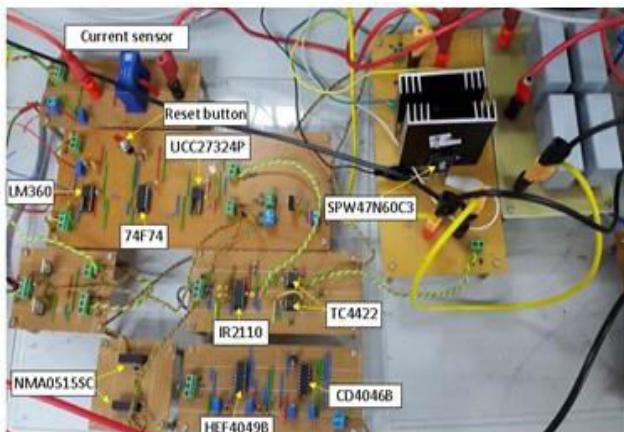


Figure-5. Experimental test rig.

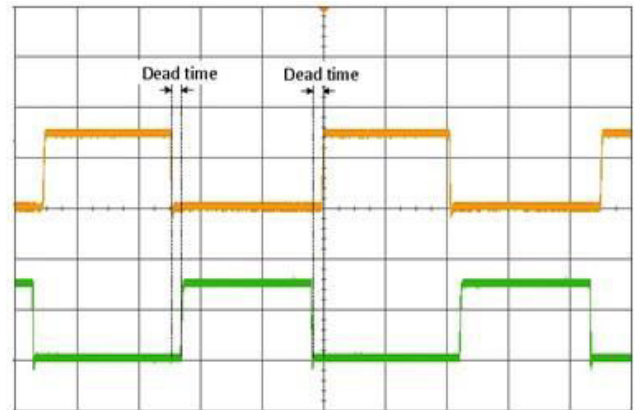


Figure-6. PWM signal at V_{gs} for switching frequency of 20 kHz. Scale: $V=10$ V/div, $t=10$ μ s/div.

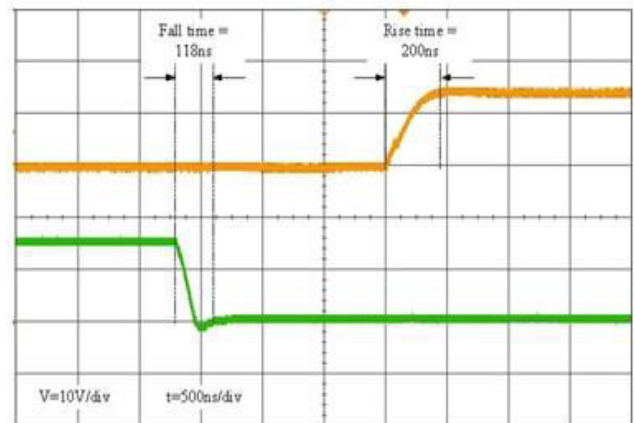


Figure-7. Rise and fall time of PWM signal at V_{gs} .

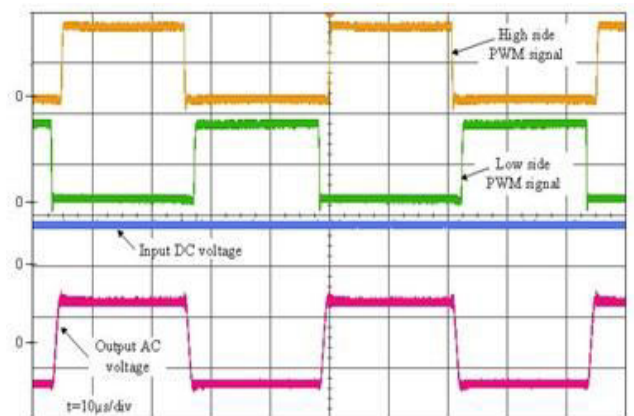


Figure-8. Input voltage and output voltage of DC to AC converter.

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