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DESIGN OF LOW POWER REVERSIBLE COMPRESSORS USING SINGLE ELECTRON TRANSISTOR

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ABSTRACT

Most of the multiplier circuits used adders in order to reduce the vertical critical path of the partial products. But adders will create many problems like glitches, uneven signal transition; and it will takemore number of steps to reduce the partial product reduction. To solve these problems, a special kind of adders that are capable to add four/six bits per decade. These adders are called compressors. The advantage of using compressors is to provide regular structure in reduction of partial product stage. The 4:2 and 6:2 compressors as processing elements (PEs) are the fundamental basic blocks for accumulating partial products during the multiplication process. In this paper, 4:2 and 6:2 compressors are designed on reversible logic using DKGP gate, one of the reversible gates and implemented in transistor level using Single electron transistor (SET). SET is considered to be popular in the field of nanoelectronics. It offers low power consumption and high operating speed. The developed compressors are simulated using SPICE software and the obtained results are compared with single electron transistor (SET) and the conventional CMOS. It is observed that the compressors using SET has considerable low power dissipation with conventional CMOS.

Keywords: 4:2 compressors, 6:2 compressors, reversible logic, DKGP gate, single electron transistor.

1. INTRODUCTION

Multiplication is a most fundamental operation in many of the signal processing algorithms and it is the most critical operation in every computational system [1]. Multipliers have large area and consume considerable power. Hence there is an impressing need for the design of good multipliers. The objective of a good multiplier is to provide a physically compact, good speed and low power consumption. There are many high-level optimization techniques available for Wallace Tree Multipliers [2].Multiplication process consists of three steps (i) Partial product generation (ii) Partial product reduction (iii) Final product computation [11]. Reduction of partial product stage will influence the performance of multiplier in terms of speed and power dissipation. Partial product reduction has high latencies because of long vertical path. Normally adders are widely used to reduce the vertical critical path. But adders will create problems like glitches, uneven signal transition; and it will take much number of stages to reduce the partial product reduction. To avoid all these problems, compressors are very much required to be implemented in the multiplier design [3][4]. Compressor is a combinatorial device which is mostly used multipliers to reduce operands while adding terms of partial products A typical (m:n) compressor takes m equally weighted input bits and produces n-bit binary number[5]. The architecture of the 4-2 and 6-2 compressor are developed on reversible logic and then analyzed using CMOS and SET.

2. SINGLE ELECTRON TRANSISTOR

Transistors have continuously minimized in size and increased in switching speed since their invention in 1947. The exponential pace of transistor evolution has led to a revolution in information acquisition, processing and communication technologies. And running over most digital applications is a single device structure - the field-effect transistor (FET). But as dimensions of the device approach the nanometre scale, quantum effects become increasingly important for device operation and conceptually different transistor structures may need to be adopted. A notable example of such a structure is the single-electron transistor, or SET. Though it is unlikely that SETs will replace FETs in conventional electronics, they should prove usefulness in ultra-low-noise analog applications. Moreover, because it is not affected by the same technological limitations as the FET, the SET can approach closely the quantum limit of sensitivity. It might also be a useful read-out device for a solid-state quantum computer.

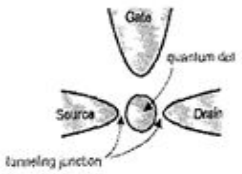

Figure-1. Schematic structure of SET [7].

The simplest device in which the effect of Coulomb blockade can be observed is the so-called single-electron transistor. It has of two electrodes known as the drain and the source, connected through tunnel junctions to one common electrode with low self-capacitance, known as the island. The electrical potential of the island can be tuned by a third electrode, known as the gate, coupled to the island through a capacitor. In the blocking state no accessible energy levels are within tunneling range of the electron on the source contact. All energy levels on the island electrode with lower energies are occupied.

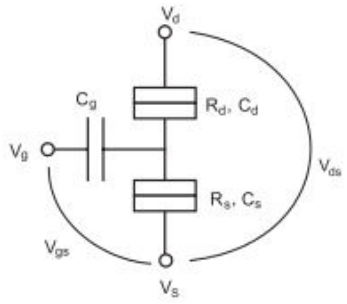

Figure-2. Equivalent circuit of SET.

When a positive voltage is applied to the gate electrode the energy levels of the island electrode are lowered. The electron can tunnel onto the island, occupying a previously vacant energy level. From there it can tunnel onto the drain electrode where it inelastically scatters and reaches the drain electrode Fermi level. Since it has controlled tunneling of single electrons across its junction, it operates at high speed. Since power consumption is proportional to number of electrons transferred across the junction, it consumes less power [6].

3. DKGP REVERSIBLE GATE

A 4* 4 reversible DKGP gate can work as a reversible Full adder and a reversible Fullsubtractor. It is shown in Figure-3(a). This can be verified that input pattern corresponding to a particular output pattern can be uniquely determined. The implementation of full adder and full subtractor from DKGP gate is shown in Figure-3(b) and 3(c), respectively. If the input A=0, the proposed gate performs as a reversible Full adder and if the input A=1, then it performs as a reversible Full subtractor[8].

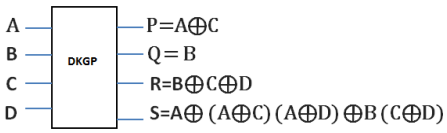

Figure-3(a).DKGP reversible gate.

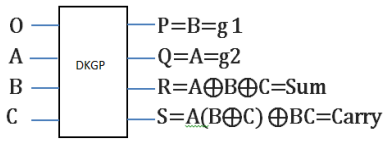

Figure-3(b). DKGP reversible full adder.

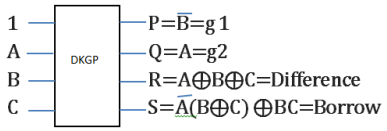

Figure-3(c). DKGP reversible full subtractor.

The proposed DKGP gate is implemented in transistor level using both CMOS and SET.

i. CMOS implementation of DKGP gate

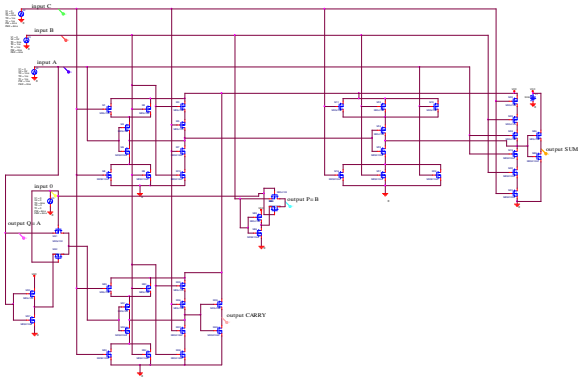

Figure-4. CMOS implementation of DKGP gate.

ii. SET implementation of DKGP gate

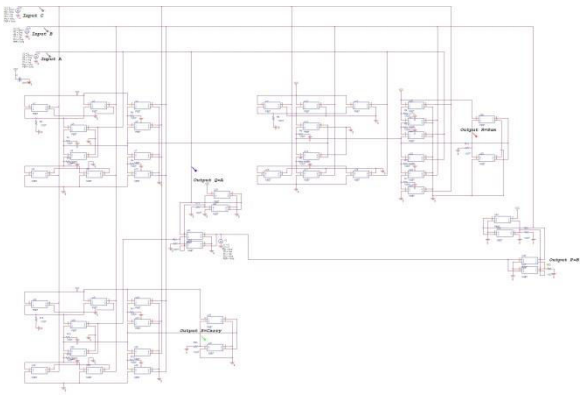

Figure-5. SET implementation of DKGP gate.

The DKGP gate using CMOS and SET is simulated in SPICE software. It is observed that the SET-DKGP consumes power lesser than CMOS-DKGP.

4. COMPRESSORS

i. Reversible 4:2 compressor

The 4-2 compressor has been widely employed in very fast multipliers for the construction of Wallace tree in order to lower the delay of the partial product accumulation stage [9][10]. The proposed reversible 4:2 compressor can be designed from two full adders using two DKGP gates by connecting the sum output of one full adder as an input to the second full adder. There are five inputs including carry in which is given to the second full adder then sum, carry and carry out outputs are obtained. Therefore four input bits compressed into two output bits.

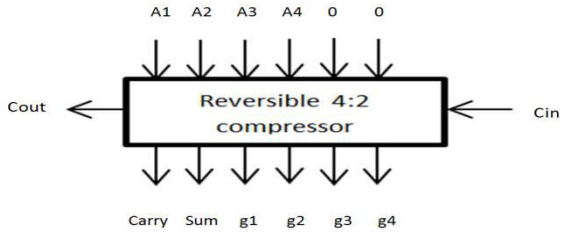

Figure-6. Block diagram of reversible 4:2 compressor.

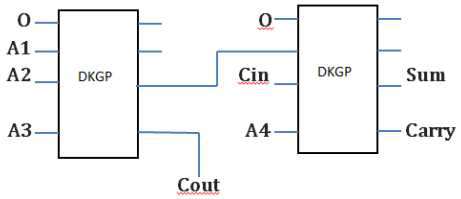

Figure-7. Proposed reversible 4:2 compressor from two DKGP gates.

ii. Reversible 6:2 compressor

Similarly in the same way, the reversible 6:2 compressor can also be designed from four full adders using four DKGP gates. The 6:2 compressor compresses 7 bits to 3 bits in which one of the inputs (carry in) is fed from neighbouring position j-1. The output of 6:2 compressors comprises of one bit in position j, second bit in j+1 and third bit in j+2.

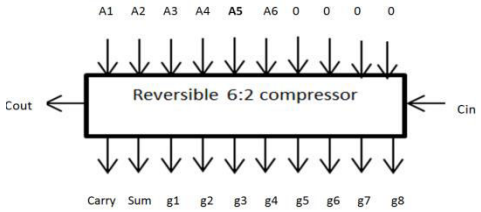

Figure-8. Block diagram of reversible 6:2 compressor.

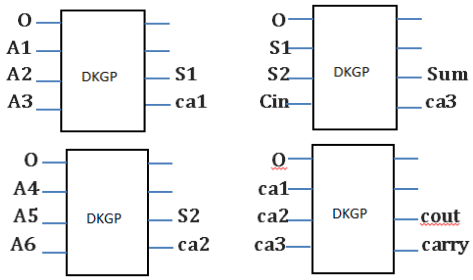

Figure-9. Proposed reversible 6:2 compressor from four DKGP gates.

5. SIMULATION RESULTS

The developed 4:2 and 6:2 compressors are simulated using SPICE software and the results are as follows:

i. CMOS 4:2 and 6:2 compressor

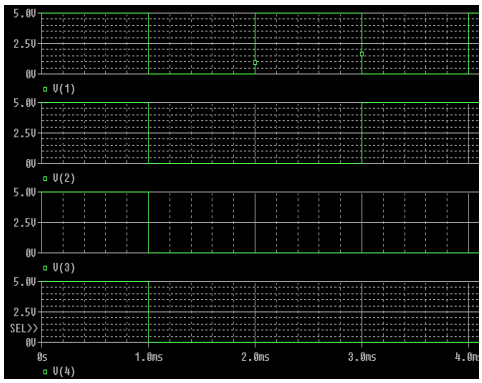

Figure-10. Input waveform for 4:2 compressor.

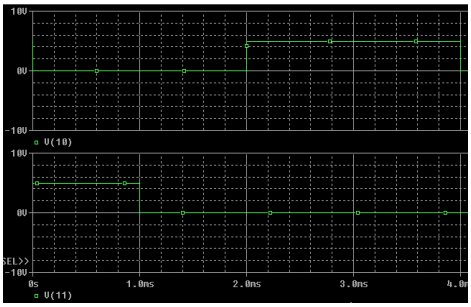

Figure-11. Output waveform for 4:2 compressor.

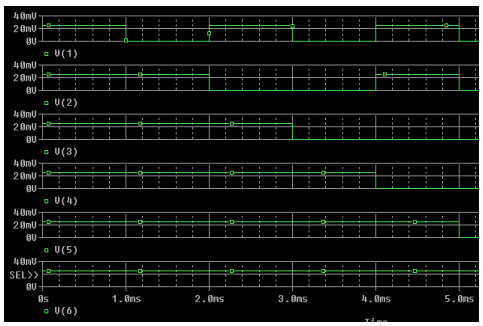

Figure-12. Input waveform for 6:2 compressor.

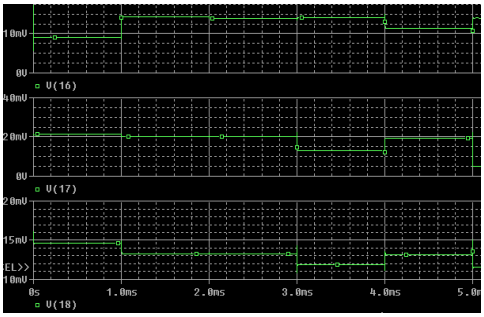

Figure-13. Output waveform for 6:2 compressor.

ii. SET 4:2 and 6:2 compressor

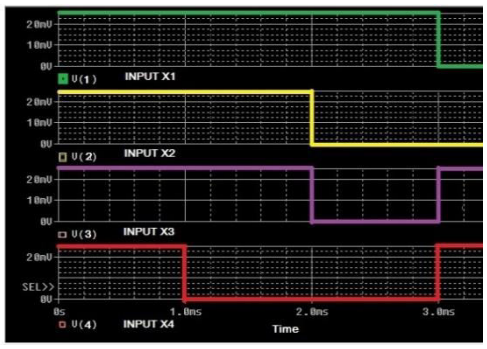

Figure-14. Input waveform for 4:2 compressor.

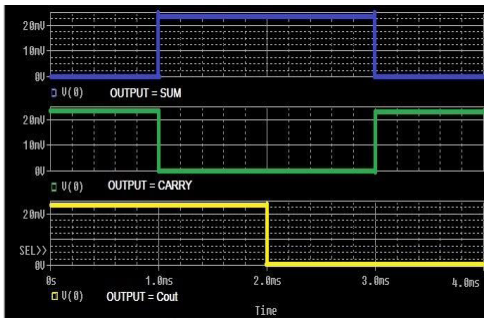

Figure-15. Output waveform for 4:2 compressor.

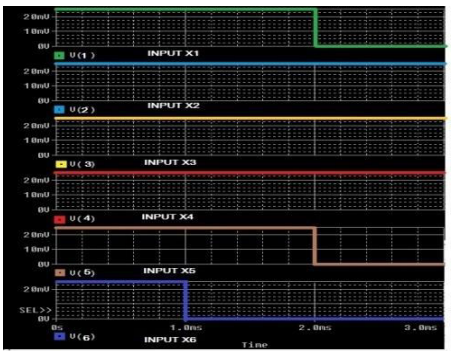

Figure-16. Input waveform for 6:2 compressor.

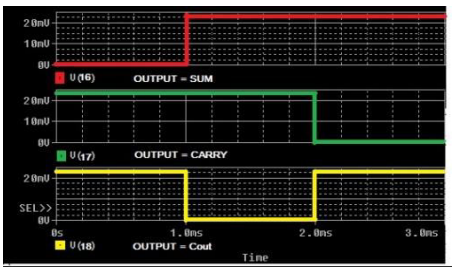

Figure-17. Output waveform for 6:2 compressor.

Table-1. Comparison of power dissipation between CMOS and SET.

	Power dissipation (in Watts)	
	CMOS	**SET**
DKGP gate	1.43mW	0.0075pW
AND gate	1.05mW	0.0021pw
4:2 compressor	2.86mW	0.016pW
6:2 compressor	5.72mW	0.03pW

6. CONCLUSIONS

The 4:2 and 6:2 compressors are designed to reduce the partial products in multiplication process. The results obtained using SPICE tool and it is observed that the single electron transistor performs efficiently and consumes low power compared to conventional CMOS. These nano compressors can cope up with nano processors in future. The scope of the paper is that these compressors can be used to develop high speed multipliers to reduce partial product delay.

REFERENCES

[1] Kiaml Z. Pekmestzi. 1999. Multiplexer-Based Array Multipliers. IEEE transactions on computers. 48(1).

[2] Naveen Kr. Gahlan, PrabhatShukla, JasbirKaur. 2012.Implementation of Wallace Tree Multiplier

Using Compressor.Int.J.Computer Technology and Applications. 3(3): 1194-1199.

[3] OklobdzijaV.G., D. Villeger S.S. Liu. 1996. A method for speed optimized partial product reduction and generation of fast parallel multipliers using an algorithmic approach. IEEE Trans. Comput. 45: 294-306. DOI: 10.1109/12.485568.

[4] Dandapat A., P. Bose, S. Ghosh, P. Sarkar and D. Mukhopadhyay. 2007. Design of an application specific low-power high performance carries save 4-2 compressor. Proceedings of the IEEE VLSI Design and Test Symposium. (DTS' 07) pp. 360-360.

[5] S.BSukhavasi, S. B Sukhasavi, V. B Madivada, H. Khan and S R S Kalavakolanu. 2012. Implementation of low power parallel compressor for multiplier using self resetting logic. International Journal of Computer applications. 47(3).

[6] VinayPratap Singh, Arun Agrawal, ShyamBabuSingh. 2012. Analytical discussion of single electron transistor. International Journal of Soft Computing and Engineering (IJSCE), ISSN: 2231-2307, 2(3).

[7] Konstantin k. Likharev. 1999. Single- electron device and threir applications. Proc. IEEE. 87: 606-632.

[8] D. Krishnaveni, 1 2M. GeethaPriya and 3K.Baskaran. 2012. Design of an Efficient Reversible 8x8 Wallace Tree Multiplier. World Applied Sciences Journal. 20(8): 1159-1165.

[9] M. Alioto and G. Palumbo. 2002. Analysis and comparison on full adder block in submicron technology. IEEE Trans. Very Large Scale (VLSI) Syst. 10(6): 806-823.

[10] Sreehari Veera machaneni *et al*. 2007. Novel Architectures for High-Speed and Low-Power 3-2, 4-2 and 5-2 Compressors. International Conference on VLSI Design, IEEE.

[11] N. Ravi, A.Satish, Dr.T. Jayachandra Prasad, Dr. T. Subba Rao. 2011. A New Design for Array multiplier with Trade Off in power and Area. IJCSI. 8(3).