



IMPROVEMENT OF POWER QUALITY IN FACILITY SIDE USING MODIFIED UPQC (UNIFIED POWER QUALITY CONDITIONER)

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ABSTRACT

The main objective of this paper is to improve power quality in the facility side i.e. distribution side. For that we are implementing most recent FACTS device called Unified Power Quality Conditioner (UPQC). The unified power quality conditioner (UPQC) is a custom power device, which mitigates voltage and current-related PQ issues in the power distribution systems. The proposed topology helps to match the dc-link voltage requirement of the shunt and series active filters of the UPQC. The topology uses a capacitor in series with the interfacing inductor of the shunt active filter, and the system neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter. The average switching frequency of the switches in the VSI also reduces; consequently the switching losses in the inverters reduce. And also, the level of harmonics present in the distribution line gets reduced.

Keywords: power quality, THD, UPQC, series active filter, shunt active filter.

INTRODUCTION

Harmonic distortion (HD) is one of the main power quality problems frequently encountered by the utilities. The harmonic problems in the power supply are caused by the non-linear characteristics based loads. The presence of harmonics leads to transformer heating, electromagnetic interference and solid state device malfunction. Hence, it is necessary to reduce the dominant harmonics below 5% as specified in IEEE 519-1992 harmonic standard [1]. Harmonic amplification is one of the most serious problems. It is caused by harmonic resonance between line inductance and power factor correction (PFC) capacitors installed by consumers. Active filters for damping out harmonic resonance in industrial and utility power distribution systems have been researched. Rationally based, passive L-C filters were used to eliminate line harmonics in [2]-[4].

Hysteresis current control [6] is a method of controlling a voltage source inverter so that the output current is generated which follows a reference current waveform in this paper.

Generally, PI controller [7] is used to control the DC bus voltage of SAF. The PI controller based approach requires precise linear mathematical model which is difficult to obtain. Also, it fails to perform satisfactorily under parameter variations, non-linearity, and load disturbances. This paper proposes a fuzzy logic controller for D.C bus voltage control [8]. Computer simulations are carried out on a sample power system to demonstrate the effectiveness of the proposed approach in suppressing the harmonics.

This paper presents [13] the control of distribution static synchronous compensator (DSTATCOM) for reactive power, harmonics and unbalanced load current compensation of a diesel generator set for an isolated system. The control of DSTATCOM is achieved using least mean square-based adaptive linear element (Adaline). An Adaline is used to

extract balanced positive-sequence real fundamental frequency component of the load current and a proportional-integral (PI) controller is used to maintain a constant voltage at the dc-bus of a voltage-source converter (VSC) working as a DSTATCOM. Switching of VSC is achieved by controlling source currents to follow reference currents using hysteresis-based PWM control.

In this paper, [14] a fixed-switching-frequency closed-loop modulation of a voltage-source inverter (VSI), upon the digital implementation of the modulation process, is analyzed and characterized.

The sampling frequency of the digital processor is considered as an integer multiple of the modulation switching frequency. An expression for the determination of the modulation design parameter is developed for smooth modulation at a fixed switching frequency.

The variation of the sampling frequency, switching frequency, and modulation index has been analyzed for the determination of the switching condition under closed loop. It is shown that the switching condition determined based on the continuous-time analysis of the closed-loop modulation will ensure smooth modulation upon the digital implementation of the modulation process.

However, the stability properties need to be tested prior to digital implementation as they get deteriorated at smaller sampling frequencies. The closed-loop modulation index needs to be considered maximum while determining the design parameters for smooth modulation. In particular, a detailed analysis has been carried out by varying the control gain in the sliding-mode control of a two-level VSI.

Experimental tests performed on a three-phase bipolartransistor controlled-current PWM power modulator show that it can operate with near-sinusoidal currents at 60 Hz with a 360-degree power angle range. Because of its capability to operate with leading power



factor and good waveform, the PWM converter is a promising alternative to the thyristor Graetz bridge. [15]

Existing Circuit Diagram & Proposed Circuit Diagram

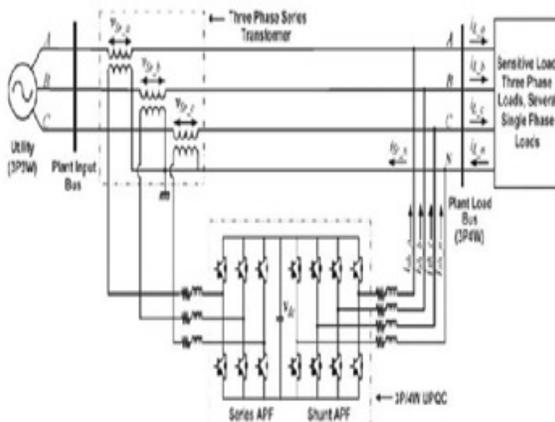


Figure-1. Existing circuit.

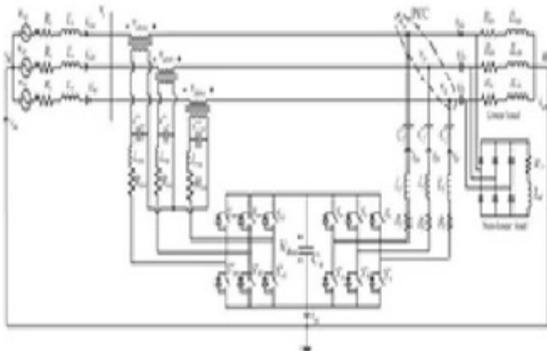


Figure-2. Proposed circuit.

Drawbacks of Existing System

- Conventional UPQC requires more rating of series and shunt active filters.
- Additionally to maintain the Low harmonics level by adding passive filters.
- The presence of harmonics will be more.
- In addition dc link capacitor has the high rating, the cost and size also bulky.
- Power Quality cannot be improved more.

PROPOSED TOPOLOGY

In case of the three-phase four-wire system, neutral-clamped topology is used for UPQC. This topology enables the independent control of each leg of both the shunt and series inverters, but it requires capacitor

voltage balancing. In, four-leg VSI topology for shunt active filter has been proposed for three-phase four-wire system.

This topology avoids the voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems associated with the four-leg topology, proposed a T-connected transformer and three-phase VSC based DSTATCOM. However, this topology increases the cost and bulkiness of the UPQC because of the presence of extra transformer. The topology consists of capacitor in series with the interfacing inductor of the shunt active filter.

The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously compensating the reactive power required by the load, so as to maintain unity power factor, without compromising its performance.

This allows us to match the dc-link voltage requirements of the series and shunt active filters with a common dc-link capacitor. Further, in this topology, the system neutral is connected to the negative terminal of the dc bus. This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables independent control of each leg of the shunt VSI with single dc capacitor.

In this topology, the system neutral has been connected to the negative terminal of the dc bus along with the capacitor C_f in series with the interfacing inductance of the shunt active filter. This topology is referred to as modified topology.

The passive capacitor C_f has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load.

The addition of capacitor in series with the interfacing inductor of the shunt active filter will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. The reduction in the dc-link voltage requirement of the shunt active filter enables us to match the dc-link voltage requirement with the series active filter.

This topology avoids the over rating of the series active filter of the UPQC compensation system. The design of the series capacitor C_f and the other VSI parameters have significant effect on the performance of the compensator.

This topology uses a single dc capacitor unlike the neutral-clamped topology and consequently avoids the need of balancing the dc-link voltages. Each leg of the inverter can be controlled independently in shunt active filter.



MODES OF OPERATIONS

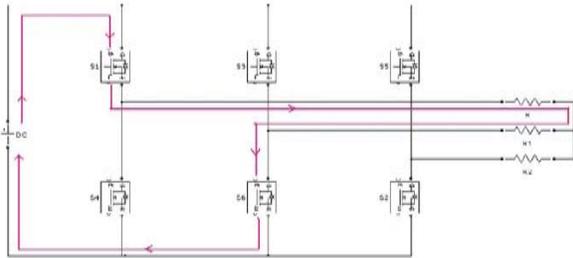


Figure-3. Mode 1.

During mode 1, Switches S1 and S6 conduct.

At that time, Phase voltage: $V_{an} = V_{dc}/2$, $V_{bn} = -V_{dc}/2$, $V_{cn} = 0$

Line voltage: $V_{ab} = V_{an} - V_{bn}$

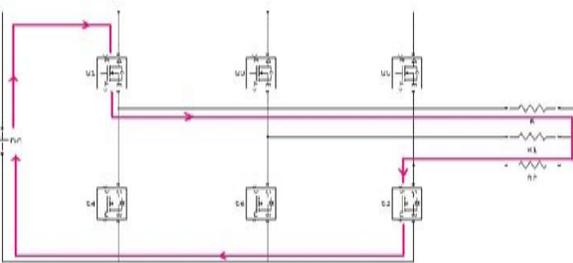


Figure-4. Mode 2.

During mode 2, Switches S1 and S2 conduct.

At that time, Phase voltage: $V_{an} = V_{dc}/2$, $V_{bn} = 0$, $V_{cn} = -V_{dc}/2$

Line voltage: $V_{ac} = V_{an} - V_{cn}$

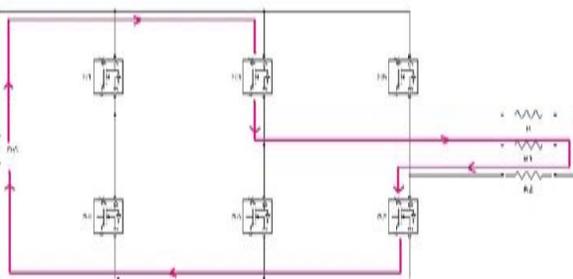


Figure-5. Mode 3.

During mode 3, Switches S2 and S3 conduct.

At that time, Phase voltage: $V_{an} = 0$, $V_{bn} = V_{dc}/2$, $V_{cn} = -V_{dc}/2$

Line voltage: $V_{bc} = V_{bn} - V_{cn}$

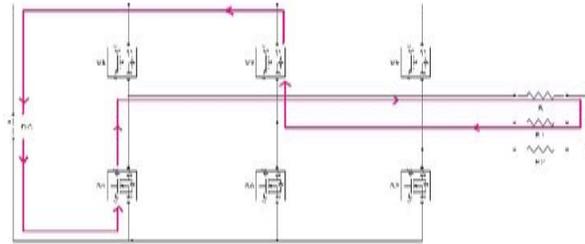


Figure-6. Mode 4.

During mode 4, Switches S3 and S4 conduct.

At that time, Phase voltage: $V_{an} = -V_{dc}/2$, $V_{bn} = V_{dc}/2$, $V_{cn} = 0$ Line voltage: $-V_{ab} = V_{an} - V_{bn}$

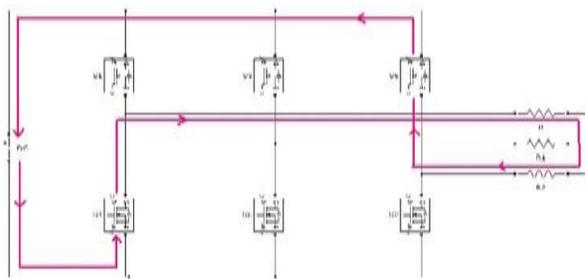


Figure-7. Mode 5.

During mode 5, Switches S4 and S5 conduct.

At that time, Phase voltage: $V_{an} = -V_{dc}/2$, $V_{cn} = V_{dc}/2$, $V_{bn} = 0$ Line voltage: $-V_{ac} = V_{an} - V_{cn}$

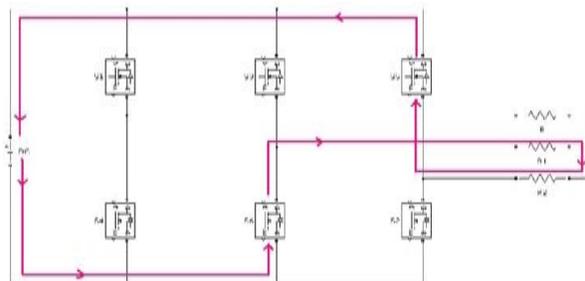


Figure-8. Mode 6.

During mode 6, Switches S5 and S6 conduct.

At that time, Phase voltage: $V_{an} = 0$, $V_{bn} = -V_{dc}/2$, $V_{cn} = V_{dc}/2$ Line voltage: $-V_{bc} = V_{bn} - V_{cn}$



SIMULATION OF UPQC

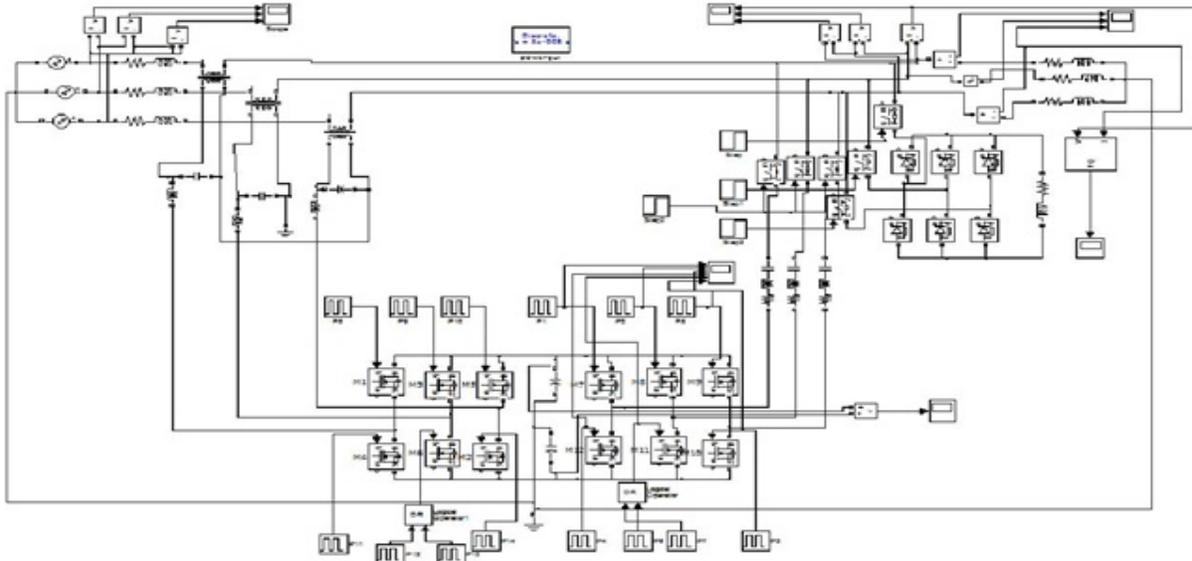


Figure-9. Conventional circuit diagram of UPQC.

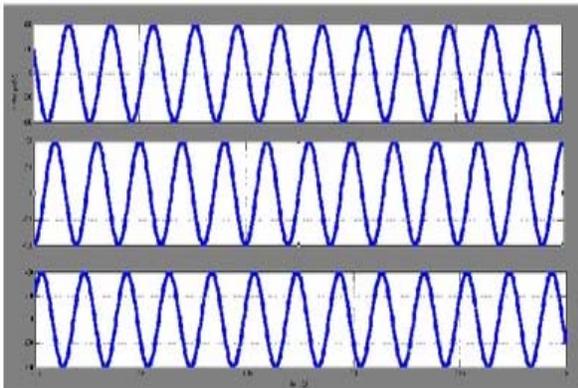


Figure-10. Three phase line voltage.

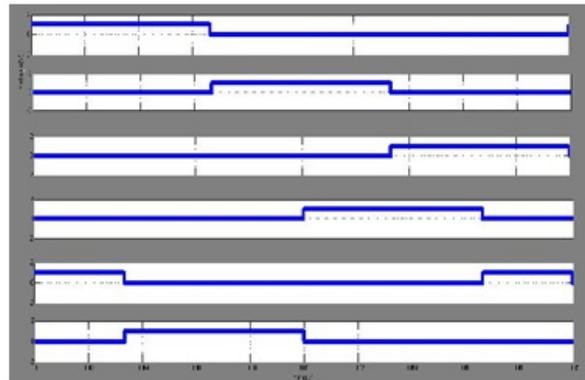


Figure-12. Triggering pulse.

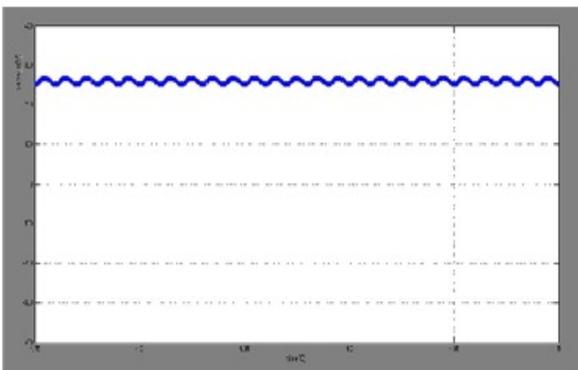


Figure-11. DC link voltage.

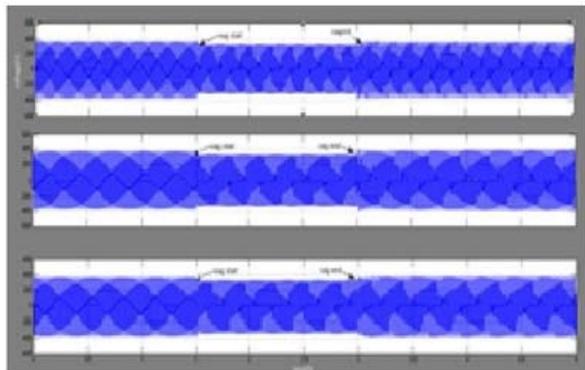


Figure-13. Three phase output voltage.

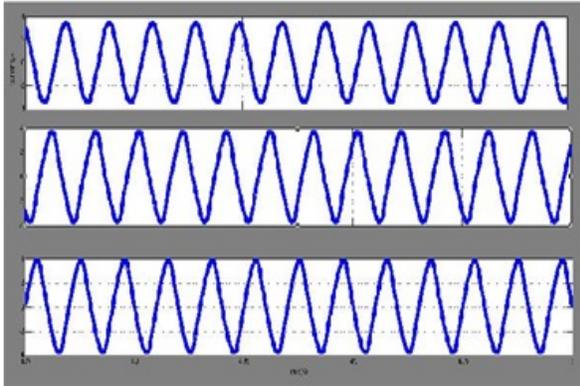


Figure-14. Three phase output current.

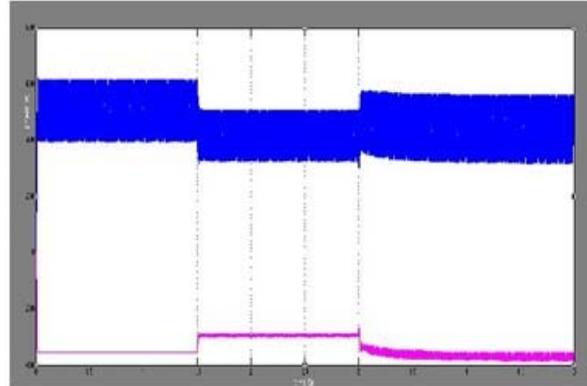


Figure-15. Power quality.

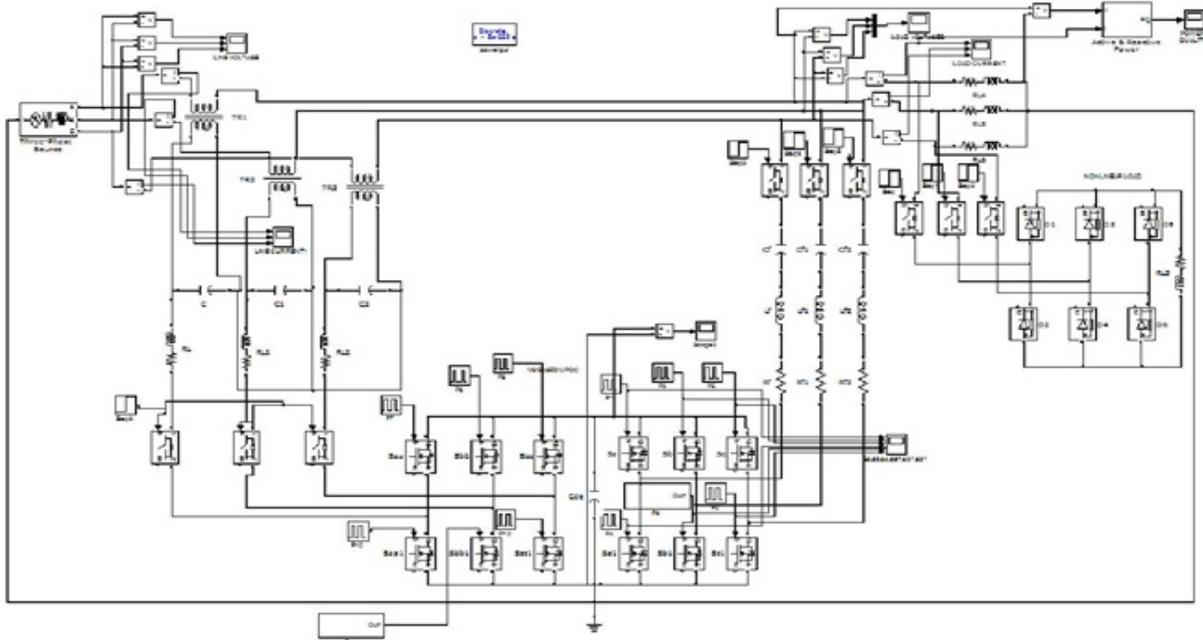


Figure-16. Proposed circuit diagram of UPQC.

Table-1. Input values for simulation.

System Quantity	Values
System Voltage	230 V (line to neutral), 50hz
Feeder impedance	1+3.141j ohm
Linear Load	$Z_{l_a} = 34+j47.5, Z_{l_b} = 81+j39.6, Z_{l_c} = 31.5+70.9$ ohm
Nonlinear load	3 phase rectifier
Shunt VSI	$C_{dc} = 2200$ micro F, $L_f = 26$ mH, $R_f = 1$ ohm
Series VSI	$C_{s2} = 80$ micro F, $L_{s2} = 5$ mH



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Table-2. Axis of the graph.

Parameter	X-axis	Y-axis
Three Phase Line Voltage	Time(sec) (0-0.05)	Voltage (V) (0-200)
Three Phase Line Current	Time(sec) (0-0.05)	Current (A) (0-10)
DC Link Voltage	Time(sec) (0-0.05)	Voltage (V) (0-100)
Three Phase Output Voltage	Time(sec) (0-0.5)	Voltage (V) (0-200)
Three Phase Output Current	Time(sec) (0-0.05)	Current (A) (0-5)
Power Quality	Time(sec) (0-0.5)	Power(W) (0-500)

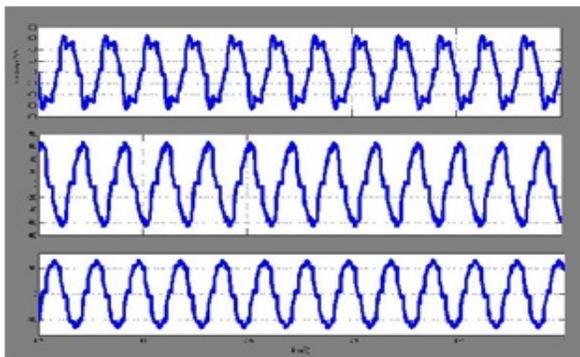


Figure-17. Three phase line voltage.

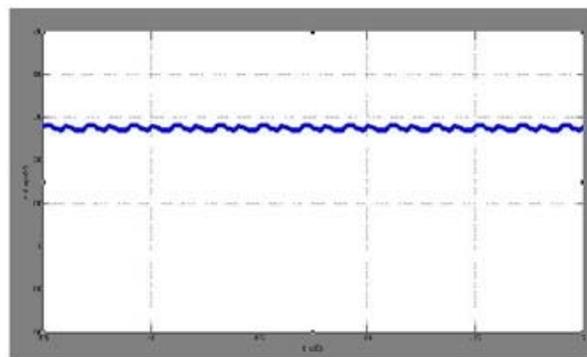


Figure-20. DC link voltage.

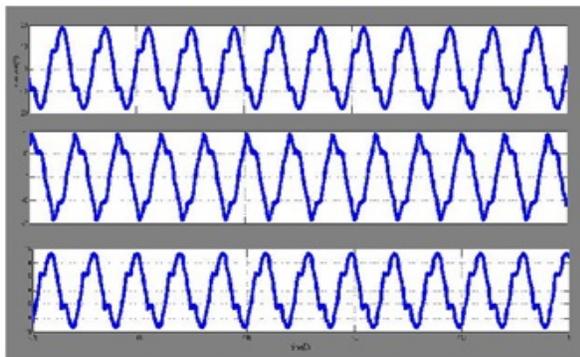


Figure-18. Three phase line current.

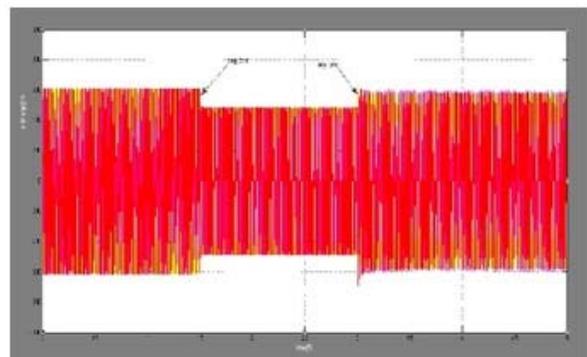


Figure-21. Three phase output voltage.

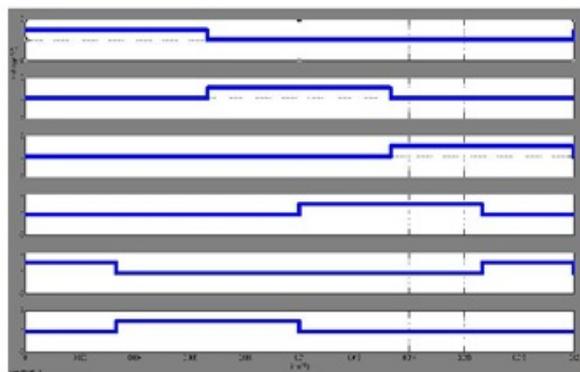


Figure-19. Triggering pulses.

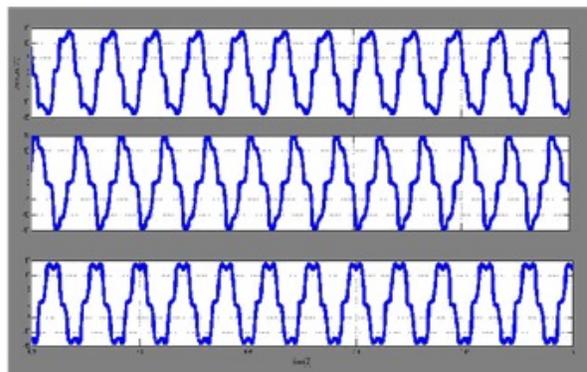


Figure-22. Three phase output current.

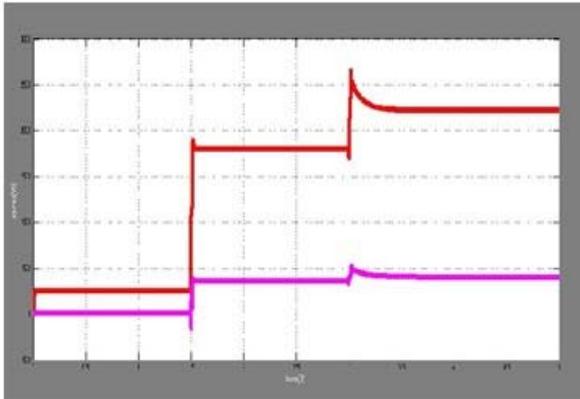


Figure-23. Power quality.



Figure-25. Photograph of hardware.

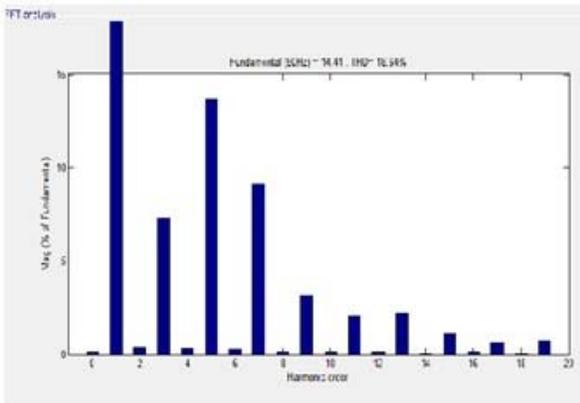


Figure-24. Total harmonic distortion.

Table-3. Total harmonic distortion comparison.

THD %	Without Compensation	Conventional Voltage	Modified Topology
i_{sa}	9.2	2.96	1.59
i_{sb}	11.7	3.20	2.19
i_{sc}	12.75	2.55	1.31
v_{la}	5.99	1.48	1.12
v_{lb}	5.86	1.59	1.24
v_{lc}	6.17	2.10	1.58

Total Harmonic Distortion is the total amount of harmonics present in the circuit. In our proposed system the present of total harmonic in the circuit can be studied by the help of the THD. The presence of various levels in the harmonics can we get from the help of the simulation. The harmonics analysis is the best tool to determine the power quality in the circuit. So by the analyzing amount of harmonics in the circuit, the design of circuit parameters can be easily determine.

CONCLUSIONS

A modified UPQC topology for three-phase four-wire system has been proposed, which has the capability to compensate the load at a lower dc-link voltage under non stiff source. The proposed method is validated through simulation and experimental studies in a three-phase distribution system with neutral-clamped UPQC topology (conventional). The proposed modified topology gives the advantages of both the conventional neutral-clamped topology and the four-leg topology. Detailed comparative studies are made for the conventional and modified topologies. From the study, it is found that the modified topology has less average switching frequency, less THDs in the source currents, and load voltages with reduced dc-link voltage as compared to the conventional UPQC topology.

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