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CERTAIN INVESTIGATIONS AND THE COMPARATIVE ANALYSIS ON THE DELAY LOGIC USED FOR COMPLEX ADDERS AND MULTIPLIERS FOR THE REDUCTION OF STATIC POWER CONSUMPTION

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ABSTRACT

For the full custom ASIC design, it is mandatory that every part of the system consideration has to be fulfilled with all the design specifications. In this delay in the complex circuits is an important aspect that has to be considered. In this paper, a comparative study and analysis of constant delay (CD) logic and the static logic is performed for various adders. This logic can also be applied for the CORDIC algorithm circuit that minimizes the delay in the circuit. The CD logic works with the pre-evaluated outputs that are much before the inputs that are fed to the respective stage. This gives an advantage over different styles of design when it comes for the multistage blocks. This control over the delay in the logic helps in the reduction of static power consumption at the different levels. Thus a power controlled design is also achieved along with the reduced delay. A comparative analysis of CD and static logic is been performed for different kind of adders like half adder, full adder, 16 BIT ripple carry adder and 16 BIT Wallace tree multiplier. The analysis is carried out in 120nm technology with frequency as 500 MHz and at a temperature of 450C.

Keywords: constant delay logic, static logic, multipliers, pre-evaluated outputs.

INTRODUCTION

Today's increase in demand of portable devises led to the increase of low power consumption of the devices with the decrease of delay in the computation keeping the efficiency high for the performance factor. There are multiple ways to attain the low power consumption. They include 1. Power reduction with the efficient design techniques/logic of the circuit. They often work on the clock & bus of the circuitry. They also include in minimizing the switching activity and swing. 2. Power reduction by efficient architectural design [6]. They emphasize on the power management techniques that could work on the whole of the block. Some of the techniques like pipelining, parallelism also fall into it. 3. Power reduction through process technology [7]. It deals with the device characteristics for low voltage operation and also reduced effect of capacitance with scaling. 4. Power reduction through appropriate algorithm selection that are used to minimize the number of operations and the number of hardware used. Coding with reduced number of registers or blocks can lead a way for this. 5. Power reduction through system integration. This involves with the usage of less global clocks. It is also important to consider the synchronization of the devices by appropriate selection of peripherals that are to be integrated with the main circuitry.

Among the different styles in the designing of circuits, the compound domino logic where it takes the advantage of swinging between static and dynamic gates has been popular in the designing of complex circuitry especially where the high performance is an unavoidable factor. Many advanced researches have been made on this by exploring the various logical optional that can extend the limitations offered by this. Some of them include source-coupled logic which offers the best performances but has higher power dissipation. Pseudo-n MOS logic is another high speed; low transistor count has very high static power dissipation with a less output voltage swing. The power dissipation of the VLSI circuits is mainly divided by static and dynamic power consumption. The reduced switching activity can yield greater control over dynamic power consumption but the main challenge is the control of static power as it is dissipated from the static circuits. In the usage of multiple circuits, it's often required to block certain parts for its non-usage. The power consumption during this period can cost higher for the low power engineers.

In this paper some of the traditional techniques like static & constant logic (CD) have been applied to multiple adders to find the comparative study of its delay and power components. It also found that by controlling the delay caused by the complex circuits we can control the static power that is been generated. It can be used further for memories and other devices like ADC or PACD where the inputs can be made random when the device is in use.

OPERATIONAL COMPONENTS OF CONSTANT DELAY LOGIC

The Constant Delay (CD) [1] Logic mainly works with the critical path for the carry generation. It also helps in reducing the power dissipation. It provides self reset advantage and the speed of the data that is been carried out. Here the delay not affected by the logic but rather based on the approximation of first order. This style can be integrated with the different logics as it doesn't require any complementary signals. CD logic works efficiently especially when the clock signals reached in

ahead of the input signals made to the circuitry. This logic often works under different temperature variations.

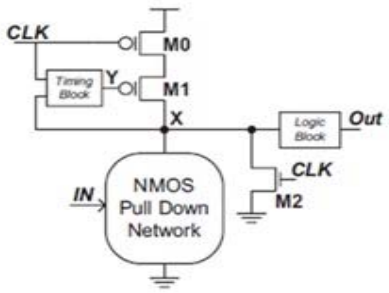

Figure-1. CD logic.

The static power is been controlled by the Timing Block which creates a timing period. The Logic block can be used to limit the unwanted glitches that are generated during the circuit operation. This block is also responsible for the cascading purpose. To achieve a better performance the logic block can be also replaced by the static gate instead of the inverted that is used in the conventional blocks, where the delay can be added extra by the usage of the inverter. Some of the other modifications also includes the implementation of different logic styles with respect to the design specifications can yield different results as per the requirements.

The operation of CD logic can be divided into four modes of operation [10] where the 1.Precharging is when the clock is high and during this the point X and the out are discharged and the VDD and the GND are in active mode. 2. Contention happened when the value of the IN enters the block for the evaluation purpose. During this a path is formed from the VDD to GND and the value of X becomes a nonzero voltage level and the OUT point will have a minor glitch. 3. CD delay, where the value of IN goes to low before the switching of CLK to low. At this point the value of X rises to high and the value of OUT is discharged to VDD. Then the delay is calculated from the CLK to OUT. 4. DQ delay where the IN goes to low after transition of CLK to low. Here the value of X enters to the contention mode and the raises to high. The delay is then calculated from IN to OUT. It is to be noted that the CD logic is to be operated on CD delay mode i.e the input arrive the logic which is earlier than the clock signal. The glitch that is generated temporarily during the contention mode can be minimized with the operation of the circuits at lower and constant temperatures. The CD logic dissipates the power during the contention mode or the when the value of X becomes '1'. This logic is still preferred because it is used in critical path where the power management techniques are used to control the power such as clock gating technique where the idle mode is blocked from the supply thus reducing the static power [9].

IMPLEMENTATION AND COMPARATIVE ANALYSIS OF CD LOGIC OVER ADDERS AND MULTIPLIERS

Adders play an important role in every block of a digital system. Each multipliers are formed from an adder with different constrain such as high speed, regularity in the output, less power consumption and also the area used by the transistors. There three stages in the designing of a multiplier, they are 1. The generation of partial products. 2. Its accumulation 3. The adding process. Any method of multiplication involves in adding and shifting procedure. In the parallel multipliers, the performance determinations are the number of partial products that is to be added with the main parameter. There are a numerous methods involved in the reduction of partial products. One of the major methods involved is Modified Booth Algorithm. In order to achieve the speed in the Wallace Tree algorithm [5], the number of stages that are added sequentially can be reduced. The concepts of parallelism, reduced shifts between the partial products and the sum ups in the internal stages will increase the speed.

The static logic is a steady state behavior [2] of a CMOS logic structures. It generates outputs as long as it receives the supply to the logic block. They generate a considerable logic delay that is normally caused in the block. Their characteristic includes low static power dissipation, high noise margin, no steady path between the supply and the ground points. Some of the negative characteristics are overcome by the CD logic like creating a steady path between VDD and the GND, high noise margin along with the benefits of low static power dissipation. These analyses are been implemented and verified from the following results.

Analysis on Half adder

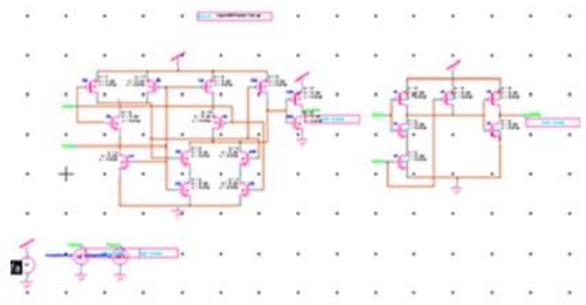

Figure-2. Block diagram of half adder in CD logic.

Table-1. Comparison with half adder.

Static Logic		CD Logic	
Parsing	0.00	Parsing	0.00
Setup	0.07	Setup	0.00
DC operating point	0.00	DC operating point	0.00
Transient Analysis	0.00	Transient Analysis	0.00
Overhead	2.58	Overhead	1.61
Total Delay	2.65	Total Delay	1.61
Power Dissipation	2.32Pw	Power Dissipation	1.96Pw

Analysis on Full Adder

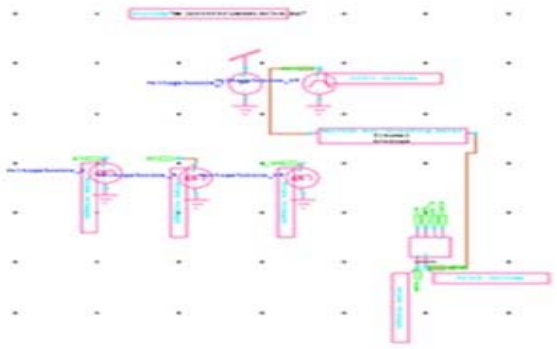

Figure-3. Block diagram of full adder in CD logic.

Table-2. Comparison with full adder.

Static Logic		CD Logic	
Parsing	0.00	Parsing	0.00
Setup	0.14	Setup	0.03
DC operating point	0.12	DC operating point	0.08
Transient Analysis	0.00	Transient Analysis	0.00
Overhead	2.93	Overhead	1.47
Total Delay	3.20	Total Delay	1.58
Power Dissipation	2.65Pw	Power Dissipation	2.13Pw

The Analysis is Carried out for 16 Bit Ripple Carry Adder

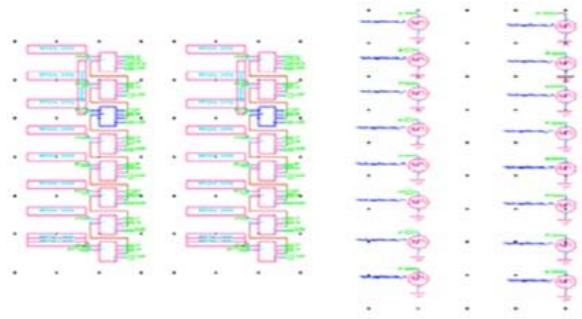

Figure-4. Block diagram of 16 bit ripple carry adder.

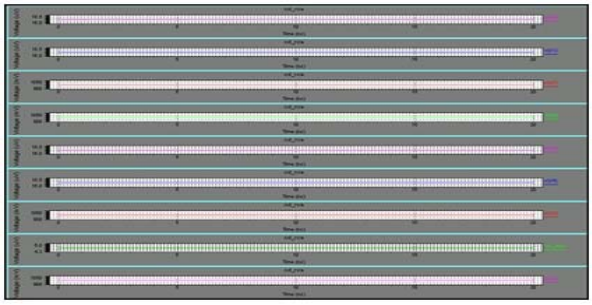

Figure-5. Waveform of 16 bit ripple carry adder.

The waveform which shows about the output functions of the 16 Bit Ripple Carry Adder. Where 1000 volt represents the "1's" and <1000 volts represents the "0's".

Table-3. Comparison with 16 bit ripple carry adder.

Static Logic		CD Logic	
Parsing	0.12	Parsing	0.02
Setup	1.10	Setup	0.50
DC operating point	8.56	DC operating point	5.34
Transient Analysis	2.52	Transient Analysis	1.34
Overhead	3.81	Overhead	2.61
Total Delay	16.11	Total Delay	9.81
Power Dissipation	13.3Pw	Power Dissipation	6.37Pw

The analysis is further carried out with the 16-bit Wallace tree multiplier. A Wallace tree works on a parallel processing. Here all the bits of partial products of each column are added by a group without any propagating carriers. Another group reduces the new set of values and further the process is carried on until a two set of matrix is formed. The final results are added using a carry propagation adder. In a high speed Wallace tree multiplier [3], a set of compressor adders and the modified carry select adder enables the parallel processing in an efficient manner. Here the compressor adder is used for partial product reduction and the addition of two rows in the final stage that are necessary for the reduction on carry propagation latency [8]. This type of Wallace tree multiplier is of higher speed with reduced power consumption than the normally used Wallace tree multiplier [4]. The analysis of the 16 bit Wallace tree multiplier with the static and CD logic is as follows.

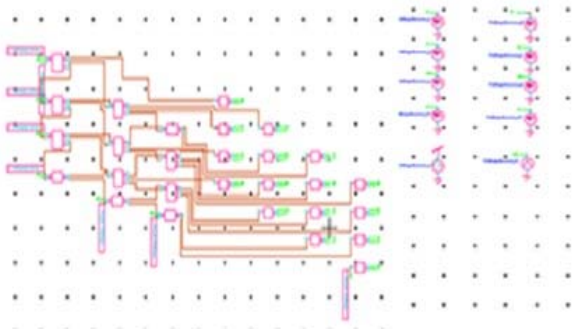

Figure-6. Block diagram of 16 bit Wallace tree multiplier in CD logic.

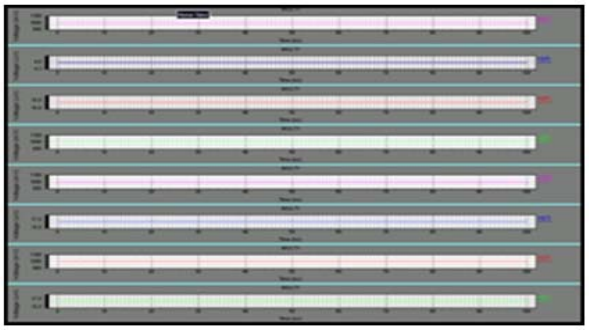

Figure-7. Waveform of 16 bit Wallace tree multiplier in CD logic.

The waveform which shows about the output functions of the 16 bit Wallace tree. Where, 1000 volt represents the "1's" and<1000 volts represents the "0's". The power analysis of Wallace tree multiplier in CD logic is as follows.

```
Power Results
vdd gnd from time 0 to 1e-007
Average power consumed -> 6.375912e-004 watts
Max power 6.375912e-004 at time 8e-008
Min power 6.375912e-004 at time 9e-008


* END NON-GRAPHICAL DATA
*

* Parsing                        0.02 seconds
* Setup                          0.50 seconds
* DC operating point             5.34 seconds
* Transient Analysis             1.34 seconds
* Overhead                       2.61 seconds
* ---------------------------------------------
* Total                          9.81 seconds

* Simulation completed  with  1 Warning
```

Figure-8. Results of power generated during the simulation.

Table-4. Comparison with 16 Wallace tree multiplier.

Static Logic		CD Logic	
Parsing	0.00	Parsing	0.00
Setup	0.16	Setup	0.11
DC operating point	0.38	DC operating point	0.25
Transient Analysis	0.38	Transient Analysis	0.28
Overhead	3.44	Overhead	2.33
Total Delay	4.36	Total Delay	2.97
Power Dissipation	3.74Pw	Power Dissipation	2.13Pw

It is analyzed from the implementation from the different logic devices that the CD logic yields better results than the static logic.

CONCLUSIONS

Efficient delay control CD logic has been implemented on basic adders and the couple of advanced multipliers. It is referred that the CD logic produces less delay in the circuit and also leads to reduce the static power that is consumed as compared to that of static logic. It is proposed that this logic can be further implemented in CORDIC algorithm which is a basic addition and shift operation and that are widely used in all the DSP applications.

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