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DESIGN OF MODIFIED RUSSIAN PEASANT MUTLIPLIER USING MSQRTCSLA BASED ADDER

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ABSTRACT

Multiplication and Accumulation (MAC) unit is recognized as high potential in every Digital Signal Processors (DSP). Multiplication is one of the essential operations every DSP applications such as Fast Fourier Transform (FFT), Digital Filters and so on. In this paper, Modified Russian Peasant Multiplier (MRPM) is designed through Very Large Scale Integration (VLSI) System design environment. The Russian Peasant Multiplier (RPM) is the best multiplication technique for improving their hardware performances. It makes the Partial Product Generation (PPG) process with the help of Multiplexers. Further Carry Select Adder (CSLA) is used in RPM based multiplier for reducing the hardware. However, still it required high speed MAC computational unit for up growing Fourth Generation (4G) based Wireless communication applications. To meet this requirement, MRPM based efficient multiplier is developed in this paper. In proposed MRPM, Modified Square Root Carry Select Adder (MSQRTCSLA) is used for performing addition operation. Further Reduced Wallace Tree Reduction (RWTR) is used in proposed design for simplifying the PPG results. Proposed MSQRTCSLA based MRPM multiplier offers 20.31% reduction in delay consumption and 61.31% reduction in power consumption than best existing Bi-Recoder based MAC unit.

Keywords: carry select adder (CSLA), multiplication and accumulation unit (MAC), digital signal processing (DSP), modified Russian peasant multiplier (MRPM), modified square root carry select adder (MSQRTCSLA), partial product generation (PPG), reduced wallace tree reduction (RWTG).

INTRODUCTION

Multiplication is an essential arithmetic operation in DSP application. The speed of DSPs largely depends on the multiplier block. This in turn increases the demand for high speed multipliers. Over the past few years, many researchers have developed various multipliers using several algorithms such as array, booth, Wallace tree and modified booth algorithms. The multiplier's speed usually determines the processor's speed. Multiplier is operated with a high degree of precision and reliability.

In Bi-Recoder multiplier, partial products are generated using multiplexer. Multiplexer is used to perform partial product generation process based on multiplier bit values. The partial product generation circuit of Bi-Recoder absolutely reduces the hardware complexity, delay and power consumption of multiplier. However, it utilizes large LUTs for storing the two-bit multiplication function.

Wallace Tree Reduction is mostly preferred for re-arranging the partial product generation. It reduces the complexity of bit products and provides two row matrixes. Finally an efficient adder is required to perform the addition operation. Wallace tree is not preferable in low power applications because of excess wiring usage that result in extra circuitry and increase in power consumption in the multiplier.

In this paper, Russian Peasant Multiplier is realized and re-constructed to increase the hardware performance. Hence, proposed structure is named as "Modified Russian Peasant Multiplier". Further Reduced Wallace Tree Reduction (RWTR) and Modified Square Root Carry Select Adder (MSQRTCSLA) is used for performing both PPG reduction and addition operation of proposed MRPM. The Proposed MSQRTCSLA based MRPM multiplier offers best performance in terms of latency and power consumption.

RELATED WORKS

Low-Power and Area –Efficiency Carry Select Adder has been explained in (B.Ramkumar and Harish M Kittur, 2012). In this paper, method of sharing the common resources is used to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. Area-Delay-Power Efficient Carry-Select Adder has been explained in (Basant Kumar Mohanty and Sujit Kumar Patel, 2014). In this novel, the CS operation is performed before the calculation of final-sum, which is different from the design of (B.Ramkumar and Harish M Kittur, 2012). Carry words corresponding to input-carry '0' and '1' generated by the CSLA based on the developed scheme follow a specific bit pattern, which is used for optimizing the CS unit.

The design of Hybrid Carry-Look ahead/ Carry-Select Adders have been described in (Yuke Wang, *et al*, 2002). In this article, a new implementation of high-speed 56-bit hybrid adder is introduced. The new adder generates the complement Ling's carries for CSAs to select the appropriate sums. Moreover, it directly implements group carry propagates and group carry generators without using

independent carry generator / propagate signals. The 16 bit carry select adder with low power and area has been explained in (Prof. Mary Joseph and Renji Narayanan, 2014). The simple and efficient gate level modification helps to reduce the area and power of CSLA. In this paper the proposed design of 16-bit regular SQRT CSLA (Dual RCA based SQRT CSLA) is compared with modified version of SQRT CSLA.

A Suggestion for a Fast Multiplier has been explained in (C.S. Wallace, 1964). The design is developed for a multiplier which generates the product of two numbers using purely combinational logic i.e., in one gating step. A Reduced complexity Wallace Multiplier Reduction has been briefly explained in (Ron S. Waters, *et al,* 2010). Wallace high-speed multipliers use Full Adders (FAs) and Half Adders (HAs) in their reduction phase. Half adders do not reduce the number of partial product bits. Therefore, minimizing the number of half adders used in a multiplier reduction will reduce the complexity.

Design and analysis of Bypassing Multiplier has been described in (M.Ahuja and Sakshi, 2013). The Braun's multiplier is one of the parallel array multipliers which are used for performing the unsigned multiplication. The dynamic power and delay of the Braun multiplier can be reduced by using the bypassing techniques i.e. 1-dimensional and 2-dimensional bypassing. Implementation of a High Speed Multiplier for High -performance and Low power Applications have been explained in (G Ganesh Kumar and Subhendu K Sahoo, 2015). In this paper, they propose a design of 8 and 16-bit multipliers using fast adders (carry save adder, Brent-Kung adder and Carry-select adder) to minimize the power delay product of multipliers intended for high-performance and low – power applications.

RUSSIAN PEASANT MULTIPLIER

Russian Peasant Multiplication (RPM) is actually a quick way to multiply the two 'n' bit multiplication. Russian peasant multiplier depends on multiplying and dividing by two. Russian Peasant Multiplier consists of Shifters, 2:1 Multiplexer and adder unit.

It is a simple architecture which consumes less area and delay for computation of multiplications. When compared to the Vedic multiplier, Russian Peasant Multiplier provides less APT (Area, Power and Time) product. RPM based multiplier gives the partial product results without help of FAs and HAs; instead it uses the multiplexers for generating the PPG results.

Architecture of 8-bit Russian Peasant Multiplier is shown in Figure-1. Similarly, 16-bit Russian Peasant Multiplier can be extended from 8-bit Russian Peasant Multiplier. In Figure-1, the Shifters and Multiplexers are used to find the partial product results which consume less area and power than Vedic multiplier. Further Wallace Tree Reduction is used in RPM based multiplier for reducing the complexity of PPG.

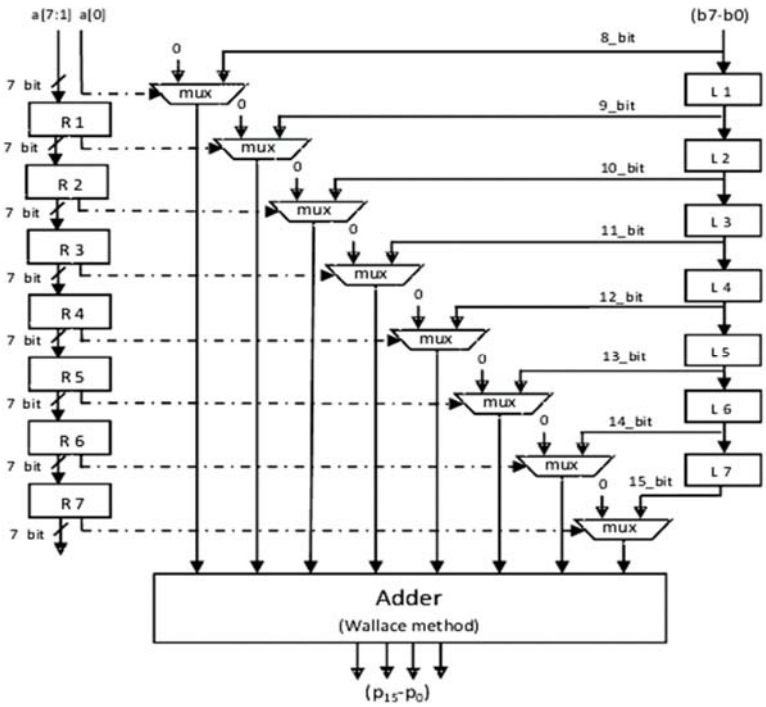

Figure-1. Architecture of 8-bit Russian peasant multiplier.

BI-RECODER MULTIPLIER

In Bi- Recoder Multiplier, partial products are generated using multiplexer. Based on the 2-bit Multiplier values, Multiplexer is used to perform the partial product generation process. The structure of Bi-Recoder Multiplier for generating partial product generation is illustrated in Figure-2. In Figure-2, the value of 'a' represents the multiplicand value and the value of 'b' represents Multiplier value. Multiplier bits are divided into four groups and each group having two bits. So, four set of multiplexer is needed to generate the partial products. If the value of b is "00" means, it passes simply 0 to the partial product generator else if it is "01" means it simply passes multiplicand value to the partial product generator else if it is "10" means it passes 1bit left shift of multiplicand value in terms of 10 bits else it is "11" means add the results of multiplicand and 1 bit left shift of multiplicand value.

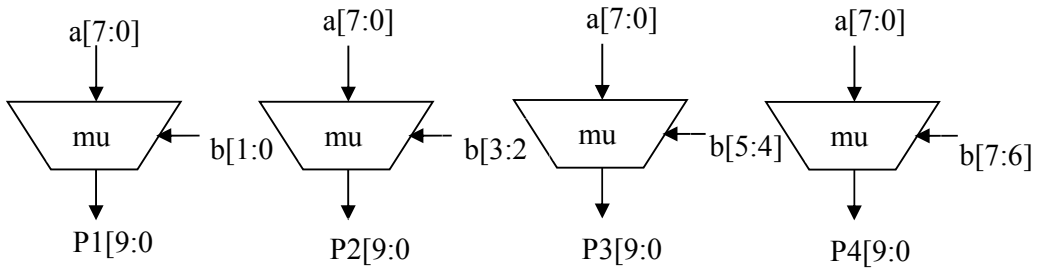

Figure-2. Partial product generation stage of Bi- Recoder multiplier.

REDUCED WALLACE TREE MULTIPLIER

A Wallace multiplier is a parallel multiplier which performs the array multiplication effectively. Array multiplier has more number of gates to perform multiplication. Hence, it occupies large area for computation. In order to overcome this problem, Wallace multiplier is preferred. The structure of reduced complexity Wallace multiplier structure is shown in Figure-3. The reduced complexity Wallace multiplier fewer HAs and FAs for performing multiplication function when compared to the traditional array multiplier. In the modified circuit, n^2 AND gates are used to form the partial products and they are arranged in an inverted triangle order. The matrix is divided into three row groups in the reduced complexity Wallace multiplier. For adding three bits, FAs is used. Single bit and a group of two bits are moved to the next stage directly. The end stage of Wallace multiplier, proposed SQRT CSLA is used instead of conventional SQRT CSLA for addition process. It reduces area as well as power.

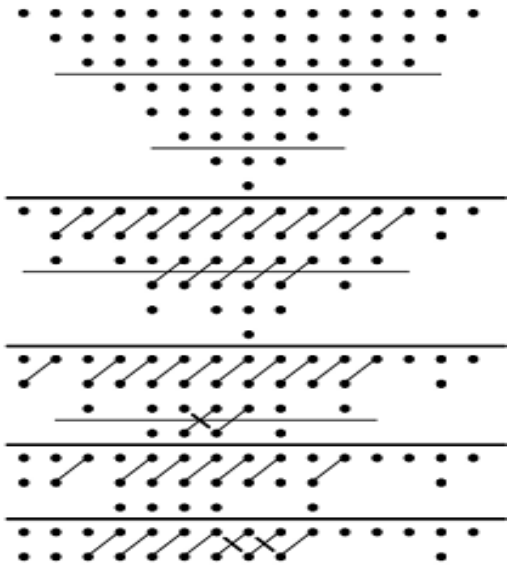

Figure-3. Structure of reduced complexity Wallace multiplier.

PROPOSED MODIFIED RUSSIAN PEASANT MULTIPLIER

In this paper, Modified Russian Peasant Multiplier is designed to improve the hardware performances of the circuit. Very Large Scale Integration (VLSI) System design environment is considered to implement the proposed design. The main consideration of VLSI System design is to reduce the hardware complexity, power consumption and to increase the speed and throughput of the system. Hence, the aim of proposed

work is reduce the delay and power consumption of multiplication.

In general, Multiplication function has three important steps:

- Partial Product Generation (PPG)
- Wallace Tree Reduction (WTR)
- Partial Product Addition (PPA)

In the place of PPG generation, MRPM circuit is developed in the proposed work. The architecture of proposed PPG generation by using MRPM has been illustrated in Figure-4. It gives 'n' rows of partial products using only 'Multiplexers'.

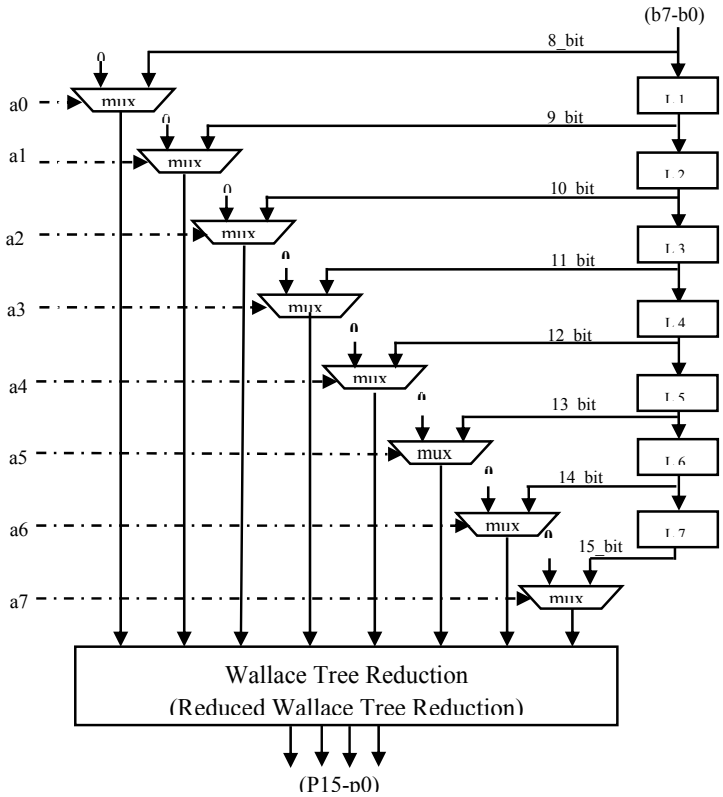

Figure-4. Proposed PPG generation by using MRPM.

To reduce the 'n' rows of partial product values into two rows, WTR methods have been used in general. But in the proposed MRPM structure, Reduced Complexity Wallace Reduction (RCWR) has been used (as shown in Figure-3). As shown in Figure-3, the final stage of RWTR requires an efficient adder (2*n-bit adder) to perform the addition process. In the place of addition part "Modified Square Root Carry Select Adder (MSQRTCSLA)" has been used in the proposed work. Hence, the proposed MAC unit named as MSQRTCSLA based MRPM.

In architecture of MSQRTCSLA (C. Uthayakumar and Dr. B. Justus Rabi, 2015), Reduced Half Adder (RHA) and Reduced Full Adder (RFA) is designed. In RFA and RHA design, four and two gates are reduced respectively than traditional ones. Further, the structure of RFA and RHA is incorporated into 16-bit Binary to Excess-1 Conversion (BEC) based SQRT CSLA for improving the hardware performance. The structure of RHA and RFA is shown in Figure-5(a) and Figure-5(b) respectively. The architecture of proposed MSQRTCSLA based MRPM has been illustrated in Figure-6.

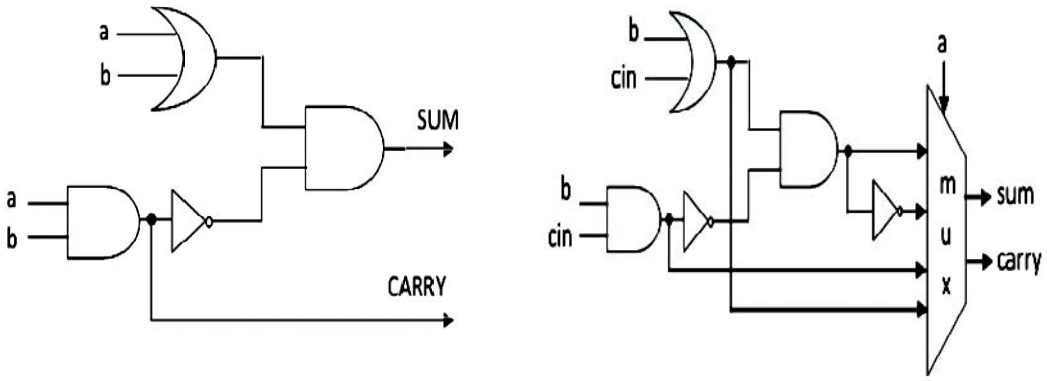

Figure-5. Structure of reduced half adder and reduced full adder.

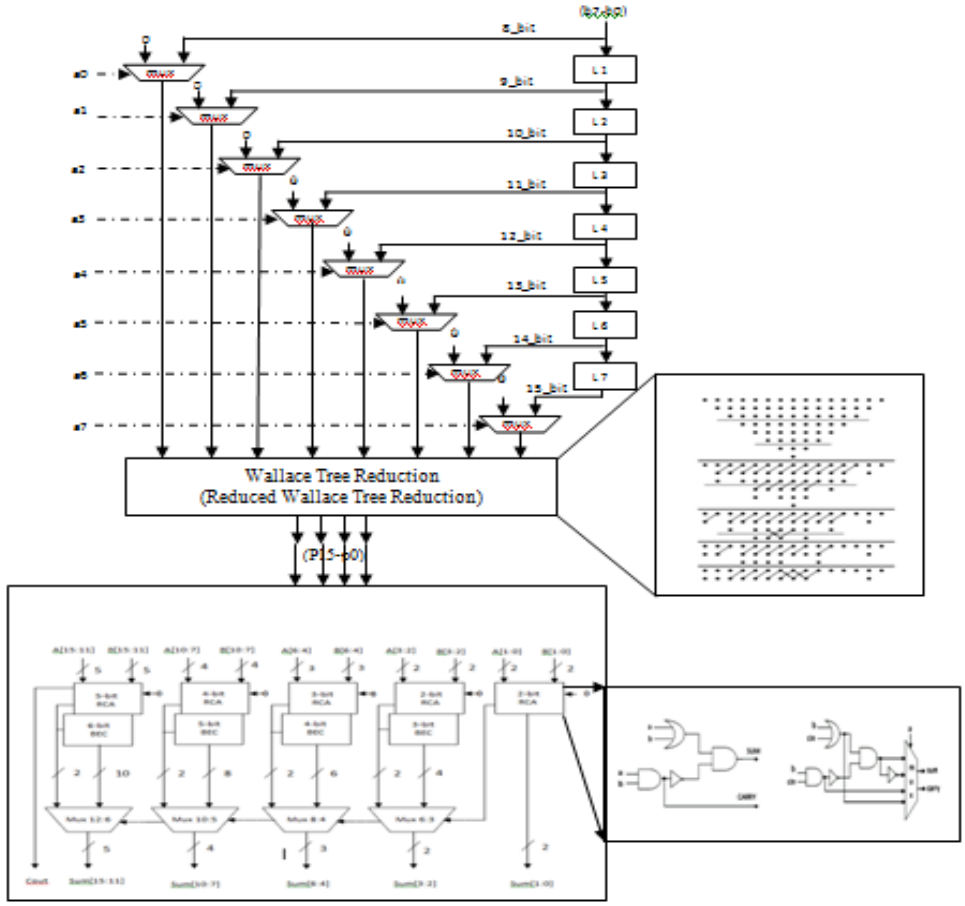

Figure-6. Architecture of MSQRTCSLA based MRPM based MAC unit.

SIMULATION RESULTS

Simulation result of Proposed MSQRTCSLA based MRPM MAC unit has been validated by using ModelSim 6.3C. The simulation result of Proposed MSQRTCSLA based MAC unit has been illustrated in Figure-7. As shown in Figure-7, multiplicand and multiplier value is given into '255' and '255' respectively, result in multiplied value '65025' is obtained in next clock cycle through proposed system. Clock based sequential circuit is used in this for improving the speed of the MAC unit.

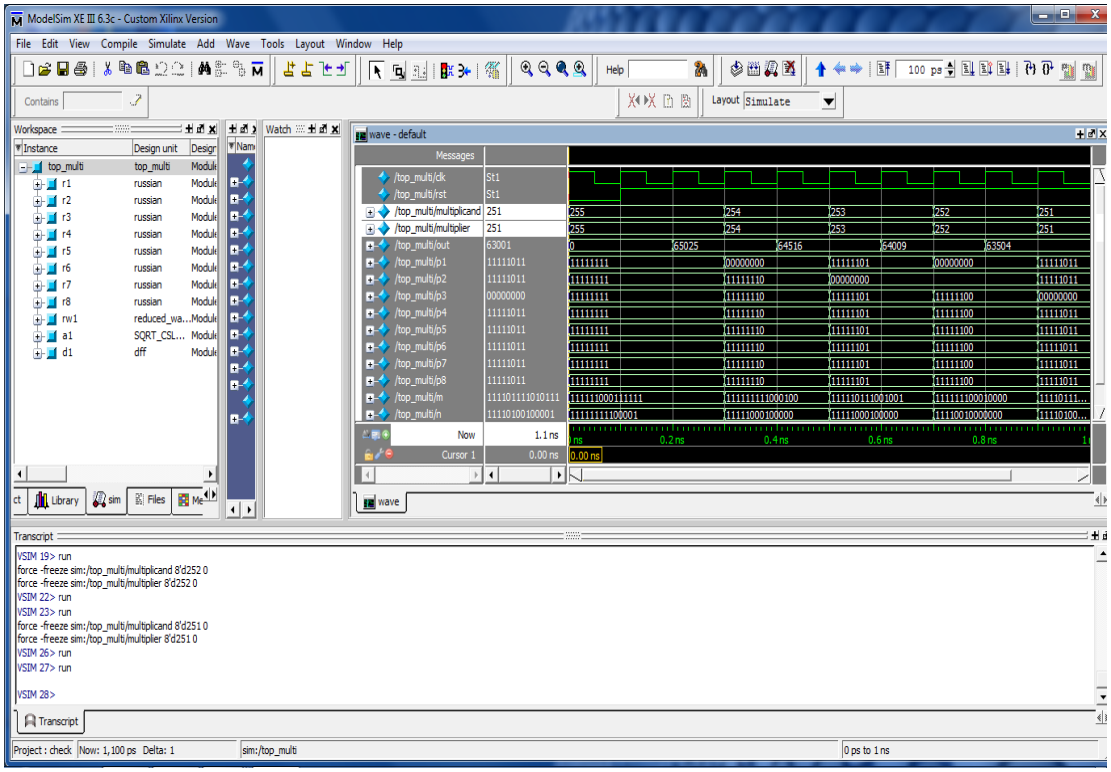

Figure-7. Simulation result of proposed MSQRTCSLA based MRPM multiplier.

PERFORMANCE EVALUATION

The performance of Bi-Recoder Multiplier, Russian Peasant Multiplier and MSQRTCSLA based Modified Russian Peasant Multiplier units are estimated by using Xilinx 10.1i (Family: Spartan 3, Device: Xc3s50, Package: PQ208, Speed: -5) design tool. The comparison of proposed MSQRTCSLA based MRPM with other traditional structures has been illustrated in Table-1.

From Table-1, it is clear that the proposed MSQRTCSLA based MRPM multiplier offers 29.41% reduction in Slices and 29.91% reduction in LUTs and 26.03% reduction in delay consumption than Reduced Complexity Wallace Multiplier using BEC based SQRTCSLA. Similarly, Proposed MSQRTCSLA based MRPM Multiplier offers 20.31% reduction in delay consumption and 61.31% reduction in power consumption than Bi-Recoder Multiplier using Reduced Complexity SQRTCSLA. The performance of Proposed MSQRTCSLA based MRPM multiplier with other traditional multiplier has been illustrated in Figure-8.

Table-1. Comparison of proposed MSQRTCSLA based MRPM with other traditional structures.

Types/Parameters	**Slices**	**LUTs**	**Delay** (ns)	**Frequency** (MHz)	**Power** (mW)
Bi-Recoder Multiplier using Compressor	77	145	31.469	31.777	978
Bi-Recoder Multiplier using Reduced Complexity SQRTCSLA	72	130	19.955	50.112	685
Reduced Complexity Wallace Multiplier using BEC based SQRTCSLA	119	224	21.499	46.513	264
Russian Peasant Multiplier using BEC based SQRTCSLA	82	154	17.000	58.823	765
Proposed MSQRTCSLA based MRPM	84	157	15.901	62.889	265

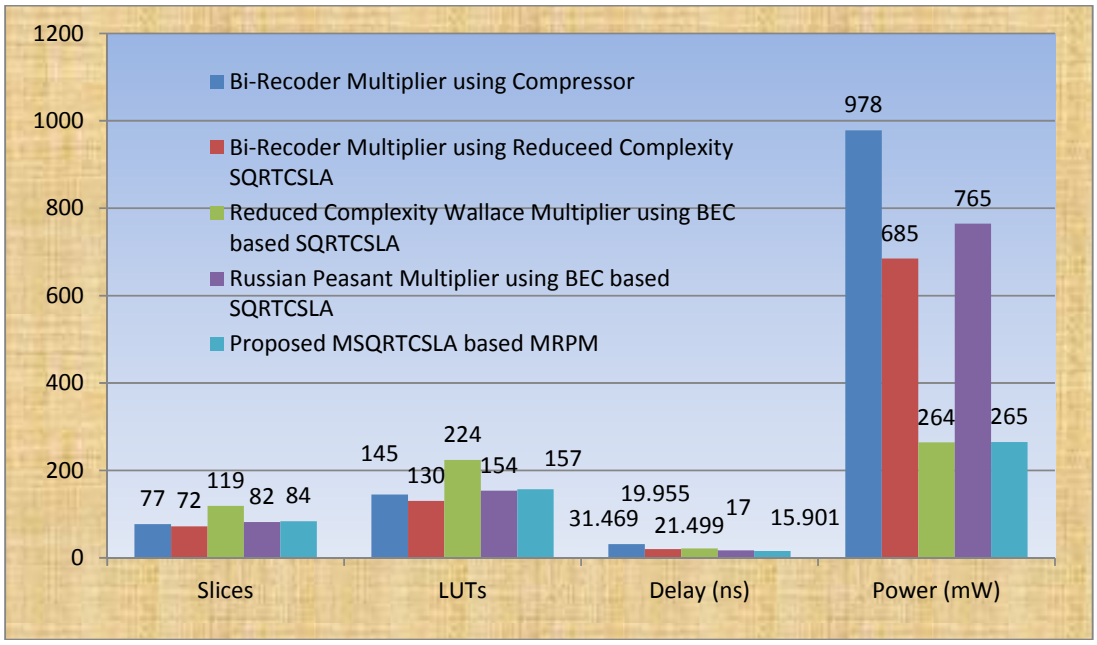

Figure-8. Performance of proposed MSQRTCSLA based MRPM with other traditional methods.

CONCLUSIONS

In this paper, Modified Russian Peasant Multiplier has been designed by using Verilog Hardware Description Language (Verilog HDL). For the Partial Product Generation (PPG), Proposed MRPM unit is used with the help of only "Multiplexers". For the Wallace Tree Reduction (WTR), Reduced Complexity Wallace Tree Reduction (RWTR) unit is used with the help of only "Full Adders". For the Partial Product Addition (PPA), Modified Square Root Carry Select Adder (MSQRTCSLA) is used with the help of Reduced Half Adder (RHA) and Reduced Full Adder (RFA). Hence, the proposed Multiplication and Accumulation unit (MAC) is named as "MSQRTCSLA based MRPM MAC" unit. The proposed MAC unit offers 29.41% reduction in Slices and 29.91% reduction in LUTs and 26.03% reduction in delay consumption than Reduced Complexity Wallace Multiplier using BEC based SQRTCSLA. Similarly, it provides 20.31% reduction in delay consumption and 61.31% reduction in power consumption than Bi-Recoder Multiplier using Reduced Complexity SQRTCSLA. In future, Proposed MAC unit offers great advantage in minimizing the chip size for designing the communication standards.

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