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VARIABILITY ANALYSIS OF PROCESS PARAMETERS ON SUBTHRESHOLD SWING IN VERTICAL DG-MOSFET DEVICE

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ABSTRACT

As the MOSFET's size is expected to be shrunk every year, it is difficult to mitigate the short channel effect (SCE) issues arising in the device. The conventional MOSFET's structure is no longer practical to apprehend these types of issues, especially for a device with a very small gate length (Lg). The SCE issues happen due to the reduction of the gate length (Lg), which causes the distance between the source and the drain region to become too close to each other. As a consequence, it causes the charge sharing effects between source and drain region that eventually leads to higher subthreshold swing (SS). A steep SS value around 55 to 65 mV/dec is desired in MOSFET device for faster switching operation. Therefore, a new architecture of Vertical Double Gate (DG) MOSFET device is proposed to circumvent these issues. Besides that, the process parameter variations in the device are also considered as one of the important factors that significantly affect the SS value. In this paper, an attempt to analyze the variability of multiple process parameters towards the SS value in 12nm gate length (Lg) vertical DG-MOSFET device has been made. At the end of the experiments, it was found that the most dominant process parameter that contributed a large effect on SS value was halo implantation tilt angle. The lowest possible value of SS was observed to be 62.52 mV/dec with signal-to-noise ratio (SNR) of -35.83 dB.

Keywords: ANOVA, DG-MOSFET, subthreshold swing, taguchi method.

INTRODUCTION

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is widely applied for amplifying and switching electronics signals. In MOSFET devices, a voltage potential that appears on the oxide-insulated gate electrode is capable of creating a conducting channel between the source and the drain region. The channel can be either n-type or p-type depending on the type of dopant used in the substrate. It is commonly recognized as a NMOS and a PMOS device. The source region is the source of charge carrier, either electrons or holes flow through the channel [1]. Meanwhile, the drain region is where the charge carrier leaves the channel.

Nowadays, MOSFET devices are actively being scaled down for miniaturization of integrated circuit (IC). By reducing the size of transistors and interconnectors, more circuits can be fabricated on each silicon wafer. Thus, the price of each circuit will become cheaper and affordable. However, miniaturization in MOSFET device has its side effect, which is known as short channel effects [2]. Many electronics scientists and researchers have conducted research on suppressing the SCEs in the nano-scale MOSFET devices. They tend to come out with new ideas of architecture and approach on how to mitigate the SCE issues.

Through the implementation of vertical DG-MOSFET architecture, the effective channel length (Lc) is no longer dependent on the gate length (Lg). The height of silicon pillars acts as a control factor to vary the size of effective channel length [3]. Therefore, various SCE problems are still possible to be mitigated even at small gate length (Lg) such 12nm of Lg. However, there is an important aspect that has to be considered, which is known as process parameter variations. Process parameter variations occur in every type of MOSFET device. These variations would affect the output responses (electrical characteristics) of the MOSFET devices. They may cause the degradation of overall MOSFET's electrical performance [4, 5].

In this paper, the 12nm gate length of vertical DG-MOSFET was successfully designed by using software SILVACO Technology Computer Aided Design (TCAD). The input process parameters that contribute the most significant impact on the SS value were investigated by utilizing L_{27} orthogonal array Taguchi method. The subthreshold swing is an important response which indicates the scalability limit of the MOSFET. It also shows how much change in the gate voltage (V_G) is required to change drain current (I_D) by one decade [6].

Vertical Dg-MOSFET design using Silvaco TCAD

A P-type silicon with <100> orientation was used as the main substrate for this experiment. A different silicon orientation will give different substrate properties such as device mobility. Normally, P-type silicon with <100> orientation is used for MOSFET fabrication process due to a significant improvement in the effective maximum mobility for the n-MOSFETs with a channel along the 100 directions and the channel direction had no effect on the noise level and the performances of the devices [7]. The silicon was etched in order to form a pillar or ridge that separated the two gates. The combination of buried oxide (BOX) and the polysilicon layer formed an enhanced channel that was capable of

suppressing SCEs by reducing the amount of charge carriers penetrating the depletion region. This transistor was connected with aluminum metal. The aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [8-10]. The complete structure of the designed device is shown as in Figure-1. It was observed that the physical gate length (Lg) was scaled down to 12nm, which met the specification in ITRS 2013 for the year 2020 [11].

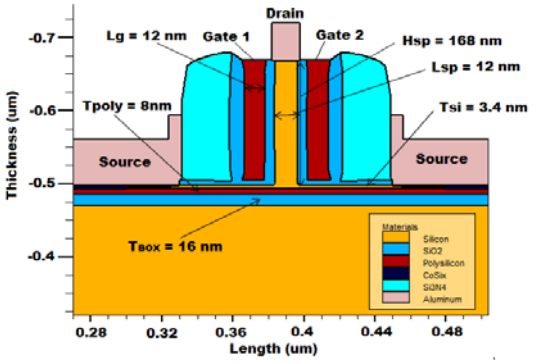

Figure-1. Structure of vertical DG-MOSFET device.

Statistical modeling using L_{27} orthogonal array Taguchi method

MOSFET processes typically have a large number of process parameters (control factors). The more complex a process is, the more control factors it has and vice versa. For each factor, normally two or three levels are selected for the appropriate orthogonal array (OA). The level of control factors is decided by their level of sensitivity. Table-1 shows the process parameters and their appropriate levels for the experiment.

Table-1. Process parameters and their levels.

Sym.	Process Parameter	Units	Level 1	Level 2	Level 3
A	Substrate Implant Dose	atom/cm³	1E14	1.03E14	1.06E14
B	V_{TH} Implant Dose	atom/cm³	9.81E12	9.84E12	9.87E12
C	V_{TH} Implant Energy	kev	20	21	22
D	V_{TH} Implant Tilt	degree	7	10	13
E	Halo Implant Dose	atom/cm³	2.61E13	2.64E13	2.67E13
F	Halo Implant Energy	kev	170	172	174
G	Halo Implant Tilt	degree	24	27	30
H	S/D Implant Dose	atom/cm³	1.22E20	1.25E20	1.28E20
J	S/D Implant Energy	kev	43	45	47
K	S/D Implant Tilt	degree	80	83	86
L	Compensation Implant Dose	atom/cm³	2.51E12	2.54E12	2.57E12
M	Compensation Implant Energy	kev	60	62	64
N	Compensation Implant Tilt	degree	7	10	13

In the Taguchi design method, it is crucial to estimate the sensitivity in a consistent way for any combination of the control factor levels [12]. In this research project, two noise factors, i.e. gate oxide temperature and polysilicon oxidation temperature, were used. These noise factors were varied for two levels in order to obtain four readings of SS for every row of the experiment. The value of the response, SS was used to determine the scalability limit of the device [13]. The values of noise factors at different levels are listed in Table-2.

Table-2. Noise factors and their levels.

Symbol	Noise factor	Units	Level 1	Level 2
U	Gate Oxidation Temperature	C°	920	923
V	Polysilicon Oxidation Temperature	C°	870	873

One of conventional practices is to guess, using trial and error method, using engineering judgment which relies heavily on luck and it is obviously inefficient and time consuming [14]. However, for this research, 27 experiments were conducted with 13 process parameters studied. A L_{27} (3^{13}) orthogonal array consisting of 27 set of experiments was developed.

Analysis of N-channel vertical DG-MOSFET device

Figure-2 depicts the graph of subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D=0.05V and V_D=1.0V for Vertical DG-MOSFET device. The value of off-leakage current (I_{OFF}), drive current (I_{ON}) and SS can be extracted from the graph. The I_{ON} is the drain current at a given gate voltage (V_G=2.0 V) and a given drain voltage. The I_{OFF} is obtained at a given drain voltage at V_G=0V.

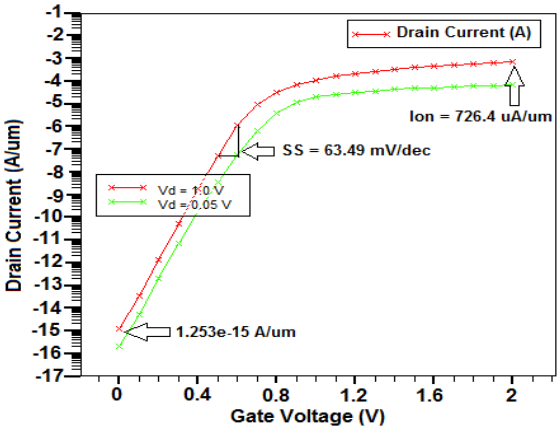

Figure-2. Graph of subthreshold drain current (I_D) versus gate voltage (V_G).

From the graph, it was observed that the value of drive current (I_{ON}) was 726.4 µA/µm. Meanwhile, the off-

leakage current (I_{OFF}) was observed to be 1.253e-15 A/μm. A very low leakage current (I_{OFF}) indicates a better suppression of the short channel effect (SCE) problems. The value of subthreshold swing (SS) was calculated by using Eqn. (1) [13]:

$$SS = \left[\frac{dV_{GS}}{d(\log_{10} I_{DS})} \right] \quad (1)$$

It was observed that the value of subthreshold swing (SS) was 63.49 mV/dec. Although the result was still within the acceptable range, it was still recommended to achieve SS as low as possible. To realize that particular objective, several input process parameters are required to be varied in order to recognize the most significant process parameters. It is important to notice that all of the input process parameters cannot be varied randomly because it will eventually defect the structure of the device. Therefore, statistical modeling is required in order to identify which process parameters would give the most significant impact on device characteristics.

Signal-To-Noise Ratio (SNR) analysis

The next step is to determine the most significant process parameters that contribute the most impact on device characteristics. The L_{27} orthogonal array analysis of the SS values was recorded in Table-3.

Table-3. SS values for vertical DG-MOSFET device.

Exp no.	Subthreshold Swing, SS (mV/dec)			
	SS_1 (U1V1)	SS_2 (U1V2)	SS_3 (U2V1)	SS_4 (U2V2)
1	63.49	63.51	63.52	63.58
2	63.08	63.24	63.07	63.09
3	62.88	62.62	62.57	62.64
4	63.42	63.55	63.67	63.64
5	63.02	63.06	63.02	62.92
6	62.57	62.88	62.84	62.59
7	63.32	63.37	63.41	63.33
8	63.06	63.07	63	62.99
9	62.56	62.78	62.72	62.51
10	62.50	62.58	62.52	62.63
11	63.61	63.58	63.62	63.53
12	63.12	63.58	63.15	63.14
13	62.39	62.25	62.88	62.75
14	63.53	63.51	63.56	63.44
15	63.34	63.67	63.67	63.56
16	62.71	62.94	62.61	62.87
17	63.51	63.49	63.53	63.42
18	63.48	63.61	63.62	63.39
19	63.05	63.06	63.06	62.87
20	62.58	62.79	62.41	62.73
21	63.65	61.3	63.69	60.64
22	63.08	63.15	63.07	63.01
23	62.91	63.16	63.20	63.03
24	63.58	63.58	63.62	63.55
25	62.91	62.86	62.84	62.82
26	62.56	63	62.98	62.88
27	63.61	63.6	63.68	63.60

After obtaining all the results, the process parameters of Vertical DG-MOSFET device were optimized by using Taguchi method. Taguchi method was assigned to analyze SS values by using SNR analysis (Lower-the-better). The SNR (lower-the-better), η can be expressed as in Equation (2) [14]:

$$\eta = -10 \log_{10} \left[\frac{1}{n} \sum_{i=1}^{n} y_i^{\,2} \right] \quad (2)$$

where *n* is number of tests and *yi* is the experimental values of SS. The SNR for each row of experiments were computed and recorded in Table-4 by using Equation (2).

Basically, the experiment row, which has the highest SNR, will be recognized as the best performing characteristics. Based on Table-4, it was observed that experiment row 21 had the highest SNR value for SS, which was observed to be -35.89dB. This indicates that the experiment of row 21 possessed the best in sensitivity for SS value. The effect of each input process parameter on the SNR at different levels can be separated due to the orthogonality of the experimental design. The SNR for each of the process parameters is summarized in Table-5.

Table-4. Mean sum of SQ and SNR for SS.

Exp no.	Mean Sum of SQ	S/N Ratio (Lower-the-Better) (dB)
1	4.04E+03	-36.06
2	3.98E+03	-36.00
3	3.93E+03	-35.94
4	4.04E+03	-36.07
5	3.97E+03	-35.99
6	3.93E+03	-35.95
7	4.01E+03	-36.04
8	3.97E+03	-35.99
9	3.92E+03	-35.94
10	3.91E+03	-35.93
11	4.04E+03	-36.07
12	4.00E+03	-36.02
13	3.91E+03	-35.93
14	4.03E+03	-36.06
15	4.04E+03	-36.06
16	3.94E+03	-35.96
17	4.03E+03	-36.05
18	4.04E+03	-36.06
19	3.97E+03	-35.99
20	3.92E+03	-35.94
21	3.89E+03	-35.89
22	3.98E+03	-36.00
23	3.98E+03	-36.00
24	4.04E+03	-36.07
25	3.95E+03	-35.97
26	3.95E+03	-35.97
27	4.05E+03	-36.07

Table-5. SNR of process parameters in vertical DG-MOSFET device.

Process Parameters	Signal-to-noise ratio (SNR)			Overall Mean SNR
	Level 1	Level 2	Level 3	
A	-36.00	-36.01	-35.99	-36.00
B	-35.98	-36.01	-36.00	
C	-36.02	-36.00	-35.98	
D	-36.01	-35.99	-36.00	
E	-35.99	-36.01	-36.00	
F	-36.02	-35.98	-36.00	
G	-36.04	-36.01	-35.95	
H	-36.01	-36.01	-35.98	
J	-36.00	-35.99	-36.00	
K	-35.99	-36.01	-36.00	
L	-36.01	-36.00	-35.98	
M	-35.99	-35.99	-36.02	
N	-35.99	-36.01	-36.00	

The chart factor effect of SS values for vertical DG-MOSFET device is shown in Figure-3. The chart depicts the type of control factor versus their corresponding signal-to-noise ratio in dB. The chart factor effect determines which level of individual input process parameters has the highest signal-to-noise ratio. Basically, the highest level of SNR for each individual process parameter will be selected as the best combination level setting of the device.

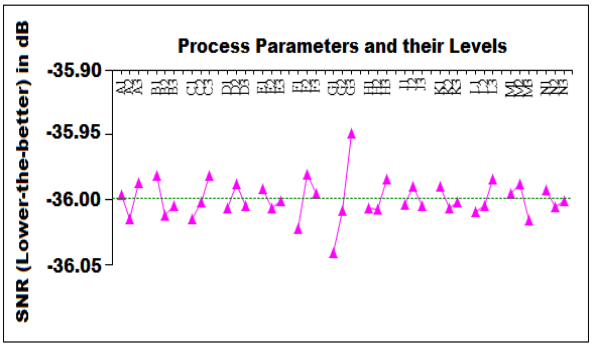

Figure-3. Factor effect plot for SNR (Lower-the-better) for SS.

Analysis of Variance (ANOVA)

The analysis of variance (ANOVA) is a common statistical method to investigate which of the input process parameters significantly affect the performance characteristic14. Basically, it utilizes parameter called sum of squares (SSQ), degree of freedom (DF), variance, F-value and percentage of each factor. The number of independent parameters related to an entity such as a matrix experiment, or a factor or a sum of square is called its degree of freedom (DF). The mean square (MS) for a factor is computed by dividing the sum of squares by the degree of freedom. The variance (mean square) of the tested process parameters is [14]:

$$MS = \frac{SSQ}{DF} \quad (2)$$

The results of ANOVA for the vertical DG-MOSFET device are shown in Table-6.

Table-6. Results of ANOVA for SS in vertical DG-MOSFET device.

Sym.	DF	SSQ	MS	F-value	Factor Effects on SNR (%)	Neutral/Significant/Dominant
A	2	0	0	2.21E+03	4.43	Neutral
B	2	0	0	2.88E+03	5.77	Significant
C	2	0	0	3.40E+03	6.79	Significant
D	2	0	0	1.24E+03	2.48	Neutral
E	2	0	0	6.77E+02	1.35	Neutral
F	2	0	0	5.25E+03	10.49	Dominant
G	2	0	0	2.56E+04	51.24	Dominant
H	2	0	0	1.98E+03	3.97	Neutral
J	2	0	0	8.21E+02	1.64	Neutral
K	2	0	0	8.63E+02	1.73	Neutral
L	2	0	0	2.04E+03	4.09	Neutral
M	2	0	0	2.51E+03	5.02	Neutral
N	2	0	0	5.03E+02	1.01	Neutral

According to these analyses, the most dominant factors for SNR were factor F (Halo Implant Tilt=51.24%) and factor G (Halo Implant Energy=10.49%). Therefore, these factors should be set at 'best setting'. Factor B (VTH Implant Dose=5.77%) and factor C (VTH Implant Energy=6.79%) were identified to be significant factors and they were not recommended to be altered. Meanwhile, the remaining factors were considered as neutral or negligible factors. Therefore, they do not contribute any significant influence on SS value. In contrast to the nominal- the-best analysis, there is no calculation of the factor effect on the means. The percent factor effect on SNR indicates the priority of a factor (process parameter) to reduce variation.

Verification test

The verification test is used to verify the estimated result with the experimental results [16]. The best combinational levels of the process parameters that produce the lowest SS value of vertical DG-MOSFET device as suggested by Taguchi Method was shown in Table-7.

Table-7. Overall best setting of process parameters.

Sym.	Process Parameter	Units	Best Value
A	Substrate Implant Dose	atom/cm^3	1.06E14
B	V_{TH} Implant Dose	atom/cm^3	9.81E12
C	V_{TH} Implant Energy	kev	22
D	V_{TH} Implant Tilt	degree	10
E	Halo Implant Dose	atom/cm^3	2.61E13
F	Halo Implant Energy	kev	172
G	Halo Implant Tilt	degree	30
H	S/D Implant Dose	atom/cm^3	1.28E20
J	S/D Implant Energy	kev	45
K	S/D Implant Tilt	degree	80
L	Compensation Implant Dose	atom/cm^3	2.57E12
M	Compensation Implant Energy	kev	62
N	Compensation Implant Tilt	degree	7

The verification test was required in vertical DG-MOSFET design because the optimal combination of process parameters and their levels, i.e. as A3, B1, C3, D2, E1, F2, G3, H3, J2, K1, L3, M2 and N1 did not correspond to any experiment of the orthogonal array. The result of the final simulation for the device is shown in Table-8. Before the optimization approaches, the best SNR (lower-the-better) was -35.89 dB at the row of experiment no. 21 as shown in Table-4. The mean sum of SQ was at 3.89E3, which was the smallest value among the others. After the optimization approaches, the SNR (Lower-the-better) of SS value for vertical DG-MOSFET device was -35.83 dB as shown in Table-8. These values are within the predicted range SNR of -35.77 to -35.88 (-35.83 ± 0.05 dB).

Table-8. Results of verification test for SS.

Subthreshold Swing (mV/dec)				SNR (Lower-the-better)
SS_1	SS_2	SS_3	SS_4	
62.52	62.78	62.72	62.56	-35.83

The lowest SS value for the device after the optimization approaches was observed to be 62.52 mV/dec, as listed in Table-8. This value was observed to be the lowest value among previous experiments. This indicates that Taguchi method was able to predict the optimum solution in obtaining the vertical DG-MOSFET fabrication recipe with the lowest possible SS value.

The comparison of the optimal result of SS value was also compared to the previous results of other researchers. Table-9 shows the comparison of the optimal SS value of vertical DG-MOSFET device with the value before the optimization approach and the value of previous researches. It can be observed that there was a slight improvement of the SS value in vertical DG-MOSFET device when the Taguchi method was applied for optimization purpose.

Table-9. Comparison of the optimal SS value with the previous researches.

Subthreshold Swing (mV/dec)			
Results from this work (Before optimization)	Results from this work (After optimization)	Results from Saad et al. (2011) [17]	Results from Rahul et al. (2014) [18]
63.49	62.52	83	63.74

CONCLUSIONS

In conclusion, the most dominant process parameter that contributed the largest effect on SS was recognized to be factor F, which was known as halo implant tilt angle. Taguchi method was able to predict the process parameters that have contributed the most significant impact on SS. The level of significance of each process parameter on SS was determined by using ANOVA method. Based on the ANOVA method, factor G (Halo Implant Tilt=51.24%), factor F (Halo Implant Energy =10.49%), factor C (VTH Implant Energy=6.79%) and factor B (VTH Implant Dose=5.77%) have been identified as the most significant factors. The final value of SS was observed to be 62.52 mV/dec with SNR of -35.83 dB. Therefore, L27 Taguchi method can be regarded as one of the effective tools to minimize response, SS in vertical DG-MOSFET device. For future development, the metal-gate/high-k stack technology can be integrated in the vertical DG-MOSFET layout for better device characteristics. Furthermore, other device characteristics such as threshold voltage (VTH), drive-on current (ION) and off-state leakage current (IOFF) and etc. can be statistically modelled by using Taguchi method for optimal device performance.

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