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DESIGN OF A DECIMATION FILTER USED IN DIGITIZER FOR EARTHQUAKE MONITORING SYSTEM WITH HIGHER SPEED

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ABSTRACT

The delegation of the Egyptian National Seismic Network (ENSN) is to determine rapidly the location and size of all destructive earthquakes worldwide and to immediately disseminate this information to concerned national and international authorities, scientists, and the public. An earthquake monitoring system consists of many electronic devices, one of these vital devices is the digitizer which converts analogue to digital signal. The Digitizer consist of three main modules, the first module is front-end, the second module is the parallel to digital converter using an oversampling technique with decimation filter and finally the packetization module. The Egyptian National Seismic Network (ENSN) is a fully automated and network system dedicated to the digital learning and real-time processing of seismological data, as considerably as the speedy exchange of earthquake data. This paper will focus on designing the decimation filter. The current decimation filter consists of three stages. The total decimation factor is 300. Finite Impulse Response (FIR) filter can reach more in effect performance with lower computational complexity and lower cumulative delay. The primary goal of this paper is optimizing the order of each stage using genetic algorithm. Finally both designs can be implemented on FPGA kit and a comparison between these two designs can be done. As a consequence, the computational complexity and the cumulative delay reduced to be 3052100 multiplications per second and 0.12 seconds respectively. The operating frequency of the modified decimation filter reached 8 MHz with power consumption of 211 mW on FPGA, VIRTEX7 xc7v585t-ffg1157.

Keywords: seismic, earthquake, digitizer, packet, decimation filter.

INTRODUCTION

Sigma delta (seismic signals [1]) analog to digital converter is used in the current digitizer in ENSN [2]. Over sampling technique is used in sigma delta to reshape the noise and achieve higher signal-noise ratio. its all zero structure, the FIR filter has a linear phase response when the filter coefficients are symmetric. The multi-stage FIR filter has been developed to realize sharp filter response with the small number of taps. By connecting M-tap FIR filter in a cascaded way, moreover, by inserting 1/N decimator between them, M^2 N equivalent taps can be realized. In recent days, 3-stage FIR filter is usually used for computationally efficient DDC as in [3]. One simple strategy to bring down the computational resources is to use a symmetric FIR filter. Because of the symmetric property of the filter coefficients, the complexity of the filter can be cut to a half by sharing the same coefficients. The novel design of FIR filter can enhance the computational complexity of the current FIR decimation filter with same performance using genetic algorithm [4]. FIR decimation filters by using multiple phases is used to guarantee minimum computational complexity with best execution. The previous and new design will be implemented using MATLAB2012b then converting this code to VERILOG CODE using MATLAB CODER, finally it will be synthesis on an FPGA kit (VIRTEX7 xc7v585t-ffg1157) using XILINIX ISE14.5. This paper is an initial step to implement the whole digitizer modules to be the first Egyptian digitizer (future work).

THE current FIR decimation filter used in the digitizer

The digitizer is sigma delta uses oversampling technique; the final sample rate is 100 samples per second. The Over Sampling Ratio (OSR) is 300 [5]. According to Trident user guide [3] the FIR decimation filter consists of three stages, Table-1 [5] shows the three stages. The decimation filter is a low-pass filter which causes a cut-off frequency is equal to1/OSR. This system, called multi-rate system [1], [6].

The cumulative delay of this design is 0.604233sec.This design can achieve using Kaiser Window. MATLAB can be employed to write this design. Table-2 indicates the pass-band frequency, stop-band frequency, stop-band ripple, pass-band ripple and sampling frequency. Table-2 shows the specifications of the three stages. The code will be converted to VERILOG code so the FIR filter should be fixed point [7]. To design fixed point FIR filter a Linear Buffer Implementation [8] can be applied. Figure-1.a shows the direct form of FIR filter while Figure1-b displays the linear buffer architecture [9]. The computational complexity of this design can be determined by the number of multiplications per second (MPS). Equation (1) shows the MPS [10] (MPS).

$$\sum_{j=1}^{m} Nj * Fj \quad (1)$$

Where Nj represents the length of the jet filter while Fj represents the sampling frequency for Goth stage

and m represents the number of cascaded stages. The filter length can be estimated from Equation (2) [10]

$$N = \frac{Ar-7.9}{14.36*\Delta f} + 1 \quad (2)$$

Where Ar is stop band attenuations while Δf is transition bandwidth (Hz). According to Equation (1) and Table-1, the computational complexity of the above system is 5364600 Multiplications per Second (MPS). Figure-2 shows a real seismic data from one of ENSN station in Egypt, passing through decimation filter with decimation factor of 300, the output data will be 100 samples per second. The left hand side of Figure-2 represents the seismic signal before passing through the current FIR decimation filter while, the right hand side of Figure-2 shows the seismic signal after passing the FIR decimation filter. Figure-2 is the current decimation filter used in ENSN without any optimization technique, Like GA,. The time lag is clearly appears, it's around 60 samples because the final data rate is 100 samples per second and the delay around 0.6 seconds. The data will appear clearly after 60 samples. The mean error between the input data and the output data (after 60 samples) is 1.9395e-10.

Design an fir decimation filter with lower computational complexity using genetic algorithm [3]

Genetic algorithm [3] is using to reach optimal solutions for corresponding problem. The trouble here is computational complexity should be minimized with three points as the previous plan. Population of solutions must be created, this population consists of chromosomes, each chromosome consists of genes, the number of genes here is lawful, and each numeral represents the decimation factor of one stage. The fitness function is defined over the genetic representation and measures the quality of the represented solution. The fitness function here is computational complexity. Later on this step the minimum fitness must selected to reach minimum complexity. Crossover and mutation are applied over the selected chromosomes. As a result a new set of chromosome is produced. An initial population is obtained by randomly creating an N number of chromosomal solutions called the first generation. The following measure, called pairing, consists of selecting the chromosomes that will mate together to multiply the issue. This is caused by using roulette wheel selection technique. These pairs will be employed for breeding. Re- production ensures that chromosomes with higher fitness will suffer a higher chance of reproduction than chromosomes with lower fitness. Replication is the application of crossover, mutation and elitism operators over the selected chromosomes. The best chromosome present in a particular generation is passed along to the next generation so that it will not be missed until the next best arrives. In this way the stability of the GA is improved. A fitness function or objective function has to be obtained to measure the operation of the chromosomes and compare their performance. This process is iterated until a fit solution appears. This repetition called a number of multiplications to acquire the optimal result. Figure- 3 is a flowchart of genetic algorithm [11]. The fitness function will be MPS, which represents the computational complexity. The number of iterations is 20. Figure-4 shows that after 5 iterations. Table-3 shows the new specification values; the pass-band frequency, stop-band frequency, stop-band ripple, pass-band ripple and sampling frequency. The new decimation factors are 5, 12 and 5. The MPS of the new design using GA is 2312500 multiplications per second. The cumulative delay is 0.1215 second. The difference between GA and the current design in MPS is 3052100 multiplications per second. The cumulative delay difference between GA and the current design of the digitizer is 0.4827 second. Besides the three stages have a linear phase response with constant group and phase delay. The mean error between the input data and the output data (after 11 samples) is 7.8425e-11. The new design is lower than the current plan of the digitizer in mean error by 1.1552e-10. The numbers of coefficients in the three stages are 57, 91 and 113 respectively. Figure-5 shows the input, which resembles with ratio of 300 and the output of real seismic data passing through the new design of FIR decimation filter with GA (decimation factor= 300). The left hand side of Figure-5 represents the seismic signal before passing through the current FIR decimation filter while, the right hand side of Figure-5 shows the seismic signal after passing the FIR decimation filter

The current and the new fir decimation filter on FPGA

All the above results are coded using MATLAB2012a. MATLAB CODER (TOOLBOX) can be sued to convert the MATLAB code to VERILOG code. VERILOG code can be a synthesis on FPGA kit using XILINIX ISE 14.5. This step is an initial step to plan all the digitizer using FPGA (FUTURE WORK). VIRTEX7 xc7v585t-ffg1157 will be applied. The result is listed below for the two designs. Table-4 shows the used and the available resources. Also establish the percent of employment resources. The total power consumption in the old FIR design is 229 mW, according to XILINIX XPOWER ANALYZER and the new FIR design with GA has a total power consumption of 211 mW. Figure-6 shows the translate, Mapping and Place & route has been done successfully on VIRTEX7 xc7v585t-ffg1157 kit. Finally the result on ISIM in XILINIX ISE 14.5 matched the result of MATLAB2012b.

Table-1. FIR decimation filter with specific order (β coefficient for the three stages = 3.3953).

	Pass-band Frequency	Stop-band Frequency	Pass-band attenuation	Stop-band attenuation	Sampling Frequency
Stage 1	592Hz	1000Hz	0.05 (linear)	0.01 (linear)	30000Hz
Stage 2	66Hz	90Hz	0.05 (linear)	0.01 (linear)	2000Hz
Stage 3	39.99Hz	42Hz	0.05 (linear)	0.01 (linear)	200Hz

Table-2. Specific values of the current design using Kaiser Window on MATLAB.

	Pass-band Frequency	Stop-band Frequency	Pass-band attenuation	Stop-band attenuation	Sampling Frequency
Stage 1	592Hz	1000Hz	0.05 (linear)	0.01 (linear)	30000Hz
Stage 2	66Hz	90Hz	0.05 (linear)	0.01 (linear)	2000Hz
Stage 3	39.99Hz	42Hz	0.05 (linear)	0.01 (linear)	200Hz

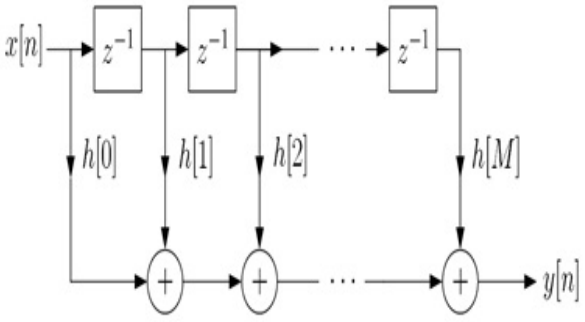

Figure-1(a). Direct form of FIR filter.

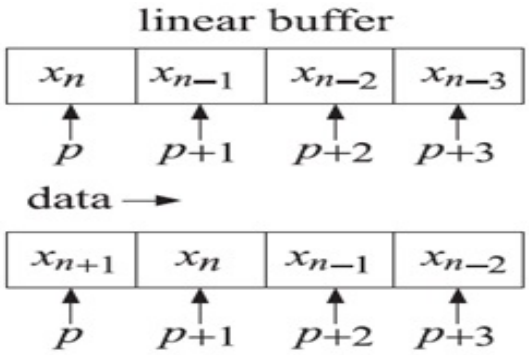

Figure-1(b). Buffer contents at successive time instants for D=3.

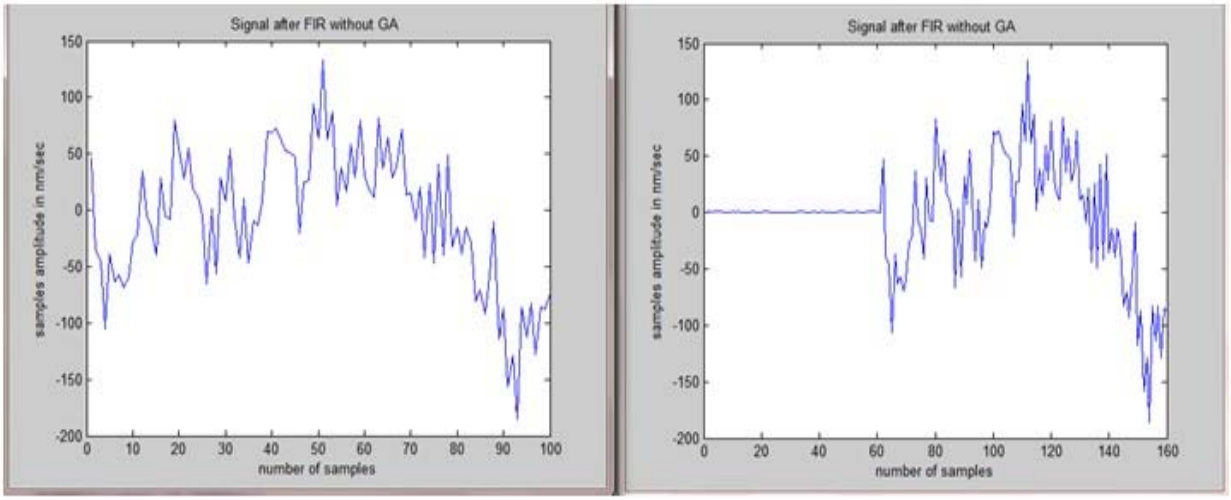

Figure-2. Effect of FIR decimation filter on real seismic signal.

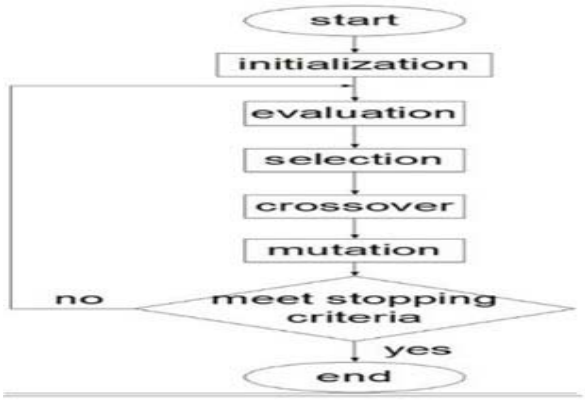

Figure-3. Flowchart of genetic algorithm (GA).

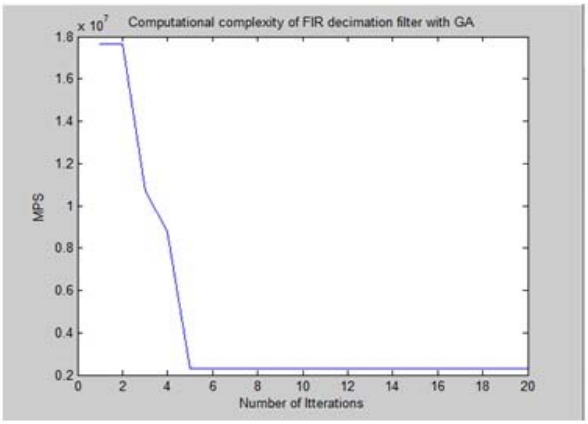

Figure-4. Number of iterations vs MPS for GA.

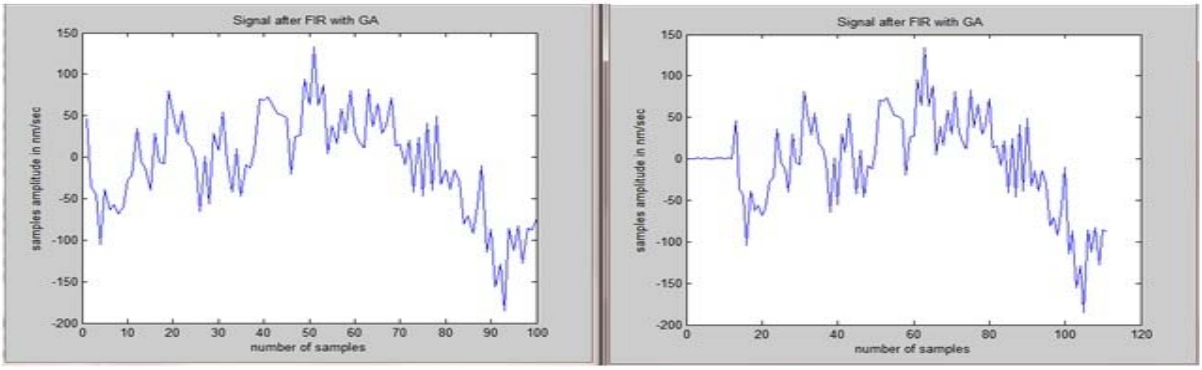

Figure-5. Effect of the new FIR decimation filter design on real seismic signal.

Table-3. New specification of FIR decimation filter using GA (β coefficient for the three stages = 3.3953).

	Pass-band Frequency	Stop-band Frequency	Pass-band attenuation	Stop-band attenuation	Sampling Frequency
Stage 1	4750Hz	5950Hz	0.05 (linear)	0.01 (linear)	30000Hz
Stage 2	301Hz	450Hz	0.05 (linear)	0.01 (linear)	6000Hz
Stage 3	40Hz	50Hz	0.05 (linear)	0.01 (linear)	500Hz

Table-4. Result of synthesis process using XILINIX ISE 14.5 (VIRTEX7 xc7v585t-ffg1157).

	Old FIR (used resources)	New FIR (used resources)	Available Resources
Number of Slice Registers	60	66	728,400
Number used as Flip Flops	13	23	
Number of Slice LUTs	3,047	1,394	364,200
Number used as logic	2,882	1,334	364,200
Number of occupied Slices	881	95	91,050
Number of LUT Flip Flop pairs used	3,048	1,408	
Clock period	293.68nsec	114.405nsec	
Frequency	3.405MHz	8.741MHz	

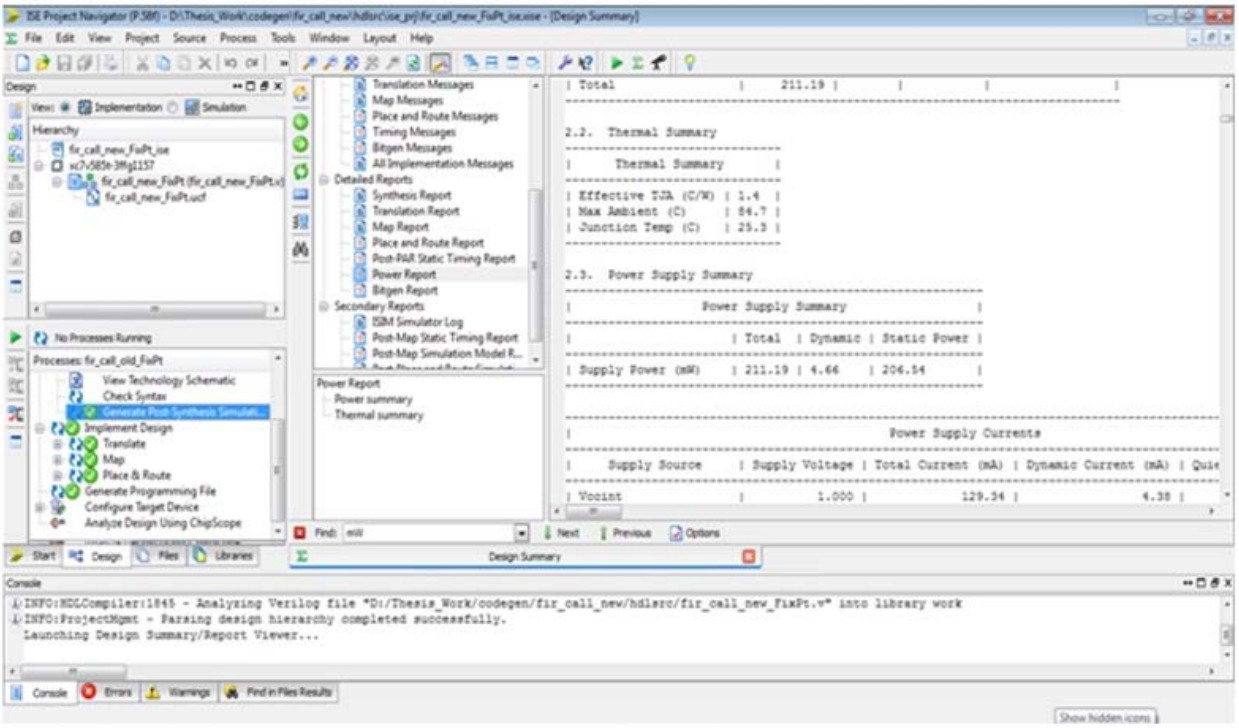

Figure-6. The implementation process (translate, map and PAR) for decimation filter (VIRTEX7 xc7v585t-ffg1157).

CONCLUSIONS

FIR decimation filters using multiple stages to guarantee minimum computational complexity with best performance. The new decimation factors are 5, 12 and 5. The MPS of the new design using GA is 2312500 multiplications per second. The cumulative delay is 0.1215 second. The difference between GA and the current design in MPS is 3052100 multiplications per second. The cumulative delay difference between GA and the current design of the digitizer is 0.4827 second. The total power consumption in the old FIR design is 229 mW while the modified filter has a total power consumption of 211 mW at operating frequency 8.741 MHz.

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