



OPTIMIZED FRACTAL INDUCTOR FOR RF APPLICATIONS

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ABSTRACT

Conventional planar inductor has large area, low inductance, low quality factor which is not suitable for present RFIC's technology. For RFIC applications we need low area, high inductance and high quality factor. This paper presents fractal inductor having high inductance of nearly 13% greater than conventional on-chip 3-D inductor with moderate quality factor values. This inductor occupies small on-chip size area of $10 \times 10 \mu\text{m}^2$ on silicon suitable for RFIC's applications. Fractal inductor performance is analysed by considering relative circuit model developed by conducting experiment in IE3D EM field solver. Due to its small size this inductor is operated at higher order frequency (10-100) GHz range that suits for RF applications. By applying the concept of fractal geometry, the length of conductor increases. Different geometries are available for fractal inductor design but, in this paper zigzag style of conductor run is considered with single iteration for one turn and two turns.

Keywords: fractal, inductance, IE3D, quality factor, RFIC's.

INTRODUCTION

Inductor is a very important component and plays key role in the design of RF circuits like phased locked loop (PLL), voltage controlled oscillator (VCO), transmitters, receivers, RF filters etc. Advancement in the Si-CMOS fabrication leads to the demand of on-chip inductor of small size with desirable quality factor and inductance values for RF circuits operating at GHz frequency range.

Fractal concept is introduced to increase the length of the conductors in the device without changing defined area. As mentioned in [1], based on different designs present in the literature such as Moore, Sierpinski, Hilbert, Luxberg etc. are replaced in the structure of the standard inductor. This is achieved by doing iterations which increases length of the conductor. It is observed that as number of iterations increases after certain limit inductance value decreased. As mentioned in [2], [3], using fractal concept electrical devices such as fractal capacitance with high capacitance in a single layer process is demonstrated and also about fractal antennas behavior in multiband frequency. As mentioned in [4], [5], Hilbert curve created based on space filling curves with property of 2-D structure is demonstrated in fractals. As mentioned in [6], fractal inductor is used to create high inductance in a single layer inductor accessing to multiple metal layers with certain limitations. As mentioned in [7], [8], there are many techniques to design inductors, some of them are conventional CMOS inductor, CMOS-MEMS inductor.

IE3D EM simulator is used for proposed inductor design and lumped series RL and Shunt RC model is used to obtain Q-factor and Inductance values. This paper is an extension of existing on-chip spiral inductor with better performance in terms of inductance and similar performance in terms of quality factor for higher range of frequencies in GHz range.

This paper comprises of Section 2 discusses about fractal inductor design and expressions used for

inductance and Q-factor calculation, Section 3 about results and Section 4 is conclusion.

Fractal inductor design

The shape of the proposed inductor is zigzag with two layers in its structure offering $5 \mu\text{m}$ spacing between each layer. Proposed multi-layer inductor is simulated in IE3D and analysis is carried out in EM field solver with the help of series RL and shunt RC lumped Pi model. The resistor and capacitor in model includes series capacitance and resistance formed between inductor turns, substrate capacitance and resistance offered substrate used and oxide capacitance formed between oxide and substrate. The lumped model is shown in Figure-1.

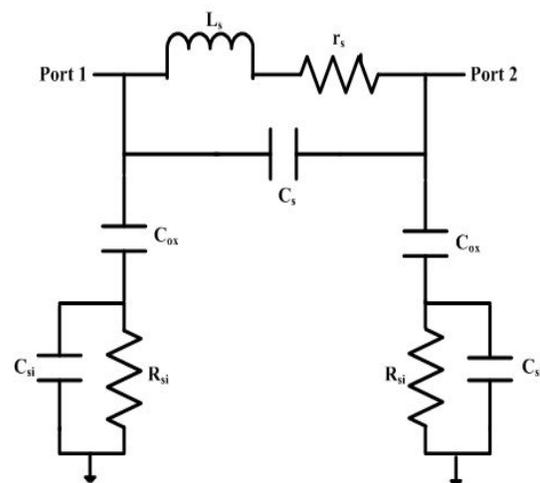


Figure-1. Lumped model of inductor.

The properties of substrate and conductor materials used in the design are mentioned in Table-1.



Table-1. Material properties.

Property	Substrate (Silicon)	Conductor (Copper)
Dielectric Constant	12	6
Loss Tangent	0.015	0.0001
Permeability	1	1.25×10^{-6}
Real Part of Conductivity (Ω/m)	0.00156	5.85×10^7

The dimensions of the proposed fractal inductors are width of conductor $0.6 \mu m$, spacing between adjacent conductors is $0.2 \mu m$, spacing between layers is $5 \mu m$, and number of turns of conductor are 1 turn and 2 turns. The top view of single turn and two turn fractal inductor is shown in Figure-2 and Figure-3 respectively. 3-D view of both the inductors is shown in Figure-4 and Figure-5 respectively. For the analysis only one iteration is considered and it's not extended for multi iterations due to area constraints. As the shape of fractal is zigzag, if multi iterations are considered the effect of mutual inductance because of coupling is more and showing negative impact on inductance greatly and on Q-factor moderately. Hence multi iterations are not considered for this model.

Material used for the design is silicon as substrate material, Silicon-di-oxide as oxide layer and copper as metal. Substrate thickness is maintained at high value to reduce the losses for increasing Q-factor value and copper has high conductivity which increases inductance value.

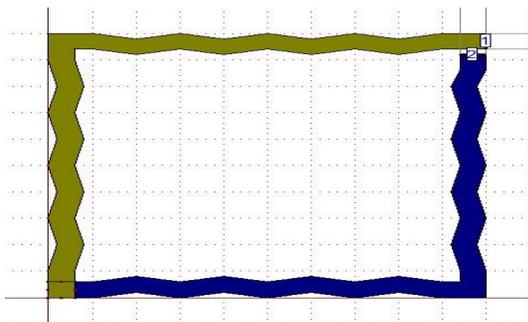


Figure-2. Fractal inductor with one turn (Top view).

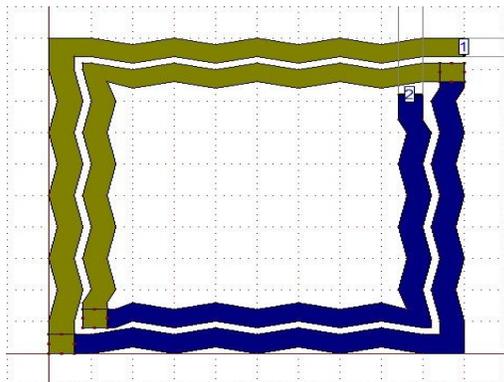


Figure-3. Fractal inductor with two turns (Top view).

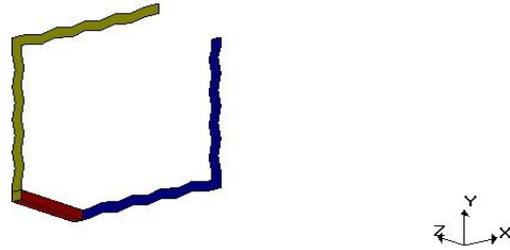


Figure-4. Fractal inductor with one turn (Side view).

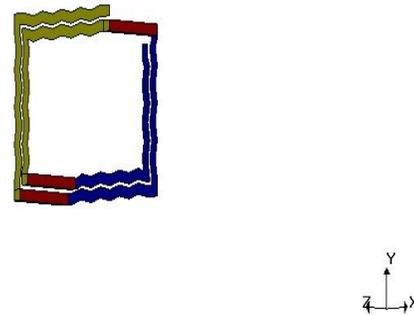


Figure-5. Fractal inductor with two turns (Side view).

The 3-D inductor considered for comparison is shown in Figure-6 and Figure-7 with one and two turn respectively. 3-D inductor is designed based on VLSI multilayer concept where half turn of conductor is placed in one layer and other half turn of conductor is placed in layer 2. Each color shown in Figure-6 and 7 represents one layer. All the conductors in each layer are connected through conical vias. Substrate used is silicon and conducting material (metal) used is copper. Conducting material used for vias is also copper to reduce losses. The outer diameter of the inductor is $10 \mu m$, width of conductor $0.6 \mu m$, spacing between adjacent conductors is $0.2 \mu m$, and spacing between layers is $5 \mu m$.

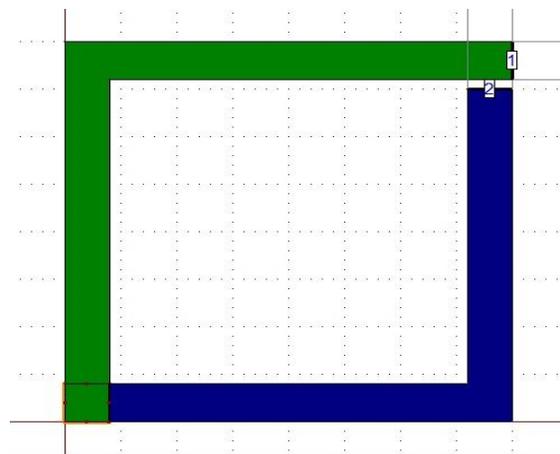


Figure-6. 3-D Inductor with one turn (Top view).

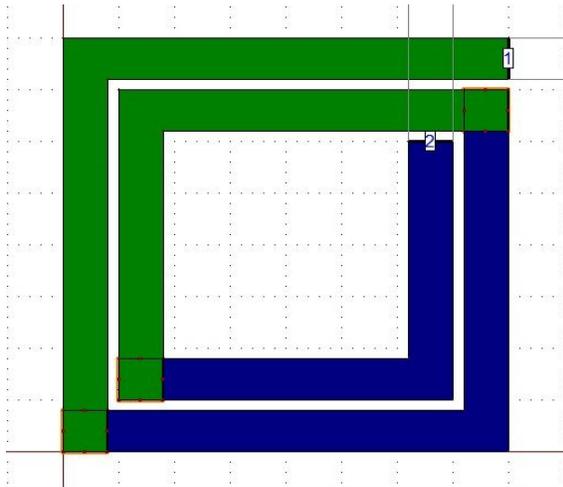


Figure-7. 3-D Inductor with two turn (Top view).

Expressions

As mentioned in [9], Greenhouse method is used for computing the inductance of planar rectangular spirals. Overall inductance of a spiral can be obtained by computing the self-inductance of individual segments and positive, negative mutual inductance between all possible wire segment pairs. As mentioned in [10], [11], general expressions for capacitances that are considered in the analysis of two port lumped model are expressed in Equation (1) and Equation (2), Quality factor is expressed in Equation (3), Inductance in terms of flux is expressed in Equation (4) and Equation (5).

Substrate capacitance

$$C_{si} = \left(\frac{WlC_0}{s} \right) \tag{1}$$

Shunt capacitance in inductor model considered is

$$C_p = C_{ox} \left(\frac{1 + W^2(C_{s1} + C_{ox})B_{s1}^2}{1 + W^2(C_{s1} + C_{ox})B_{s1}^2} \right) \tag{2}$$

Where w is metal width, l is length of conductor, C₀ is substrate capacitance per unit area and typically value is given between 10⁻² and 10⁻³ fF / μm². C_{si} and C_{ox} are substrate and oxide capacitance respectively. R_{si} is substrate resistance. Series resistance R_s is responsible for metal loss and this parameter gets affected greatly due to frequency variation. The quality factor Q, of the inductor is expressed as

$$Q = \frac{wL_s}{R_s} \frac{1}{1 + \frac{R_s}{R_p} \left[\left(\frac{wL_s}{R_p} \right)^2 + 1 \right]} \left[1 - \frac{R_s^2(C_s + C_p)}{L_s} - w^2 L_s (C_s + C_p) \right] \tag{3}$$

Resistance of a wire to higher frequencies current is greater than resistance to direct current. At higher frequencies current does not penetrate far into the body of conductor but travels along the surface. At higher order frequencies skin depth is very low and current is passed through thin shell of metal. Total magnetic flux associated

with the second conductor, due to conductor carrying current I₁ is given by

$$\Phi_{21} = \int \int \frac{\mu_0 I_1}{4\pi r^2} dl_1 dl_2 \tag{4}$$

Magnetic flux is increased by increasing the width of conductor. The mutual inductance between conductors is given as

$$M_{21} = \frac{\Phi_{21}}{I_1} = \left[\frac{\mu_0}{4\pi} \right] \tag{5}$$

RESULTS

Inductance and quality factor values obtained for fractal inductor are compared with standard 3-D inductor. Inductance against frequency for one turn and two turn is shown in Figure-8 and Figure-9. From the result inductance of fractal inductor is nearly 13% higher than 3-D inductor for both one turn and two turn.

Procedure followed for the analysis of inductor is as follows:

1. After designing assign porting at each end, set meshing frequency and sweep range of frequency for simulation.
2. Apply meshing for entire design and begin simulation.
3. Inductance and Q-factor values are obtained based Y-parameters expression shown in Equation (6) and Equation (7), respectively.

$$\text{Inductance (L)} = -1 / (2 * \pi * \text{freq} * \text{Im} \{Y_{11}\}) \tag{6}$$

$$\text{Quality Factor (Q)} = \text{Im} \{Y_{11}\} / \text{Re} \{Y_{11}\} \tag{7}$$

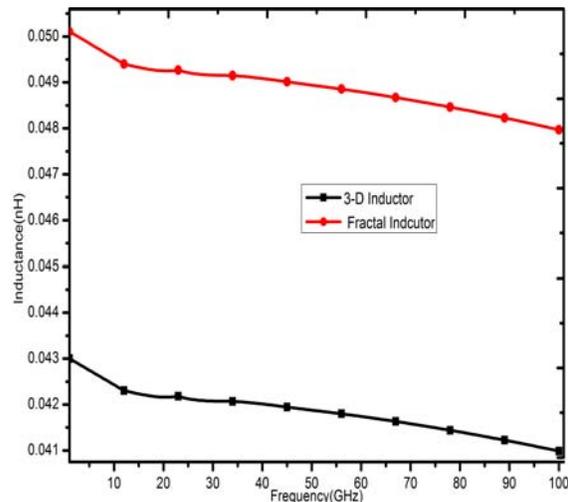


Figure-8. Frequency Vs Inductance for one turn.

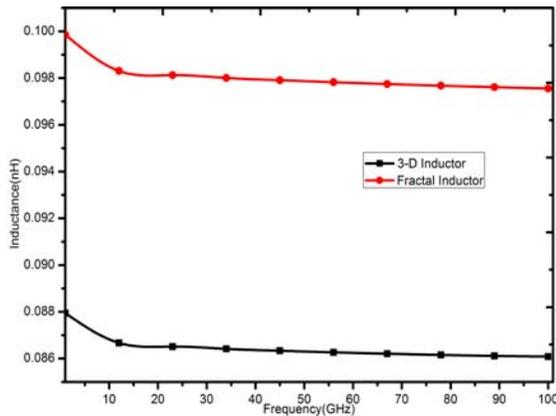


Figure-9. Frequency Vs Inductance for two turn.

Quality factor of the fractal inductor against frequency for one turn and two turn is shown in Figure-10 and Figure-11. From result it can be observed that quality factor of both inductors is moderate and has less difference.

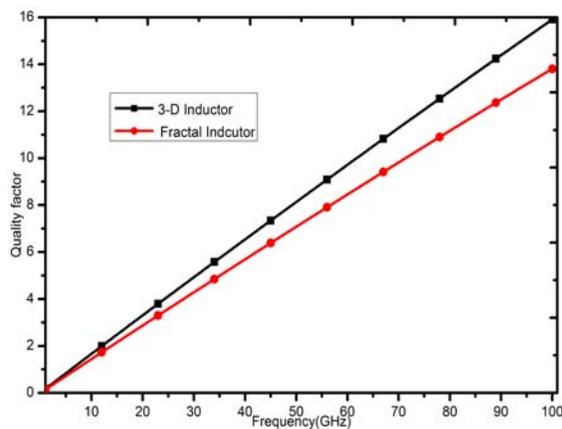


Figure-10. Frequency Vs Quality factor for one turn.

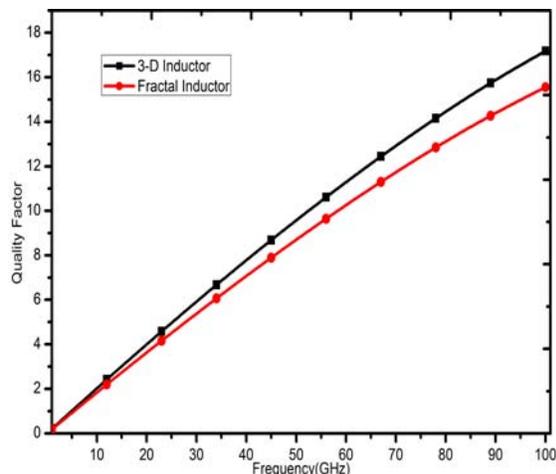


Figure-11. Frequency Vs Quality factor for two turn.

The maximum value of Inductance and Q-factor is compared with existing fractal structure as shown in Table-2. Values mentioned in the table are maximum values obtained in the structure mentioned respectively. 3O in table represents 3-omega iterations, 5O is 5-omega iterations and 7O is 7-omega iterations.

Table-2. Comparison with existing fractal structure.

Structure	Q-factor	Inductance (nH)	Area (mm ²)
3O[12]	5.2	3.6	3.52
5O[12]	6.5	4.2	2.21
7O[12]	4.7	4.4	3.42
My work	17	0.1	0.0001

From Table-2 it can be observed the optimization in terms of area is achieved with high Q-factor for single iteration. The value of inductance can be increased further by varying dimensions of the conductor within the specified area.

CONCLUSIONS

From the results, the proposed fractal inductor has higher inductance of 13% over 3-D inductor and quality factor of proposed fractal inductor is near values with constant width 3-D inductor moderate. As the proposed inductor is occupying less on-chip area of cross-section $10 \times 10 \mu\text{m}^2$, when compared with existing fractal inductor structures the area occupied by proposed inductor is very low, hence area optimization is achieved. The proposed fractal inductor is more suitable for RF applications in the frequency range of (10-100) GHz.

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