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ANALYSIS OF MINIATURE ON-CHIP 3-D INDUCTOR FOR RF CIRCUITS

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ABSTRACT

In this paper, parametric analysis of miniature on-chip 3-D inductor is presented. The effect of conductor width, spacing between conductors and number of turns of inductor on Quality factor (Q-factor), inductance and Self-resonant frequency (SRF) are studied. Improvement in percentage increase of Q-factor is due to increase in conductor width. It can be found that ~72% of on-chip area reduction is observed when compared with conventional inductor design. Effective Q-factor and inductance are to be verified experimentally through dynamic variation of different parameters over the desired frequency range. The dimension of inductor considered for analysis is 100 µm ×100 µm, suitable for improved inductor design in high frequency RF circuits.

Keywords: inductance, quality factor, RF circuits.

INTRODUCTION

Inductor is an important and essential component in on-chip RF circuits. In RF circuits like voltage controlled oscillator (VCO), Low noise amplifier (LNA) and Phase locked loop (PLL), on-chip inductor Q-factor is the key element. In literature on-chip inductor design based on standard silicon process provides maximum Q-factor of 10 with large area, this low Q is due to ohmic losses and eddy current losses. Ohmic losses in device is due to thin metal layers and eddy current losses is due to high substrate coupling.

As mentioned in [1], these losses affect self-resonant frequency and Quality factor of device which limits specifications of RF circuits operation. Improvement in RF-VLSI technology demands for small-size and high Q-inductors. As mentioned in [2], advancement in silicon processing technologies lead to the development of high speed on-chip devices for RF circuits operating at higher frequencies. As mentioned in [3], during the latest trends, MEMS technology provides better solution for providing small area and high-Q inductors. As mentioned in [4], in literature, CMOS and CMOS-MEMS inductors provides maximum Q-factor of 8 and 13 at 5.85GHz respectively. As mentioned in [5], limitation of MEMS technology is cost effective, development of microsystems and its miniaturization is major challenge. To overcome this challenge multi-layer on-chip inductor design is considered. To decrease losses of device substrate layer with high thickness and material with high conductivity is considered. As mentioned in [6], at high frequencies, due to skin effect and high thickness of oxide layer current entering to the conductor decreases, which in turn decrease the substrate losses in device. As mentioned in [7], in addition to this when outer diameter of device is decreased, the area occupied by the device is minimized, which decreases the substrate losses. As mentioned in [8], to achieve cost-effective silicon devices, area-efficient devices with better performance at desired frequency is required.

On-chip inductor considered for analysis is designed using silicon as substrate with high thickness and copper as conducting material. The dimension of outer diameter of device is 100µm and on-chip area occupied is 100 µm×100 µm, which is minimized to decrease losses and to increase Quality factor.

This paper comprises of as follows Section II discuss about design and modelling, Section III about results and discussion and Section IV about conclusion.

DESIGN AND MODELING

On-chip inductor performance is analysed based on Inductance, Quality factor and self-resonant frequency. Quality factor and inductance of the inductor are effected with variation in conductor width, spacing between conductors and number of turns of device. On-chip inductor shown in Figure-1 is a 4.5 turn inductor with outer diameter of 100 µm, width of conductor of 8µm, spacing between conductors is of 2 µm and spacing between layers of conductor of 5 µm.

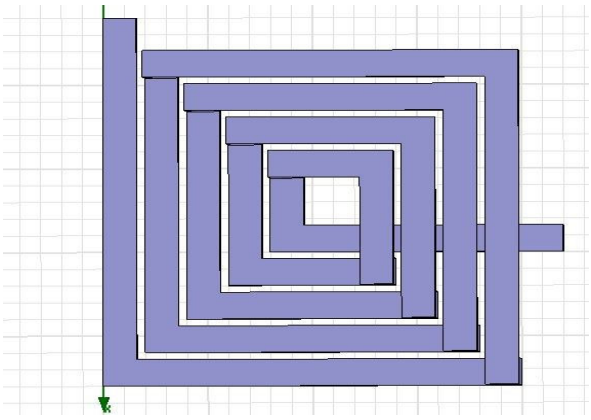

Figure-1. On-chip 3-D inductor with 4.5 turn.

This on-chip inductor is designed using multi-layer technology in VLSI. Conductors are placed on two different layers in which half turn of the conductor is placed in layer 1 and another half turn is placed in layer 2. All the conductors placed in layer1 and layer 2 are interconnected using vias. The material used for the

conductor run and for vias is copper. The conductivity of copper is very high, resistivity is very low which decreases loss in conducting material. When distance between inductor and substrate is increased by placing oxide layer, substrate capacitance is deceased which further decreases the parasitic capacitance reducing substrate losses. This spacing also isolates the inductor.

Three dimensional (3-D) view of on-chip inductor is shown in Figure-2. This inductor is designed and simulated in High Frequency Structure Simulator. Modeling of inductor on silicon is done considering the basic lumped model consists of series inductance and series resistance. Equivalent resistance and capacitance of substrate and oxide are considered in parallel combination. The capacitance in the model effects the self-resonant frequency of the device. Design of this inductor is based on 180 nm technology which is not a layout specified CMOS technology. As the on-chip area of the device is minimized to µm scale, the device finds more suitability for RF circuits which operates at higher order frequency ranges.

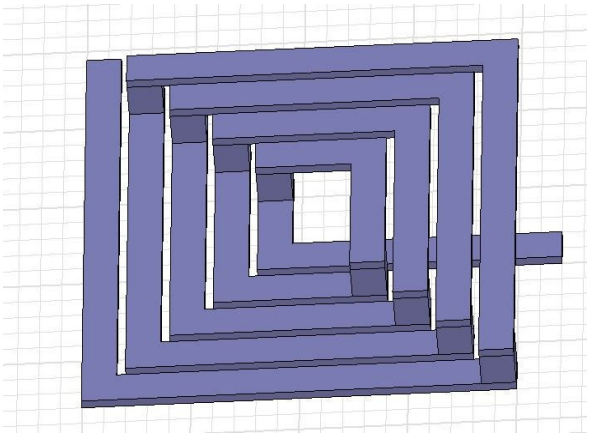

Figure-2. 3-D view of on-chip inductor with 4.5 turn.

Analytical expressions considered for obtaining Quality factor and inductance are given by Equation (1), Equation (2) and Equation (3).

$$Q = \frac{wL_s}{R_s} \cdot \frac{1}{1+\frac{R_s}{Rp}\left[\left(\frac{wL_s}{R_s}\right)^2+1\right]} \left[1 - \frac{R_s^2(C_s+C_p)}{L_s} - w^2 L_s(C_s + C_p)\right] \quad (1)$$

where Ls is series inductance and Rs is series resistance, Cs is substrate capacitance, Cp is parasitic capacitance.

$$\emptyset_{21} = \frac{\mu_0 I_1}{4\pi} \int_{-\frac{l_2}{2}}^{\frac{l_2}{2}} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \frac{e^{-j\beta_1 z|}}{\sqrt{(d)^2+(z-z|)^2}} dz| dz \quad (2)$$

where d is distance between conductors, Z and Z| are position of conductors. Magnetic flux is increased by increasing the width of conductor. The mutual inductance between conductors is given by

$$M_{21} = \frac{\mu_0 I_1}{4\pi I_2}\left[\frac{\emptyset_{21}}{e^{-j\beta_z z}}\right] \quad (3)$$

where I1 and I2 are current flowing in conductor 1 and conductor 2.

As mentioned in [9], inductance of an on-chip inductor is calculated based on Greenhouse concept. Total inductance of a device is a summation of self and mutual inductance. Mutual inductance again consists of positive and negative terms. When spacing between conductors is increased negative mutual inductance is decreased which results to the increment in the total inductance value. The response of on-chip inductor against frequency is in terms of Quality factor and inductance for dimensions conductor width 8 µm, spacing between conductors 2 µm, number of turns 4 and spacing between layers 5 µm are shown in Figure-3 and Figure-4 respectively. From Figure-3 it can be observed that the maximum Quality factor obtained is nearly 20 at 30 GHz.

From Figure-4 it can be observed that the device losses its inductive nature at 50 GHz, after 50 GHz device behaves like capacitor. The maximum value of inductance of this device is 5 nH at 48 GHz.

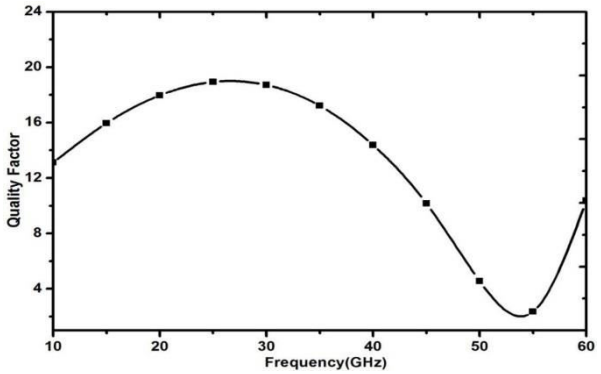

Figure-3. Quality Vs Frequency for on-chip inductor of range (10-60) GHz.

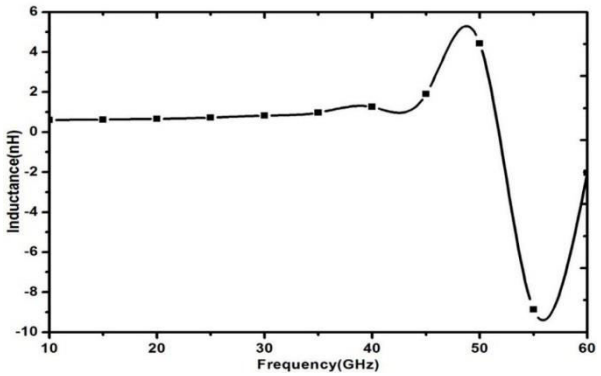

Figure-4. Inductance (nH) Vs Frequency for on-chip inductor of range (10-60) GHz.

RESULTS AND DISCUSSION

On-chip inductor considered here is analysed in terms of conductor width variation, spacing between conductor's variation and number of turns of the device. The response of these devices in terms of parametric variation is plotted and the behaviour of the device is observed. In Figure-5 and Figure-6 the response of device

in terms of Quality factor and inductance w.r.t conductor width variation from 6µm to 12 µm is shown. In Figure-7 and Figure-8 the response of device in terms of Quality factor and inductance w.r.t spacing between conductors from 1 µm to 4 µm is shown. In Figure-9 and Figure 10 the response of device in terms of Quality factor and inductance w.r.t number of turns from 1 to 3 is shown. The frequency range of operation considered for the analysis is from (10-60) GHz.

From Figure-5 it can be observed that as conductor width increases Q-factor value increases. Q-factor value mainly depends on series resistance in which losses are incurred. As losses are increasing, quality factor value decreases. In expression shown in Equation (1) the loss term is mentioned in denominator in form of series resistance. From Figure-6, the inductance value decreases as width of conductor is increasing. The resonant frequency is increasing as the width of conductor is increasing. The maximum inductance value obtained is 5nH at 48 GHz frequency. In this analysis spacing between conductors is 2 µm, number of turns of the device is 3

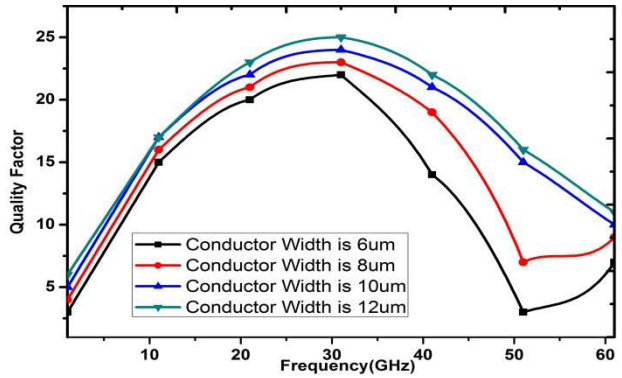

Figure-5. Quality factor of inductor for different conductor width.

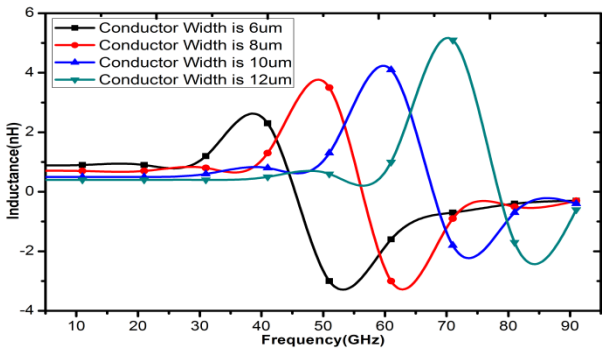

Figure-6. Inductance of inductor for different conductor width.

From Figure-7 it can be observed that due to variation in conductor spacing of the device the quality factor is varying. As spacing is increasing the quality factor of device is increasing. From Figure-8, the inductance value is increasing as spacing between conductors is increasing. In this analysis width of conductor is 8µm, number of turns of the device is 3.

The simulation process followed for the analysis of inductor is meshing and porting of the device. After porting S-parameters are obtained to calculate Quality factor and inductance. Now from S-parameters, Y-Parameters are obtained. Using Y-Parameters the quality factor and inductance values are calculated using the expressions shown in Equation (4) and Equation (5) respectively

$$Q = \frac{Im\{Y_{11}\}^{-1}}{Re\{Y_{11}\}^{-1}} \quad (4)$$

$$L = \frac{Im\{Y_{11}\}^{-1}}{\omega} \quad (5)$$

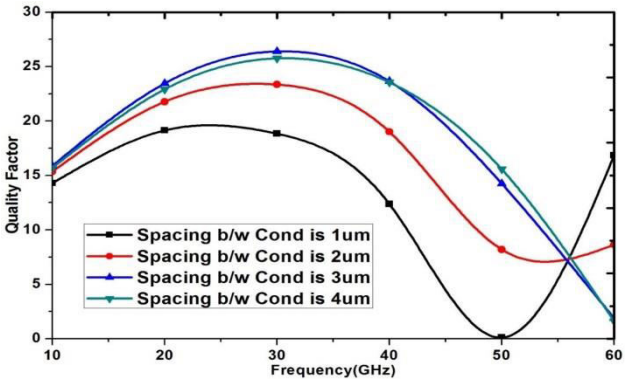

Figure-7. Quality factor of inductor for different spacing between conductors.

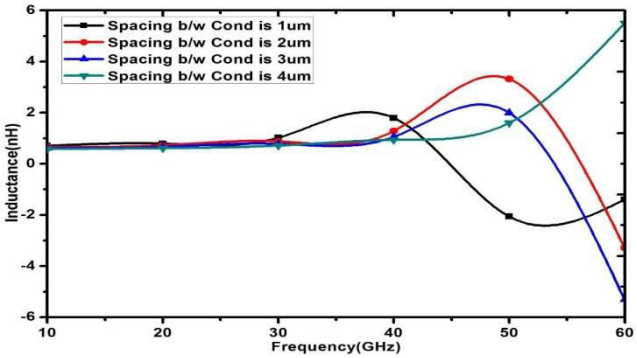

Figure-8. Inductance of inductor for different spacing between conductors.

From Figure-9 it can be observed that as number of turns of device increases the parasitic capacitance between the turn's increases, as capacitance increases losses in device increases which leads to a decrement in Quality factor. From Figure-10 it can be observed that the inductance value is increasing as number of turns are increasing which is due to increment in the overall conductor length. In this analysis width of conductor is 8µm and spacing between conductors is 2 µm.

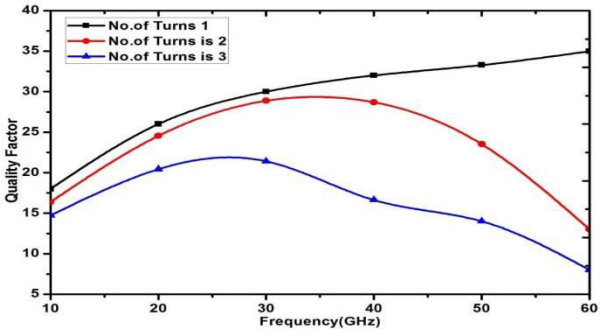

Figure-9. Quality factor of inductor for different turn numbers.

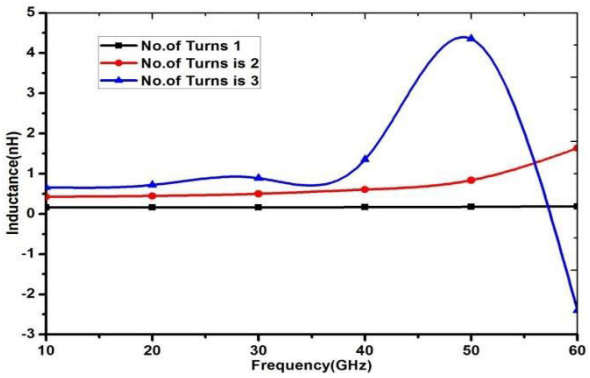

Figure-10. Inductance of inductor for different turn numbers.

Comparison between previous works and my design is shown in Table-1. The values mentioned in the table under my work are the maximum inductance, Q-factor and SRF obtained by the parametric analysis. The area of inductor for the entire analysis process is same as mentioned.

Table-1. Comparison of different inductors.

Works	Shape	Q	L (nH)	Size	SRF (GHz)
Si-GaAs[1]	Rect	29.5	15	470*470	11.4
Silicon[1]	Rect	19.4	12.5	470*470	8.6
Nitride[1]	Rect	12.5	2.4	315*315	13
MEMS[4]	Circ	27	0.61	185*200	65
My work	**Rect**	**18**	**5**	**100*100**	**72**

CONCLUSIONS

Thorough investigation of miniaturized inductor for RF circuits is concluded in this paper. The parametric characteristics of this design was presented and the design procedure outline its performance in terms Quality factor and inductance. The effective Q-factor and inductance was also studied experimentally by considering dynamic variation of the design parameters with in the frequency range of (10-60) GHz. Better performance of the design is obtained with the optimized parameters from different iterations. Maximum value of quality factor obtained in the analysis is 18 at 30 GHz, Inductance is 5nH at 48GHz and SRF of 72 GHz. Size reduction of ~72% is obtained for the design when compared to conventional inductors.

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