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ANALYSIS AND DESIGN OF A CLOSED LOOP BRIDGELESS SEPIC CONVERTER FOR SRM DRIVE WITH REDUCED RIPPLE CURRENT

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ABSTRACT

The switched reluctance machine (SRM) is used for many application of electric drive system due to its simple construction and its robustness.Due to doubly salient structure of SRM; the torque pulsations are high when compared to other sinusoidal machines. The major drawback of using SRM drive is torque pulsations and increased components in the converter. In order to avoid these drawbacks a new bridgeless Single Ended Primary Inductor Converter (SEPIC) for closed loop control of SRM drive is proposed.The proposed converter reduces a conduction loss, input current ripple, torque ripples and also the Total Harmonic Distortion(THD).The requirements of converter for switched reluctance motor drives and the proposed new converter are analyzed and dicussed. In this paper a new converter topology for speed control of a switched reluctance motor is proposed and verified through MATLAB simulation

Keywords: switched reluctance motor (SRM), bridgeless converter, single ended primary inductor converter (SEPIC), power factor correction (PFC), ripple reduction, pulse width modulation (PWM), total harmonic distortion(THD).

1. INTRODUCTION

The switched reluctance motor is the least expensive electrical machine to produce, yet one of the most reliable. As such, research has blossomed during the last decade and they require a power electronic converter and controller to function, however a successful realization of an SRM variable drive system demands an understanding of the converter and controller subsystem and their integration with the machine. The SRMdrive has recently gained considerable attention among researcher to several reason. Firstly there is a greater degree of independence between phases than is possible in conventional ac or dc drives. Due to very little mutual inductance the mutual coupling is neglected and this is a unique feature of this machine only. Due to this feature, a short circuit fault in one phase winding has no effect on other phases. Secondly the stator poles which are made up of steel laminations without permanent magnet or cages. So the motor is cost effective compared to conventional induction motor and synchronous motor. Thirdly due to unidirectional current requirement , the converter has a minimum number of switching devices compared to conventional inverter fed synchronous or induction motor drive and thereby greately simplifying the design. Also high starting torque can be achieved without large inrush current and the torque produced is independent of current direction. Therefore SRM is easy to manufacture, low priced variable motor due to its simple structure with reduced cost over various AC and DC motor drives [1].

For switched reluctance motor the converter is not fixed till now also the research is going on to overcome the problems associated the converters and the various topologies used now a days are resonant, bifilar, split dc supply, r-dump and asymmetric bridge converters. The major drawbacks of SRM drive is large torque ripples due to its discontinuity in the generated torque. By using phase current overlapping method, the torque ripples can be reduced to a small extent. Torque ripples also produced due to back emf produced during commutation of each phase causes the stator current to fall behind the reference current. After the occurrence of reference current, the phase current reaches zero causing a negative torque and high torque ripples produced by SRM drive. Therefore, converters which are used in SRM drive are to be modified to have fast commutation ability for its desirable operation.

In most of the AC-DC converters used for drive applications requires many active power factor correction circuits (PFC) due to the demand in high efficiency and low harmonic pollution. Generally, a full-bridge diode rectifier is employed at the input current path so that it produces more conduction losses during low line. To solve this problem, bridgeless converters are proposed to avoid input bridge diode and the

In Figure-1, a bridgeless SEPIC converter with ripple-free input current is proposed is shown. Here, an auxiliary circuit consists of input inductor and capacitor to reduce the input current ripple. In general, coupled inductors are used to minimize the input current ripple [2].

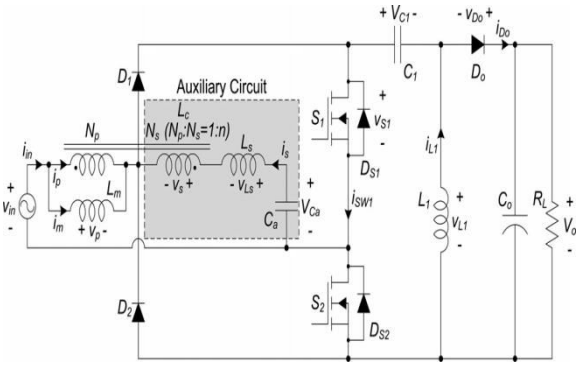

Figure-1. Proposed bridgeless SEPIC converter.

2. ANALYSIS OF THE BRIDGELESS SEPIC CONVERTER

The auxiliary circuit consists of N_s as an additional winding of the input inductor L_c, an auxiliary inductor L_s and a capacitor C_a. TheL_c as a coupled inductor can be exhibited as a magnetizing inductance L_m and turns ratio of the ideal transformer is$1: n(n = N_s/N_p)$.Figure-3(b) shows the proposed gate signals for the switches. One switch is continuously turned ON and current through the intrinsic body diode is forced to run via channel of the switch. So, the conduction loss on the switch can be reduced and improved efficiency. The value of the capacitance C_a is assumed to be high and during switching period V_{Ca} is considered as voltage source. By volt-second balance law, under steady state the average inductor voltage is zero and average capacitor voltage V_{ca} is equal to the input voltage V_{in}during switching period. Likewise,average capacitor voltage V_{C1} is equal to the input voltageV_{in}. The diodes D_1 and D_2 act as input rectifiers. The intrinsic body diodes D_{S1} and D_{S2} of the switches S_1 and S_2simultaneously gets operated by the gate signals as shown in Figure-2(b). The components such as C_1, L_1, D_o, C_o are same as that of conventional converter.

The operation of the converter is similar in both half cycles of the input voltage. So, it is sufficient to analyze the positive half cycle of the input voltage during one switching period. Before the main switch gets turned ON, the output diode D_o is in OFF mode during discontinuous conduction mode (DCM).In order to consider the output voltageV_o as a constant, the value of output capacitor C_o is considered as adequately large. During the switching period T_s, the input voltage is assumed to be constant which is equal to V_{in}.

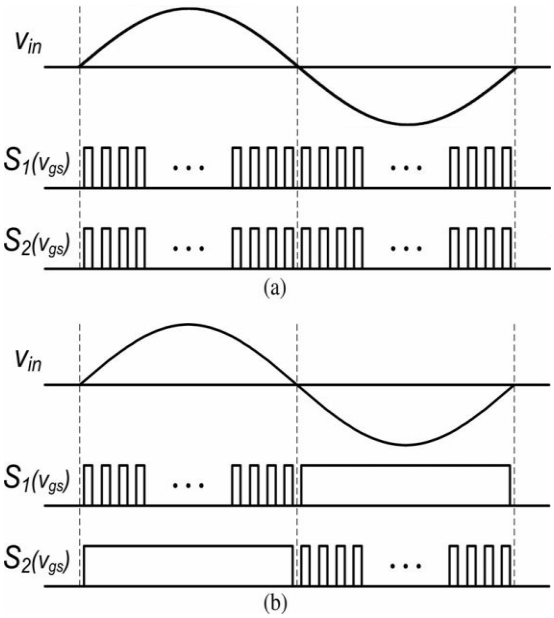

Figure-2. Gate drive signals. (a)Same gate signals for S_1 and S_2. (b) Proposed gate signals for S_1 and S_2.

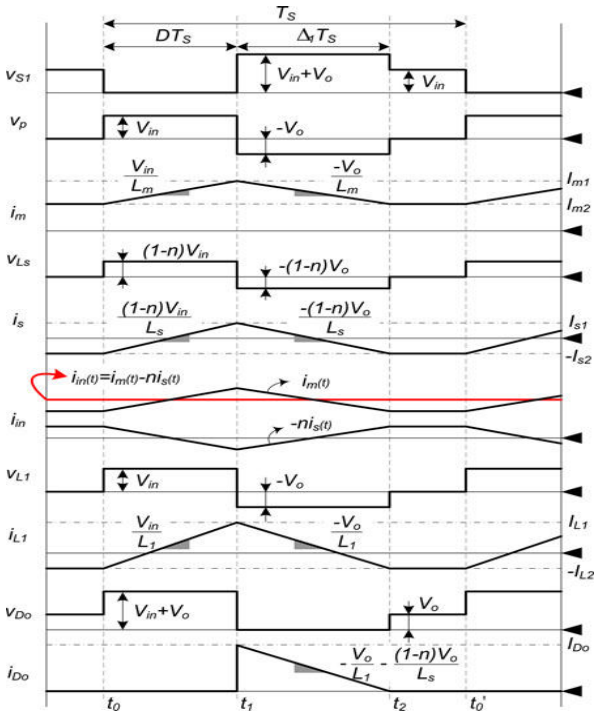

Figure-3. Waveforms of the proposed converter.

The waveform of the proposed system is shown in the Figure-3. Here, the magnetizing current i_m varies from the maximum value of I_{m1} to the minimum value of I_{m2} and also the inductor current i_s varies from the maximum value of I_{s1} to the minimum value of $-I_{s2}$. At one switching period T_s, the operation of the proposed converter can be divided into three modes of operation. The various operating modes of the converter are shown in the Figure-5. The switch S_1 and diode D_o is turned OFF

and the switch S_2 is conducting before the instant T_0. The sum of freewheeling currents I_{s2} and I_{L2} gives the value of the input current.

The operation of the proposed converter with closed loop configuration is symmetrical in two half-line cycles of input voltage. Therefore, the converter operation is analysed during one switching period in the positive half-line cycle of the input voltage. An auxiliary circuit, which consists of an additional winding of the input inductor, an auxiliary small inductor and a capacitor, is utilized to reduce the input current ripple. Coupled inductors are often used to reduce the current ripple. For a half period of the input voltage, one switch is continuously turned ON and the current via an intrinsic body diode is forced to flow through the channel of the switch. It can reduce the conduction loss on the switch.

3. MODES OF OPERATION

Mode 1 [t_0, t_1]: InFigure-4(a), switch S_1 is turned ON and switch S_2 is still conducting at the time instantt_0. The magnetizing current i_m increases from its minimum value of I_{m2} linearly with slope of$\frac{V_{in}}{L_m}$due to the voltage v_p across magnetizing inductance is V_{in}.

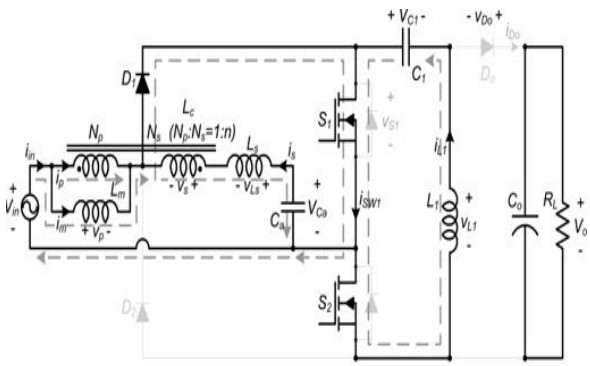

Figure-4(a). Operation of Mode 1.

The voltage V_{Ls} across L_s is $(1-n)V_{in}$ and therefore, the current i_s increases from its minimum value -I_{s2} linearly with a slope of$(1-n)\, in/L_s$.

Mode 2 [t_1, t_2]: InFigure-4(b), switch S_1 is turned ON and switch S_2 is still conducting at the time instant t_1. The magnetizing current i_m decreases from its minimum value of I_{m1} linearly with slope of $-\frac{V_o}{L_m}$due to the voltage v_p across magnetizing inductance is-V_o.The voltage V_{Ls} across L_s is $-(1-n)V_o$ and therefore, the current i_s decreases from its maximum value I_{s1}linearly with a slope of$-(1-n)\, V_o/L_s$.

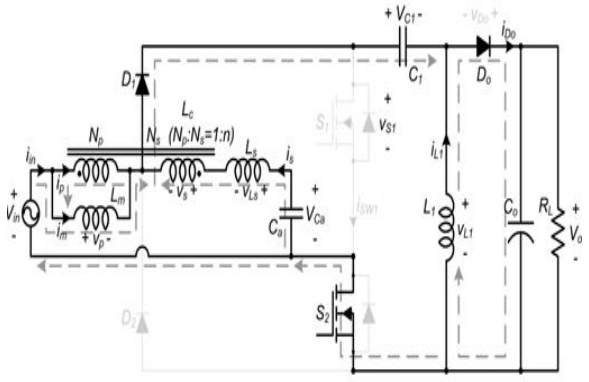

Figure-4(b). Operation of Mode 2.

Mode 3 [t_2, t_0^1]: InFigure-4(c), the current i_{Do} becomes zero and the diode D_o is turned OFF at the instant t_2. The input current i_{in} is the sum of freewheeling currents I_{s2} and I_{L2}. The input current is given as $i_{in} = i_m - ni_s = -i_s - i_{L1}$.

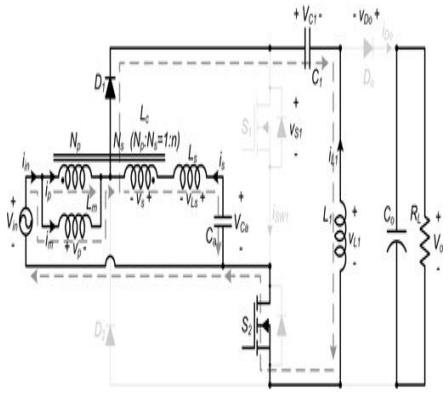

Figure-4(C). Operation of Mode 3.

4. DESIGN VALUES

The proposed converter is simulated by using MATLAB with the specifications and parameters as follows: v_{in}=220 V_{ac}, f_L=60 Hz, f_{sw} = 100 kHz, D = 0.25, L_m= 600 μH, n = 0.7, L_s= 127 μH, L_1= 63 μH, C_a= 0.3 μF, C_1 = 440μ F, C_o= 880 μF, and R_L= 77 Ω.[5].

5. SIMULATION RESULTS

The Figure-5 shows the Simulink model of conventional SEPIC converter. The output from the SEPIC is given as an input to SRM after inverted by inverter.

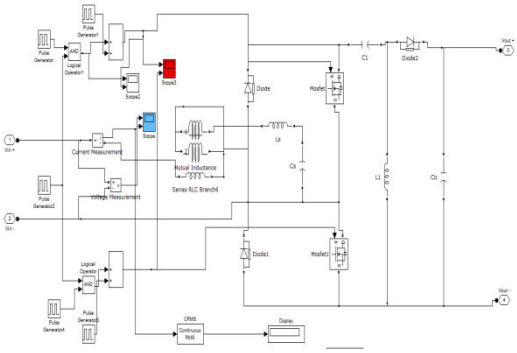

Figure-5. Simulink model of conventional SEPIC.

The Figure-6 shows the output waveform of conventional system. It depicts that the current and torque ripple produced is more. So, the performance of the motor is greatly affected by the converter. The input voltage consists of more ripple current due to the presence of an input bridge diode at the SEPIC. The gate pulses from the pulse generator are used to trigger the MOSFET. The turn ON and turn OFF time of the MOSFET enables the inductor L to charge and discharge. The output is displayed taking flux, torque, current with reference to time. The output waveform implies that more current and torque ripple produced during simulation.

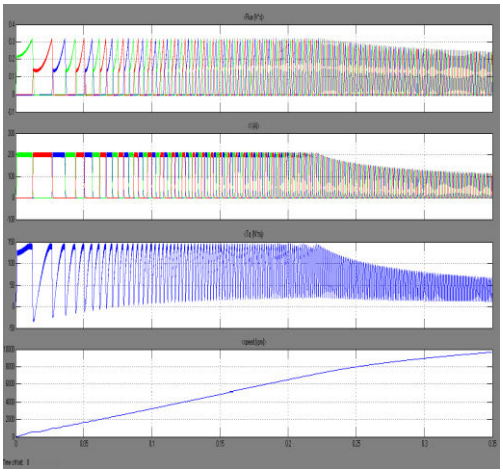

Figure-6. Output waveform of conventional SEPIC.

The simulink model of a proposed bridgeless SEPIC converter is shown in the Figure-7.

Initially, AC voltage source is used as input. This AC voltage source is given to the bridgeless SEPIC converter to produce DC with reduced ripple current, which is given to SRM after converting into AC by an inverter.

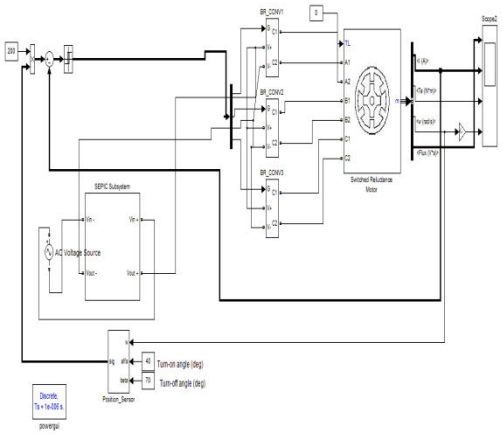

Figure-7. Simulink model of bridgeless sepic converter.

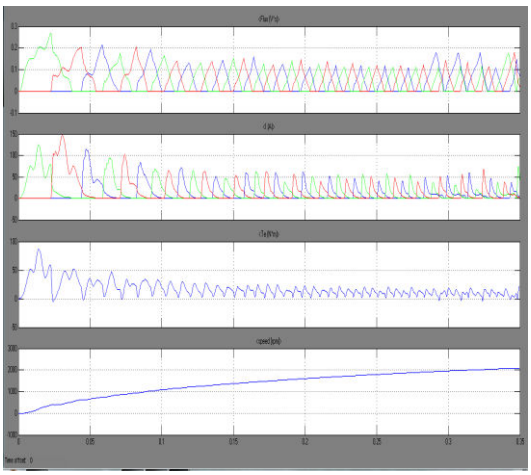

Figure-8. Output waveform of bridgeless SEPIC.

The output waveform implies that current and torque ripple produces is reduced during simulation compared to conventional system is shown in the Figure-8. The outputs are displayed taking flux, current, torque and speed with reference to time.

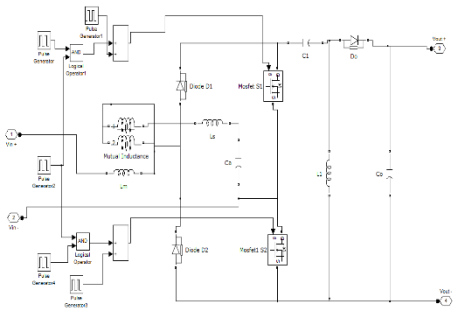

Figure-9. Model of open loop SEPIC converter.

Bridgeless the Figure-9.The output of conventional and the proposed bridgeless SEPIC converter

are given and the reduced output current ripple is also shown in the waveform.[9]

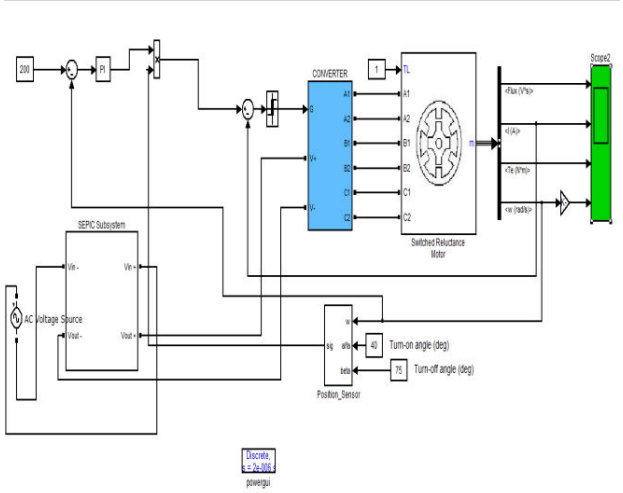

Figure-10. Model of proposed closed loop SEPIC converter.

The output waveform implies that current and torque ripple produces is reduced during simulation and the results were compared with conventional bridgeless SEPIC system is shown in the Table-1. The outputs are displayed taking flux, current, torque and speed with reference to time. The speed obtained using closed loop configuration is constant.

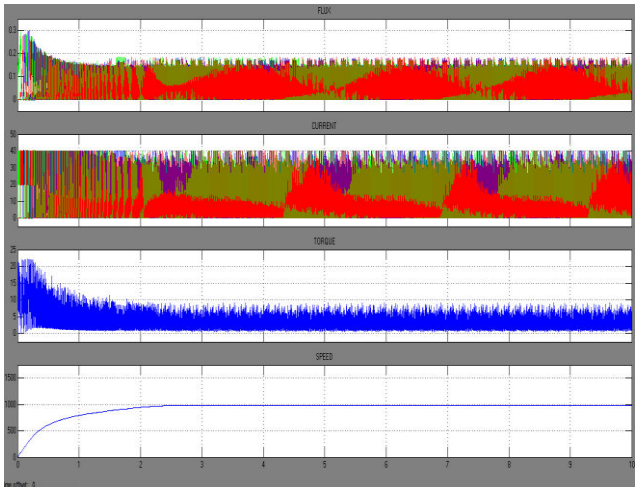

Figure-11. Output waveform of closed loop Bridgeless SEPIC.

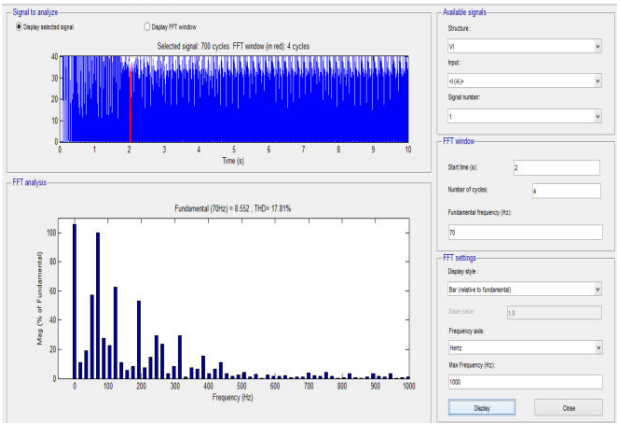

Figure-12. Output waveform of FFT analysis of a closed loop bridgeless SEPIC.

The Figure-12 shows that the FFT analysis of a proposed closed loop operation of bridgeless SEPIC converter and it shows the total harmonic distortion value is also reduced.

Table-1. Comparison results.

Parameters	Open loop bridgeless SEPIC system	Closed loop bridgeless SEPIC system
Flux (v-s)	0.7	0.3
Phase Current (A)	100	40
Torque (Nm)	25	22
Speed (rpm)	2000	1000

6. CONCLUSIONS

The proposed method uses half-bridge switch modules which is more compact and has higher utilization of power switches and lower cost, without degrading in performance. By employing this closed loop bridgeless SEPIC converter, the ripples can be greatly reduced with improved performance .A comparison between the proposed topology and the open loop SEPIC converter shows that the component current ripples and the THD values are lower in the presented topology. In low-voltage high-current applications, the proposed topology can be more beneficial than a conventional open loop SEPIC converter. Thus, the simulation and its outputs have shown that the output have a tendency of improved performance with reduced torque ripples throughout its operation and it can be used in medical application such as .The theoretical analysis, simulation results and experimental results were provided.

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