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# A LITERATURE SURVEY AND INVESTIGATION OF VARIOUS HIGH PERFORMANCE DOMINO LOGIC CIRCUITS

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**ABSTRACT**

In deep sub-micron regions, the dynamic power and abstaining reliability problems will be reduced when the power supply voltage was trimmed down. The consumption of power in highly performing circuits has climbed to the level where it enforces the most important limitation to the rising performance and functionality. If power consumption is keep on increasing then the highly performing circuits will start to intake power in terms of more than thousands. The foremost factor in CMOS technology based design is dynamic switching power which can be reduced by reducing the supply voltage. If the supply voltage is reduced then it automatically reduced the transistor current which affects the speed of the circuit. The threshold voltages are scaled down so that it will compensate the speed of the circuit which was affected because of lowering the supply voltage. It also helps to maintain the dynamic power consumption with sufficient level without affecting the performance of the circuit. As a result of threshold voltage reduction the sub threshold leakage current starts increasing exponentially. It will be a tremendous boost in the designing of energy efficient circuits which was focusing on lowering the leakage current. The domino logic circuit design techniques are suitable for highly performing circuits for its higher speed and uniqueness of area in comparison with Static CMOS Circuits. The noise margin illustrates significant reduction if the domino logic circuits were operated in deep sub micrometer. In this paper, a literature survey and investigation of various domino logic circuits have been carried out stating their features, advantages and disadvantages in a profound manner.

**Keywords:** domino logic circuit, dynamic power, full-swing, power delay product, threshold voltage, supply voltage, reduced-swing, keeper transistor, sleep switch.

## 1. INTRODUCTION

Domino logic is a cascade structure which consists of many stages, each stage was evaluated and the output was rippled to next stage as input and it will be continued for the whole circuit. It is one of the dynamic logic technique based on CMOS and it was designed using either NMOS or PMOS transistors. The technique was developed to increase the speed of the circuit. The states of the nodes will not return to 1(HIGH), unless the next clock cycle and once fallen it could not recover [1]. Hence the structure is referred as Domino logic, which is the well-liked dynamic logic and it operates maximum of 2X times quicker compared to static CMOS logic, as the dynamic gates suggest less input capacitance for the similar output current and a switching threshold also get reduced [17] – [20]. The operation of Domino logic circuits is an identical style as that of clocked CMOS circuit. Here, for precharge and evaluation phases a single clock was used for a cascaded series of dynamic logic blocks. The domino logic circuit integrates the entire individual static CMOS buffer transferred into the logic gate. Figure 1 shows the articulation of domino logic circuit. In the phase of precharge (Clock = LOW), the dynamic node of all dynamic gates are precharged to "1" via pull up transistor, thereby the final outputs of the subsequent buffers was precharged to "0". All the transistors of subsequent dynamic gates are nourishing from buffers, so that they are all turned OFF.

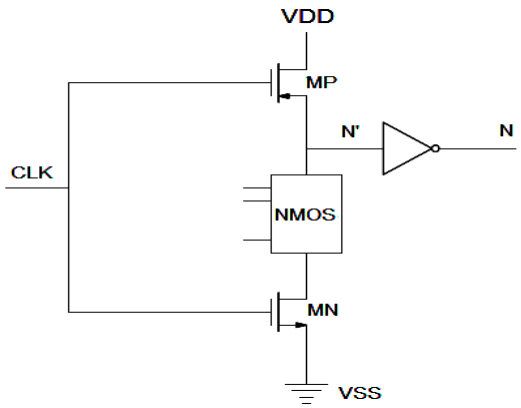


**Figure-1.** Articulation of domino logic circuit.

In the phase of evaluation, dynamic node is either maintained in HIGH or discharged through the Pull-down transistor (MN) based on the given function. So the final output of the buffers either goes LOW or remains HIGH respectively. In Domino logic, it is important to note the transition of the dynamic node is at all times from LOW level to HIGH level. There exist a cascaded series of logic blocks, the evaluation phase outcome of the succeeding stage to evaluate and process was continued. Apparently, cascading within the evaluate phase of the clock several number of logic stages can be evaluated. The paper has

been organized as follows. An introduction to domino logics and their features have been vividly elaborated in Section 1. The related work on conceptual description of power dissipation and circuit techniques has been discussed in Section 2. A literature survey of various types of domino logic circuits with their features has been entailed in Section 3. Finally at the last section conclusion of the paper was mentioned.

## 2. RELATED WORK

There are two distinctive classes of power dissipation concerned in the CMOS circuit's namely dynamic power dissipation and Static power dissipation. In case of dynamic power dissipation, both PMOS and NMOS devices are ON simultaneously for particular time during the functioning of the circuit. The input and output transition times decides the duration of the time interval. During this time interval, a pathway occurs between Supply Voltage (Vdd) and Ground (Gnd) and a short-circuit current of minimum flow occurs. But it does not affect the major factor in dynamic power dissipation [2]. The essential constituent of dynamic power dissipation starts from transient switching of the nodes. The signals in CMOS devices produce charging and discharging of parasitic capacitances between the two logic levels HIGH & LOW. The dynamic power dissipation is proportional to the square of supply voltage. The threshold and supply voltages for CMOS transistors in deep sub-micron techniques are significantly reduced down which results in reduction of dynamic power dissipation to a great extent. In static power dissipation, the power dissipation occur only when no transitions occur and a leakage current flow through the transistor during the steady state condition of the transistor. Leakage power depends mainly on the length of gate in addition to the thickness of oxide and varies exponentially with threshold voltage. In CMOS transistors reduction in threshold voltage and supply voltage offers a reduction in dynamic power dissipation.

To reduce the power few different techniques were proposed in domino logic circuits: Standard Single low Threshold Voltage, Standard Single High Threshold Voltage, Standard dual threshold voltage and Modified dual-Vt technology.

a) Standard Single Low Threshold Voltage: This method proposes that every standard low Vth voltage transistors of $V_t$ = 0.4 volts have been employed for implementation. The low-Vt transistor methodology provides minimum propagation delay by the transistor.

b) Standard Single Threshold Voltage: This method proposes that every standard high Vth voltage transistors of $V_t$ = 0.7 volts have been utilized for implementation. This method endow with comparatively lesser leakage current and power dissipation.

c) Standard dual threshold voltage: The necessity for integrated circuits with less delay, low power dissipation, higher integration density along with superior performance may be achieved by the formulation of a downscaling technology and reducing of the supply voltage. To suit these requirements, the threshold voltage of transistor has to be down scaled which results in increase in the sub-threshold leakage current owing to increased leakage power. A core approach of reducing the leakage current of sub-threshold is by means of dual-threshold CMOS design technology [3]. It uses the mixture of fast low threshold voltage (FLTV) and slow high threshold voltage (SHTV) devices. Then the focal objective of DTCMOS is to perk up the increase in leakage at the slow high threshold voltage devices without deterioration of circuit performance. This decreases leakage to a greater extent, but the performance shall be reduced when compared to the CMOS technology. The combination of PMOS with high-Vt and NMOS with the low-Vt devices transistors in the output inverter has been used.

d) Modified dual Vth technology is the updated version of standard dual Vth technology. In the modified dual Vth technology a high Vth transistor was introduced at the output inverter in domino logic in the standard dual Vth technology. In this modified dual-Vt methodology, Standard high Vth transistor with pull-down transistor and standard low-Vt transistor with pull-up transistor has been introduced for better performance.

## 3. LITERATURE SURVEY OF VARIOUS DOMINO LOGIC CIRCUITS

### 3.1. Standard domino logic circuit

The standard domino logic circuit [4], [16] comprises of a static inverter and n-type dynamic logic block. During the phase of precharge, the output of the dynamic gate will be charged to the supply voltage (Vdd) and the output of the inverter is set to "0". During the phase of evaluation, conditional transition from zero to one was carried out by the inverter. All the inputs must ensured to be "0" at the last part of precharge phase and changeover should be "0" to "1" at the time of domino gate is fed into its subsequent domino gates. If the previous stage assesses to "1" and a high fan-out has been achieved then the dynamic node discharges due to the existence of static inverter at the output. A keeper transistor was introduced to neutralize the leakage issues and to set up the low impedance path in the feedback path. The lost charge due to pull-down leakage path was taken care by the keeper transistor.

The keeper is fully turned ON at the commencement of the evaluation phase. The speed of the circuit gets degraded by the contention between pull down network and keeper transistor at the time of pull down network is ON. The size of the keeper is minimized to reduce the power and delay degradation also it cannot offer essential noise immunity for reliable operation. So there occurs the tradeoff between high speed operation and reliability. The standard domino logic circuit has been shown in Figure 2.

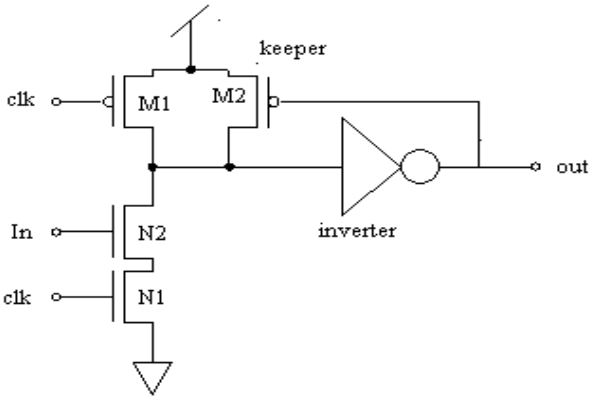


**Figure-2.** Standard domino logic circuit.

### 3.2. Dual threshold domino logic

In general we use to represent high Vth transistors with double channel lines [5]. The speed of the circuit was decided by the transistors in the significant evaluation path. In dual-Vth domino circuit, low Vth and high Vth was assigned to the active transistors in the evaluation phase and precharge phase respectively. The leakage current was reduced significantly, when high Vth transistors are forced into cutoff during idle state compare to low Vth in the circuit. During the idle state of domino logic the clock value is assigned high removing the pull up transistors and leakage current in high Vth is comparatively low comparing to Low Vth. If the count of high Vth was increased the leakage current will be reduced considerably. The potential energy is fully exploited only if high Vth have strong cutoff. Dual threshold domino logic suppresses the leakage current which results in total power dissipation reduction. Figure 3 shows the Dual threshold domino logic circuit.

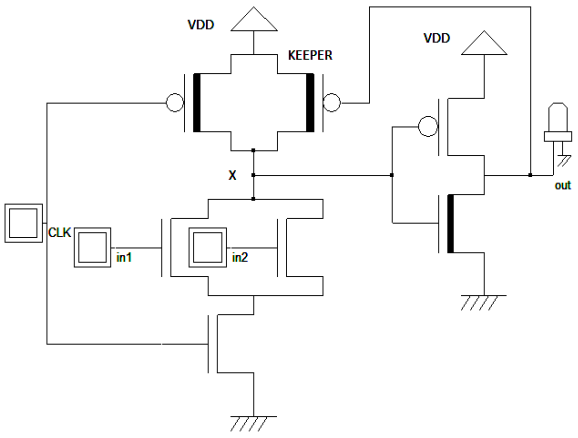


**Figure-3.** Standard dual-Vth domino circuit.

Every transistor activated during evaluation phase includes low Vth and pre charge phase transistors with high Vth are not vital for efficient outcome of domino logic circuit. When all the high-Vth transistors compared with low Vth transistors at cutoff in dual Vth domino logic circuit, the sub threshold leakage current was greatly minimized. The input vectors that are applied after the clock is gated high will determine the modes of the remaining high Vth transistors in standard dual domino logic techniques. Eventually, in the standard dual domino logic technique energy and delay overhead issues were not discussed for coming in and go away in its stand-in mode.

### 3.3 Stacked transistor dual threshold voltage technique

In Stacked Transistor Dual Threshold Voltage (ST-DTV) technique involves both active and standby mode in the mechanism to minimize the leakage current in the circuit. This method is based on the observation that leakage of the circuit is less in two off-state transistors that are connected in series compared to a single device. If we increase the single device channel length by twice the leakage current of the stack will afford significant reduction. The ST-DTV technique [6] was illustrated in the Figure 4. The method involved in this method is splitting up the existing transistor into two and both the transistors length and width were scaled down to half of the existing transistor. Here the transistor M1 and M4 are stacked so that the two half sized transistors M1,M2 & M3, M4 too.

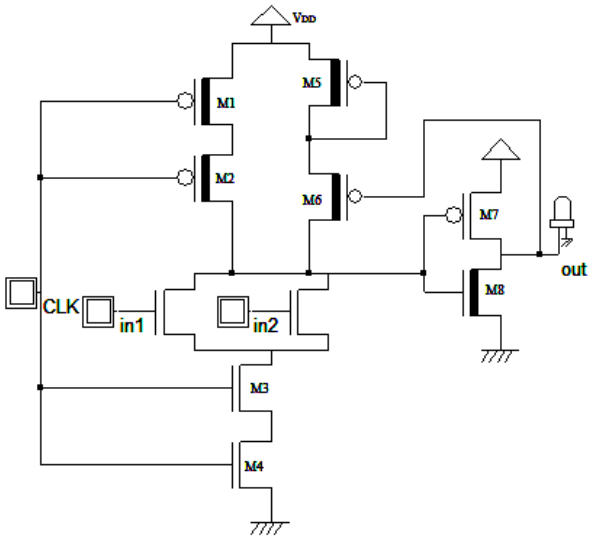


**Figure-4.** ST-DTV technique.

When the two halved transistors are switched OFF at the same time, then the provoked reverse bias stuck between the 2 half sized transistors results in the decrease of leakage current. The propagation delay is inversely proportional to the stack intensity so to reduce the speed of the circuit it is mandatory to increase the transistor stack. At the same time the circuits fails if the depth of the stack is increased due to charge sharing. The

value of clock is '0' then M1, M2 transistors will be assigned ON state and M3, M4 transistors will be assigned OFF state. This result, the evaluation node to precharge to the value VDD and the output of the CMOS inverter maintained to be low. When the clock becomes HIGH, the stacked pMOS transistor is OFF and nMOS transistor is ON in the evaluation phase. The evaluation node maintained in HIGH or change from "1" to "0" transition depending on the input combinations in pull down network [5], [6]. So the technique assists in the abating of sub threshold leakage current which reduces the power consumption in the circuit.

### 3.4. Sleep switch dual-Vth domino logic circuit

During an idle mode in domino logic circuit, the technique makes use of the sleep switches to locate the dual Vth and fetch down the state of low leakage by making use of a single clock cycle, which leads to the reduction of sub threshold leakage current. A 2-input OR gate using domino logic circuit with sleep switch dual-Vth circuit technique [7] has been figured out in Figure 5. A high-Vth NMOS switch has been added along with the dynamic node of the domino circuit. A separate sleep signal was used to control the functioning of the high Vth transistor. The sleep signal was maintained at the LOW level in the active mode which helps to cutoff the sleep switch so that the circuit behaves as Standard dual Vth domino circuit.

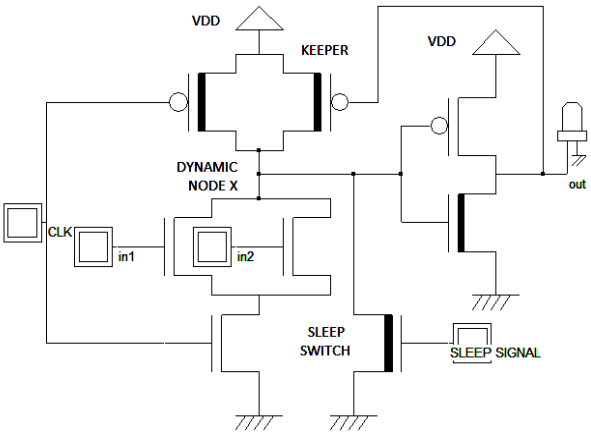


**Figure-5.** Sleep switch dual Vth domino logic circuit.

On the other hand, the clock signal is set to HIGH during the standby mode of operation, which turns OFF the high pull-up transistor of each domino gates. To turn ON the sleep switch the sleep signal value has to set as HIGH. Once the sleep switch is ON the domino gates dynamic node started to discharge via sleep switch by turning OFF the high Vth transistor of the output terminal. So the output transition will change from LOW to HIGH by cutoff the high Vth keeper. Then the succeeding gates also started to discharge in domino fashion due to the output transition from LOW to HIGH. The dynamic node voltage settle down to steady state, the sub threshold leakage current will reduce significantly with every high-Vth transistors getting strongly cut-off. A single clock cycle strongly turns off the high Vth transistors and the technique doesn't impose any additional gating on the input signals. So compared to standard dual-Vth technique this methodology afford momentous reduction in power, delay and area.

### 3.5 Modified dual-threshold domino logic circuit

The Modified dual-threshold domino logic circuit is an amendment of standard dual-threshold technology. In standard dual-Vt technology, high Vth transistor was introduced at the output inverter circuit but in modified dual-threshold domino logic circuit standard high Vth and standard low Vth transistors have been set up at pull down and pull up transistors respectively. During the pre charge phase the output of the circuit will be at logic '0' [8]. Since the output is logic '0' the second stage could not able to estimate the function while constructing a pipeline structure. So the modified dual-threshold domino logic circuit was set up to resolve this problem. During the Precharge phase the clock is gated to "0". In the evaluation phase the clock is gated to HIGH so that the logic function is evaluated based on inputs. During the phase of pre charge, the output will be hold in the clock which was under the control NMOS transistor which was put in at the discharge path of output inverter.

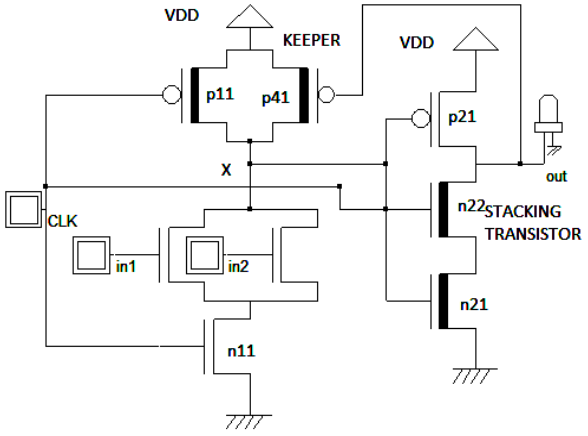


**Figure-6.** Modified dual-Vth domino logic circuit.

There is no path exists for charging or discharging in the pre charge phase because if the clock is gated with "0", p11 will be ON state, both n11 and n22 will be OFF state. So the dynamic node X is pre charged to supply voltage (Vdd) by p11 and p21 will become OFF. So the output of the circuit is Tri-state and does not hold on to its previous state values in it.

### 3.6. Standby switch domino logic circuit

A lower energy and lower delay overhead a dual Vth methodology was proposed to prevail over the inadequacy of the existing domino logic circuit

configurations. To place a lower leakage position in a dual Vth domino logic circuit [9] within a single clock cycle it introduces a standby switch. It was investigated to trim down the sub threshold leakage currents in its idle mode as depicted in Figure 7. A Low Vth estimation block was connected with high Vth NMOS transistor (standby switch), which is separated by standby clock and used as discharging path for the node X. In a single clock cycle with a help of standby switch the circuits entry and leaving in the standby mode was done with ease.

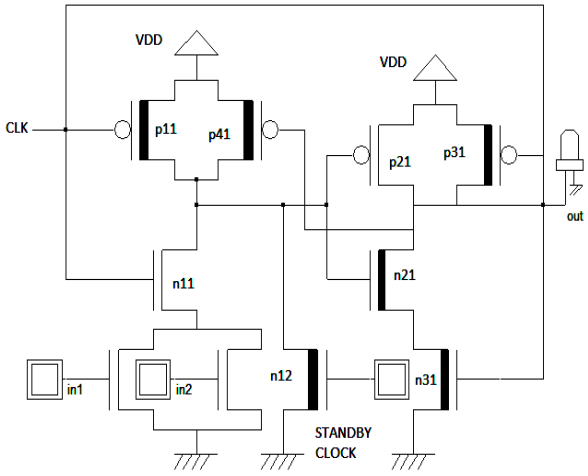


**Figure-7.** Standby switch domino logic circuit.

In case of conventional domino logic to precharge both the dynamic node X and output to supply voltage (Vdd) to logic HIGH, a CMOS NAND gate was bring in as an alternative of output inverter. So that during evaluation phase succeeding stages will be evaluating its logic function endurably. At Precharge mode (Clock is LOW) the transistors p11 and p31 was in ON condition at the same time n11 and n31 will be in OFF condition. So both the node X and output of the circuit is pre charged to Logic 1 (VDD) by the transistor p11 and p31 irrespective of the state of standby-clock. During this period of time the evaluation and standby phases were not controlled by NAND gate configuration. The key difference between the Dual and Standard dual Vth domino logic is the presence of Precharge and standby phases in former domino logic. The high Vth pull up transistors p11 and p31 are turned OFF and pull down transistors n11 and n31 are turned ON in standby mode (Clock is HIGH). Once the standby transition reaches HIGH state it will turn on the standby switch n12 and the dynamic node X started to discharge via n11 and n12. This leads to turn ON the p21a PMOS transistor and turn OFF the n21 a NMOS transistor.

The output of the circuit is charged to Logic HIGH (VDD) by cutting down the p41 a PMOS transistor. Subsequent to the "0" to "1" transition in the output of the circuit all the succeeding gates started to discharge in the domino fashion. If the voltage node is settled down to steady state value then the high Vth transistors will be robustly cutoff so that the sub threshold leakage current is reduced significantly. Even though within a single clock cycle all the high Vth transistors have been turned OFF it does not require any additional gating in the input signals. The dynamic mode X maintains Logic "0" in the standby mode irrespective of input vectors of Low Vth evaluation block to avoid floating state. This will result in large leakage current in the output inverter. The circuit can be differentiated from traditional domino logic by shifting the standby switch n12 from dynamic node to source of n11. This operation improves the speed of the circuit and low down the capacitance load effects in the dynamic node. The enhancement of body effect of n11 was carried out by connecting the discharging transistor of Low Vth evaluation block from ground to dynamic node. It also increases the Vth and reduces the cut off leakage current. The Standby switch domino logic circuit offers an effective Power, delay and also shows better efficiency in area too.

### 3.7. Standard Footless Domino Logic (SFLDL) Circuit

The footless scheme [10] is characterized by the feature that the discharge of dynamic node is much faster. This property is exploited by the high-performance circuits. The circuit of SFLD logic is shown in Figure 8.

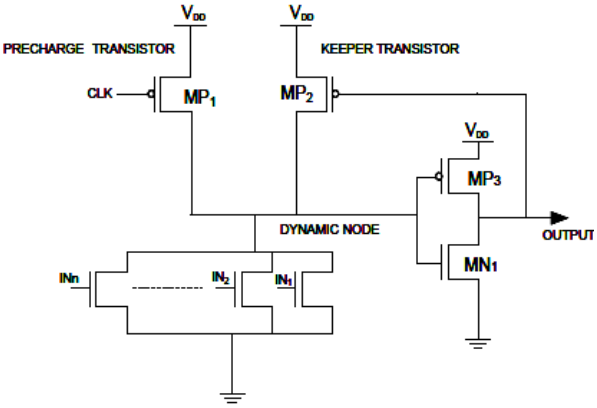


**Figure-8.** Standard footerless domino logic circuit.

The functioning of footless domino is as follows: In Precharge phase, When Clock is "0": The dynamic node is charged to Supply Voltage (Vdd) and keeper transistor MP2 is turned ON to maintain the voltage of the dynamic node. In Evaluation phase, When Clock is "1": Depending on the input combination of the circuit the dynamic node will be in the state of HIGH or discharged to ground.

The keeper transistor size should be small enough to lessen the contention current between keeper transistor and NMOS pull down transistor at the same time it should be large enough to compensate for charge sharing problems. The dynamic node will be evaluated to logic level '0' with the help of pull down network. If both the pull down and keeper transistor compete with each other

to drive the output of dynamic node then it will lead to two opposite directions which is a distinct effect referred as contention. This also results in the degradation of speed in the circuit as well as increase in power consumption.

### 3.8. High Speed Domino Logic (HS)

In High Speed (HS) domino logic, the combination of output and delayed clock are accountable for the keeper transistor operation. During the commencement of evaluation phase (Clock is "1") operation, the keeper transistor MP2 turns OFF and MP3 turn ON. By making the clock value HIGH the contention will get reduced between the evaluation network and keeper transistor. At the same time the keeper transistor will be in OFF condition at the commencement of evaluation node. When the delay of the two inverters become equal then the transistor MP3 gets turn OFF. If the dynamic node getting discharged to ground i.e., any input value is "1" then NMOS transistor MN1 remains OFF. At this moment of time, then the voltage at the keeper gate will be the difference of supply voltage and threshold voltage (VDD - Vth) and not VDD so that it allows the path of higher leakage current to pass through the keeper transistor. Incase during the evaluation phase if dynamic node remains HIGH, MN1 turn ON and that heave the gate of keeper transistor. So the keeper transistor should be turned ON to maintain the dynamic node to be HIGH and thus it reduces the effect of leakage. This high speed domino logic technique has the merits of excellent power reduction, propagation delay and low power delay product. The high speed domino logic [11] circuit is displayed below in Figure 9

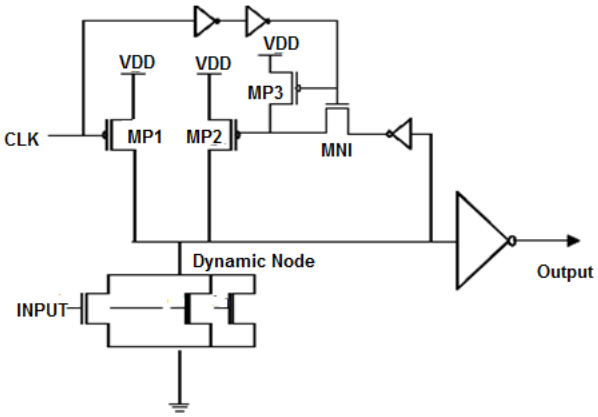


**Figure-9.**High-speed domino logic.

### 3.9. Conditional Keeper Domino Logic (CKD)

In Conditional Keeper Domino Logic two keeper circuits were involved [12]: a small keeper and a large keeper. In this method, the keeper device (PK) in conventional domino is sub-divided into two smaller ones: PK1 and PK2. The keeper sizes are selected in such a way that PK=PK1+PK2. Such sizing insures the same level of leakage tolerance, because of the conventional gate but yet improving the speed. During the pre charge phase (Clock is "0") the pull up transistor is switched ON which lead to the dynamic node to start charging supply voltage (VDD). Thus the noises immunity of the circuit is improved significantly in conditional keeper domino logic and it was shown below in Figure 10.

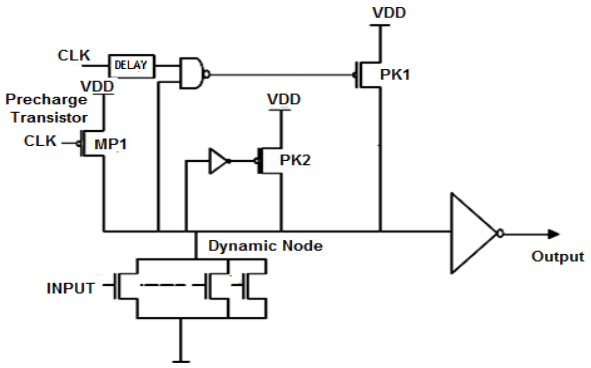


**Figure-10.** Conditional keeper domino logic.

At the commencement of the evaluation phase (Clock is HIGH), the large keeper PK1 and pre-charge transistors will be in the state of OFF. The dynamic node will remains HIGH during the standby mode, all the inputs value are LOW logic level where the delay of two inverters will be equal. This act leads to the output node of the NAND gate to LOW, which causes the larger keeper PK1 to be turned ON. In order to prevent the erroneous discharge of dynamic node the larger keeper is arranged in such a way that both the inverters delay will be same. During this operation all the inputs remain in LOW state. To compensate the charge leakage the small keeper PK2 is maintained in ON state until large keeper PK1 has been activated. By using small contention current to the pull down network the speed of the circuit was improved and also remains sufficient to maintain noise immunity.

### 3.10. Split Domino Logic (SDL)

There are numerous parallel branches in large fan-in dynamic OR gate. The NMOS pull down network results in a large quantity of leakage current occurs if the dynamic node is maintained at supply voltage (VDD). The propagation delay increases due to large parasitic capacitive effect, because this parasitic capacitance should be discharged to zero during evaluation. In Split-domino logic is an incredible technique where the pull down networks was spitted into smaller group with small sized keeper in both circumstances results improvement in the internal operation of the gate. For that reason, theoretically two keeper transistors are required with a width almost half as that of the conventional circuit. Figure 11 displays the 16-bit domino OR gate split in two sections. The circuit overhead is not as much as it might appear, because there are two static inverters in the conventional domino circuit in the place of two and three input NAND gates, and besides this they could be implemented using

minimum sized transistors. The circuit overhead is nearly the same as that of conditional keeper technique [13].

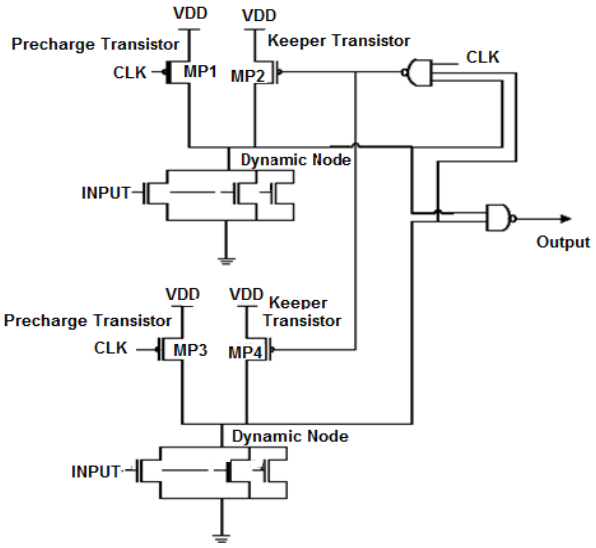


**Figure-11.** Split domino logic circuit.

### 3.11. Diode Footed Domino (DFD)

The diode footed domino logic [14] was designed from existing general domino logic circuit by adding up a NMOS Pull down transistor M1 in succession with the footer of the evaluation mode. The NMOS transistor was configured using diode, so the terminals of gate and drain were connected together. The circuit diagram of diode footed domino configuration was shown in Figure 11.

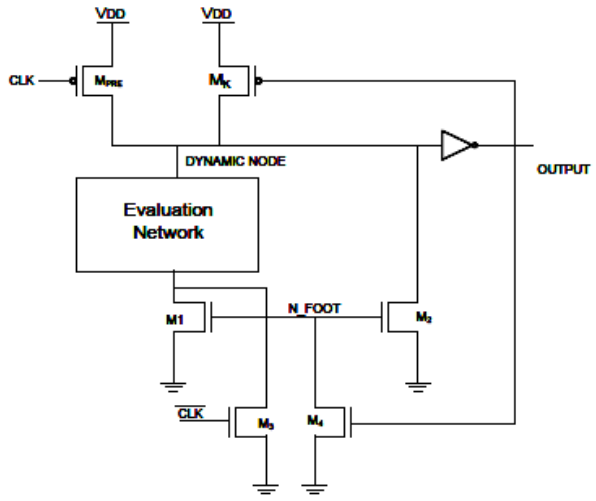


**Figure-12.** Diode footed domino logic.

The added NMOS transistor creates stacking effect since it was connected in succession with evaluation network. As a progression of stacking effect the circuits sub threshold leakage current and robustness gets improved in terms of performance. The current mirror has also been employed in the pull down network to increase the evaluation current and speed of the circuit. The robustness in the diode footed domino show good improvement when compared to existing domino logic circuits under the same delay.

### 3.12. Three Phase Domino Logic Circuit

Generally the circuit performance is prejudiced by input at all time and noise may have any time period in static logic circuits. For the most part of awful case it is implicit that, the DC noise may appear in the input of the circuit, hence the static noise margin has been engaged to estimate the worst case noise margin [15]. The circuit is sensitive to the inputs, if the evaluation time is limited which will lead to increase noise margin and affects the output of the circuit. In logic family noise duration is limited by limiting the evaluation time duration which was influenced by input also results in limited time. In that particular issue the dynamic noise margin ought to be engaged in the process and three phases were involved in this domino logic family.

The Precharge phase is the first phase where the input should not influence the output at the same time the circuit is all set for the next phase to begin. As soon as all the inputs are ready to process the evaluation phase begins its operation of execution and outputs illustrate the change depending upon the input values. The change in the output will have an effect on the circuit and it's the only phase where the output of the circuit is changed. So particularly in this phase noise started to influence the output of the circuit.

After the end of evaluation phase the values evaluated are saved for the next stage of circuit operation. The next stage to evaluation phase is save phase in which the design of circuit should not have an effect on the phase irrespective of inputs. In the Clock – Delayed domino logic the clock signal is propagated in parallel with the logic and the delayed form of clock is fed as clock signal for further stages. The rising edge of the clock will initiate the evaluation phase and clock delay is designed in such a way that all the inputs are all set for process. The three phase domino logic circuit is shown in Figure-13. The CLKD signal is designed in such a way that it was a delayed version of CLK. The PFET transistor used in the Save phase is comparatively larger than the keeper transistor which are used in usual domino gates. Then in the design the NAND gate was replaced for the NOT gate. In the Precharge phase the value of supply voltage was charged to dynamic node such that the footer transistor is OFF and the transistor MP1 is ON. Since the footer transistor is in OFF condition the inputs won't affect the dynamic node. When the valuation phase arrives the value of CLK = 1, which will turn ON the footer transistor and the MP1 transistor is pushed to OFF condition. Depending on the input values the evaluation was carried out to compute the output of the circuit. In this phase the PFET are in OFF state will allow the pull down transistor to discharge the dynamic node so faster than expected. The

save phase was initiated once the CLKD charges to VDD and NAND gate started to influence the operation of the circuit. If the dynamic node is discharging the output of the NAND gate remains in High and as a result the save transistor remains in Low. In case if the dynamic node is not discharging the NAND gate value is Low and as a result the save transistor state becomes High. So the dynamic node is associated to supply voltage through the PFET save transistor. If the dynamic node is discharged the PFET save transistor is sturdy enough to maintain the dynamic node voltage to be superior to the threshold voltage.

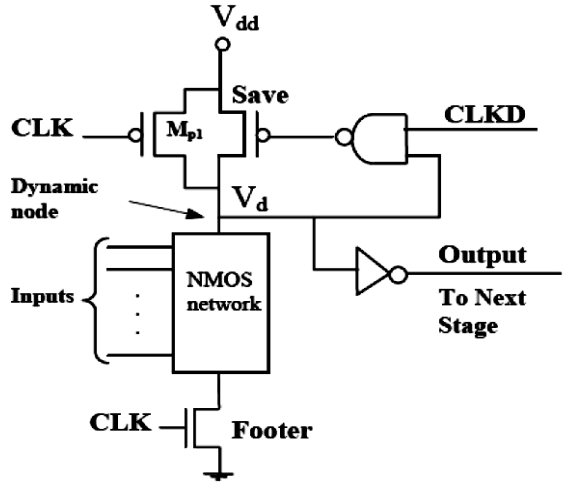


**Figure-13.** Three phase domino logic circuit.

## 4. CONCLUSIONS

Domino logic circuits were engaged in large array of applications such as microprocessor, memory, digital logic, etc. It has enormous advantages than static logic circuit, entails lesser number of transistor counts, reduces the output load capacitance and hence enhances the operating speed. In this paper, a detailed introduction about domino logic circuits, their features and advantages have been elaborated in a profound manner. Also the power dissipation and circuit techniques have been detailed. A literature review and of various domino logic circuits has been carried elaborated stating their distinct features. It is clearly inferred that the leakage current was suppressed by dual threshold domino logic thereby reduces the total power dissipation. Stacked transistor dual threshold voltage technique abates the sub threshold leakage current which in result power consumption also reduced significantly. The sleep switch dual threshold voltage technique shows better reduction in Power, improvement in delay and reduction in area in contrast with standard dual-Vth domino logic. The high speed domino logic circuit shows excellent reduction in power, enhancement in propagation delay and power delay product was improved significantly. The conditional keeper domino logic circuit improves speed and also maintains the noise immunity. The diode footed domino logic improves the robustness when compared to standard footless domino and conditional keeper domino under the same delay. As a future work, few domino logic circuits shall be implemented and simulated for projecting its performance compared to the existing domino logic circuits.

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