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FPGA BASED DESIGN AND IMPLEMENTATION FOR DETECTING CARDIAC ARRHYTHMIAS

D. Hari Priya[1], A. S. C. S. Sastry[2] and K. S. Rao[1]
[1]Department of Electronics and Communication Engineering, Anurag Group of Institutions, Hyderabad, India
[2]K.L University, Andhra Pradesh, India
E-Mail: haripriyaece@cvsr.ac.in

ABSTRACT

Detection of arrhythmias by processing ECG has become vital. The QRS complex being a dominant feature of ECG places a key role in identifying Cardiac arrhythmias. The QRS complex being detected by 17 Hz band pass filter and shaped into a square pulse of 200ms width representing R peak by other circuitry is utilized in this work. Various arrhythmias are identified based on abnormalities in the time intervals between consecutive R peaks using Tompkins algorithm is presented. The algorithm is implemented in FPGA Spartan3.The algorithm is written in Verilog HDL and tested on Xilinx 13.1 ISE. The simulated test results have shown the detection accuracy around 99.3% and dynamic power consumed is 22mW.

Keywords: cardiac arrhythmia, tompkins algorithm, CSA and wallace multiplier.

INTRODUCTION

With the advent of integrated circuit technology rapid developments were introduced in the present day market in the form of portability, battery operated devices. Especially the biomedical instrumentation field, devices like heart rate monitors based on ECG has become very popular. Small size and low power consumption are of prime importance in such type of portable devices.

In medical instrument the weak bio signal (less than few mV) needs to amplified and filtered for further processing. An instrumentation amplifier was built using discrete components can be utilized as presented in [1]. However by the design of a fully custom IC the power consumption and size can be reduced to a significant level [2]. Further if the circuits needed for all the other functions were integrated on the same chip, the space and power consumption can be reduced.

When aiming for low power consumption the circuit must be operated with low voltage. Since the average power consumption is proportional to the square of the supply voltage in digital circuits [3], it is the most efficient method to achieve low power consumption. But in analog circuits the power consumption is proportional to the dynamic range of the circuit [4] and hence cannot be reduced by reducing the supply voltage.

To identify cardiac arrhythmias the pulse is usually detected on the basis of the largest peak in ECG signal, known as the QRS complex. The morphology and amplitude of QRS complex contains higher information and provides significant contributions to physicians for diagnosing heart diseases. QRS detector is presented in Holter tape recorder for analyzing the tapes faster. Many researchers have developed algorithms for accurate detection of QRS complex with offline data [5]. Portable and real time arrhythmia monitor is needed to monitor high risk heart patients [6]-[8]. In home care ECG monitoring, the abnormal ECG information is transmitted to other end where physician can interpret the ECG data. This will transmit the unwanted data in case of faulty QRS detection also. Hence research for an accurate QRS detection algorithm is necessary for the interpretation of automatic ECG diagnosis.

Muscle noise, artifacts due to electrode motion, power-line interference, and baseline wander, and T waves with high frequency characteristics similar to QRS complex make the QRS detection complex. Digital filters are used to remove the noise and improve SNR. QRS complex degradation by undesired noise sources can be prevented by specific QRS template. Linear digital filtering, nonlinear transformation, and decision rule algorithms are important processing steps of Software QRS detector [9].

Based on analysis of slope, amplitude and width of QRS complex, Pan Tompkins presented a real time QRS detection algorithm [10]. A novel method is introduced based on simple moving average with wavelet based denoising for real time QRS detection. The digital filters and FFT are used to extract the feature components of QRS complex. The features are changing with physical variations and noise.

Beyond QRS detection, many works have been proposed in related fields like signal enhancement or pattern classification. Adaptive wavelet algorithm was proposed for recognition of normal beat and cardiac arrhythmias. Two sub-networks are cascaded in the recognition system. In the first sub- network, the activation functions take the Morlet wavelets and were responsible for extracting features from each ECG signal. The second sub-network, a probabilistic neural network (PNN) [5], is used to classify cardiac arrhythmias.

The morphologic features of QRS complex could be also performed in the frequency domain in order to find changes in QRS complex power spectra between normal and arrhythmic waveforms [11]. In this case Fourier

transform shows the changes in QRS complex due to rhythm origination and conduction path in order to discriminate by a neural network. A more deep analysis of ECG Fourier Transform for QRS features extraction and classification was proposed [12]. There were methods of the principal component analysis (PCA), the adaptive resonance theory (ART), the wavelet neural network (WNN), or the fuzzy neural networks (FNN) [13], Fuzzy C-Means Clustering Neural Networks (FCMCNN) method [14] and LMNN classifier [15].

The FPGAs have become popular in medical systems due to their rapid prototyping capability [15]. It is more flexible and provides potential alternative for hardware design [16] and are most popularly used for reconfiguration purpose. The Dynamic Reconfiguration of the system produces enormous advantage in implementing a process.

QRS DETECTION AND SHAPING CIRCUIT

To detect QRS complex 17 Hz band pass filter with Q of 3.3 and shape the R peak into a square pulse of 200ms width by other circuitry is used. Multiple-feedback band pass filter configuration is used to design filter. As QRS complex positive part is important for shaping QRS complex the half wave rectifier is used to provide positive output by compare with threshold level which is set by an automatic threshold circuit. In presence of artifacts and noise interference also the variable threshold levels are set for variety of QRS complex morphologies to provide reliable R wave triggering. The criteria for threshold variation are as follows:

a) The baseline interference and P waves are the source of increasing the minimum threshold level than filter output.
b) The filter output is stored in sample and hold circuit with 10sec delay from previous R wave and most of the delayed signal is added to the minimum threshold. It leads the circuit to function as fast automatic gain control and it is deciding the previous QRS complex size.
c) 200ms refractory period is generated by mono stable circuit, which leads the circuit to trigger from ringing output of filter as well as on T waves incorrectly. The stored filter output is reset by mono stable circuit by every 50ms and it allows quick recovery from saturation and direct towards failure.

Table-1. Arrhythmia detection algorithms.

Arrhythmia	Evaluation
Bradycardia	RRt > 1.5 sec; ARt > 1.2 sec
Tachycardia	ARt < 0.5 sec
Asystole	No R wave for more than 1.6 s
ventricular fibrillation	No R wave for more than 1.6 s
Skipped beat	RRt < (1.9) * (ARt-1);
Premature ventricular contraction	RRt-1 < (0.9) * (Art-2); RRt-1 + RRt = 2*Art-2
R-ON-T	RRt-1 < 0.33(ARt-2); RRt-1 + RRt = 2*Art-2
BIGEMINY	RRt-3< 0.9(ARt_4); RRt-1 < 0.9 * Art-4 RRt-3+ RRt-2= 2 * (Art-4); RRt-1 + RRt = 2 * (Art-4)
Trigeminy	RRt-2< 0.9 * (Art-3); RRt-1 < 0.9 * (Art-3) RRt-2+ RRt-1 + RRt = 2 * (Art-3)
Interpolated PVC	RRt-1 < (0.9) * (ARt-2); RRt-1 + RRt = ARt-2
APB	RRt-1 < 0.9 * (ARt-2); ARt-1< RRt-1 + RRt< 2 * ARt-2; Rate > 10/min

RRt is recent R-R intervals, RRt-X is previous R-R intervals, ARt is average of 8 successive RR intervals and Art-X is average of 8 successive RR intervals

This work proposes the FPGA implementation of the algorithm for detection of cardiac arrhythmia's consuming less power. The detection of QRS complex by means of band pass filter and shaping the R peak into a

square pulse of 200ms width by other circuitry is utilized. The time interval between R peaks and the average of 8 recent RR intervals are measured for detecting various arrhythmias. A total of 11 arrhythmias are considered for identification.

SYSTEM DESIGN

Each R peak is shaped into a pulse of 200ms width including refractory period. The time interval between the falling edge of R peak and rising edge of next R peak is measured by using a 12 bit counter with a resolution of 1ms. During the rising edge of R peak, the counter output is latched and the standard pulse width of 200ms is added to calculate the RR interval. Similarly other 8 RR intervals also calculated and are labeled as RR_{t-1}, RR_{t-2}, RR_{t-3}, RR_{t-4}, RR_{t-5}, RR_{t-6}, RR_{t-7} and RR_{t-8}. The average of 8 RR intervals AR is calculated and other averages are labeled as AR_{t-1}, AR_{t-2}, AR_{t-3} and AR_{t-4}. The system block diagram is given in Figure-1.

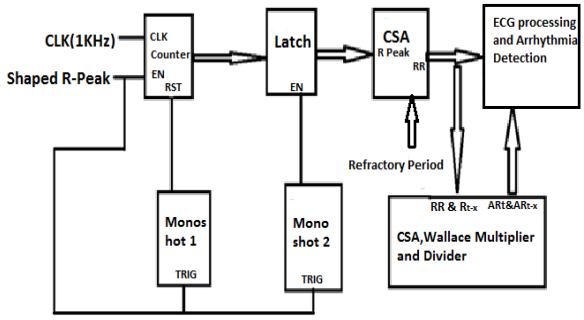

Figure-1. Block diagram of ECG processing for arrhythmia detection.

SYNCHRONOUS UP COUNTER AND MONO SHOT CIRCUIT

The output of monoshot1 is used to reset the counter and monoshot2 is used to enable the latch. The monoshot1 is designed by using shift registers and gate circuit as shown in Figure-2. The shaped ECG signal is given as input to SR1 and is shifted by 1 KHz clock. The output of SR1 is again shifted by SR2 with the same clock. Both the SR outputs are passed through gate circuitry to generate a pulse to reset the counter. Again the shaped ECG signal is given as input to SR and is shifted by 1 KHz clock. The monoshot2 is designed by using shift registers and gate circuit as shown in Fig3. The output of SR and shaped ECG signal are passed through gate circuitry to generate a pulse for latch enable. The latched output represents the time between two R peaks. This time interval is added with 200msrefractory period using Carry Select Adder (CSA) to calculate RR intervals. The wave forms of mono shot circuits of normal and abnormal ECG signal are shown in Figure 4 and 5.

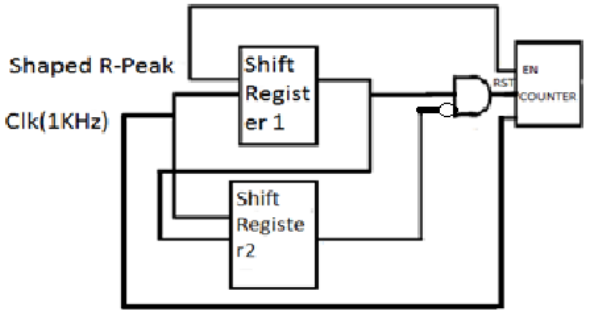

Figure-2. Monoshot1circuit for counter reset.

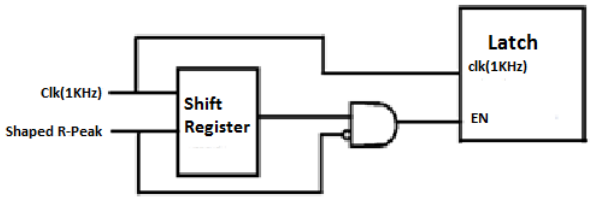

Figure-3. Monoshot2 circuit for latch enable.

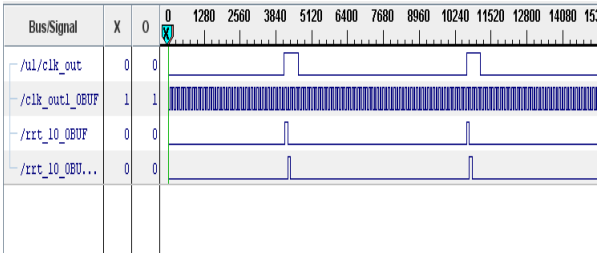

Figure-4. Counter reset and latch enable with shaped normal ECG signal.

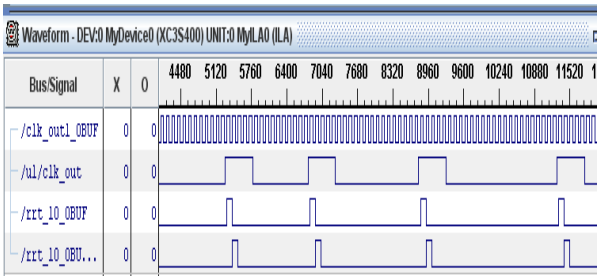

Figure-5. Counter reset and latch enable with shaped abnormal ECG signal.

RR INTERVAL CALCULATION USING MODIFIED CARRY SELECT ADDER WITH CBL

The RR intervals are calculated by adding 200msrefractory period to R peak intervals of latch output using CSA adder. The CSA is designed by using Common Boolean Logic (CBL) term. In the truth table of single bit full adder, the sum of adder with logic 0 carry in is

complement of the sum with logic 1 carry in which are marked by circle in Table-2. By using this logic, the adder is designed by a XOR gate and INV gate to generate the summation pair and an OR gate and AND gate to generate the carry pair and adder design is shown in Figure-6. The switching activity of system is reduced due to less number of gate utilization by using Boolean logic.

Table-2. Truth table of full adder.

C_{in}	A	B	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

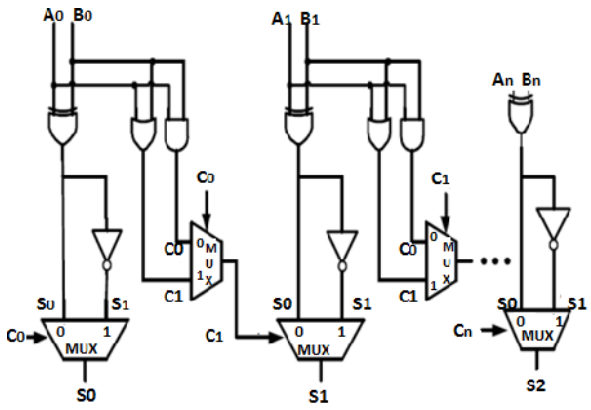

Figure-6. CSA with Common Boolean Logic.

ECG PROCESSING AND ARRHYTHMIA DETECTION

All the parameters RR_t, RR_{t-1} RR_{t-2}, RR_{t-3}, AR_t, AR_{t-1}, AR_{t-2}, AR_{t-3} and AR_{t-4} are observed by using above design. The multiplier and divider is required to calculate other parameters like $2*AR_{t-2}$, $0.9* AR_{t-2}$ etc. Multiplier consumes high amount of power and produces delay during the partial products addition. Most of the multipliers are designed with different kind of multi operands adders that are capable to add more than two input operands and results in two outputs, sum and carry. The number of adders is minimized by Wallace Tree. Compressors are used in multiplier architecture. Multipliers are usually structured into three functions: partial-product generation, partial-product accumulation and final addition. The main source of power, delay and area is the partial-product accumulation stage. Compressors reduces the number of adders required at the final stage and thus reduces power consumption. Also it contributes to reduce the critical path and maintains the performance of the circuit.

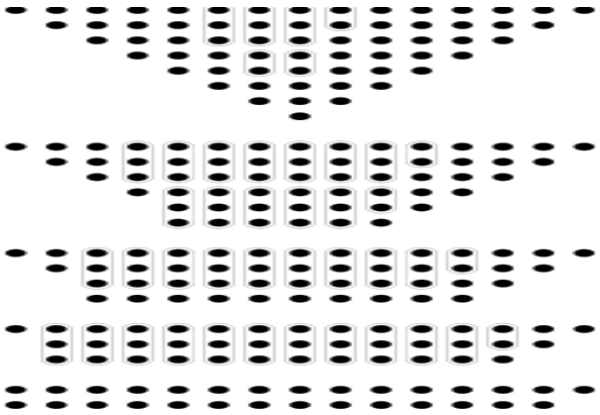

Figure-7. Modified Wallace tree multiplier with pyramid structure.

The Wallace tree construction method is usually used to add the partial products in a tree-like fashion in order to produce two rows of partial products that can be added in the last stage. The pyramid structure of Wallace filter is shown in Figure-7. The Wallace tree is fast since the critical path delay is proportional to the logarithm of the number of bits in the multiplier. The prominent method is considering all the bits in each column at a time and compresses them into two bits (a sum and a carry). 4:2 compressors, 3:2 compressors and 5:3 compressors are used for compression. The architecture of Wallace tree using CBL based CSA is shown in Figure-8.

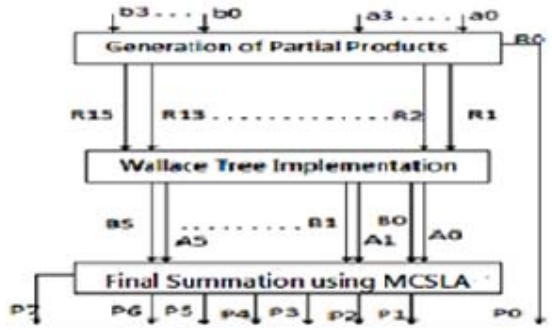

Figure-8. Wallace tree architecture using CBL based CSA.

RESULTS

11 arrhythmias are considered for processing as mentioned in Table-1. The shaped QRS complex into a square pulse of 200ms is made available. The design is implemented on Spartan3 FPGA and the algorithm is written by using Verilog HDL language. Low power is achieved by using low power adder (CSA) and multiplier

(Wallace multiplier). XILINX ISE13.1 is used for simulation and functional verification. The on chip functionality is verified by chip scope analyzer. The result of on chip verification is shown in Figures 4 and 5. The simulation result of different arrhythmias are shown in Figures 9, 10, 11 and 12. The dynamic power consumption is calculated on Xilinx and was measured as 22mW and power analysis report is shown in Figure-13.

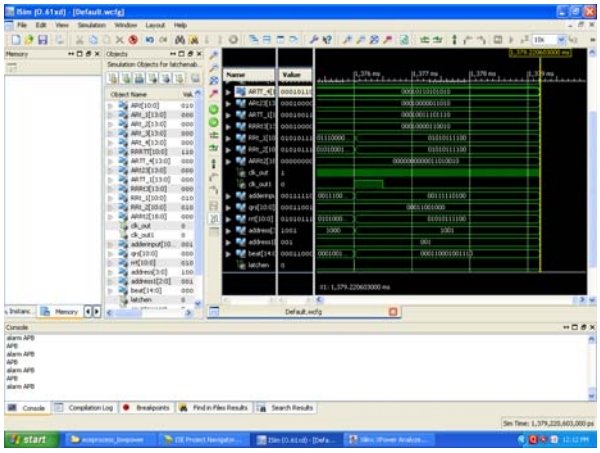

Figure-9. Simulation result of arrhythmia APB.

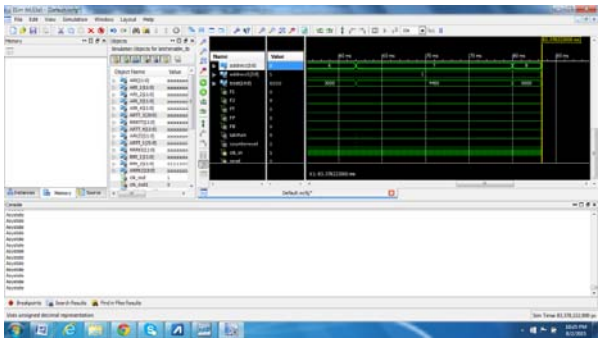

Figure-10. Simulation result of arrhythmia Asystole.

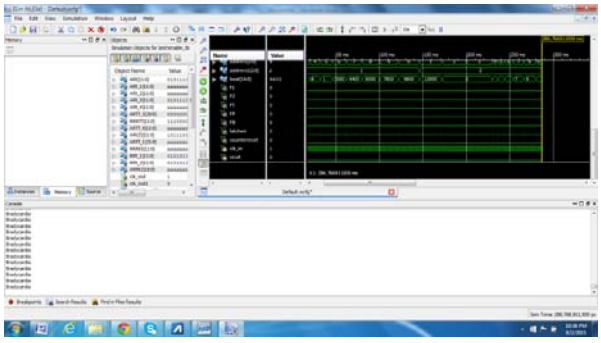

Figure-11. Simulation result of arrhythmia Bradycardia.

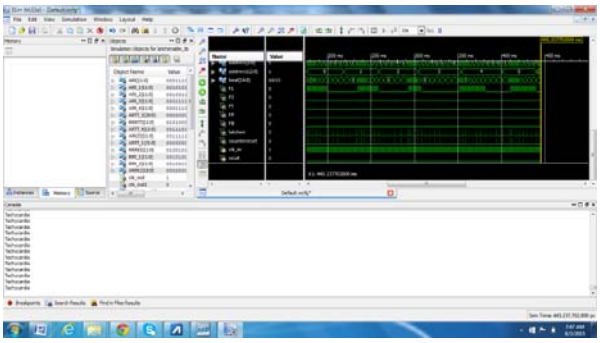

Figure-12. Simulation result of arrhythmia Tachycardia.

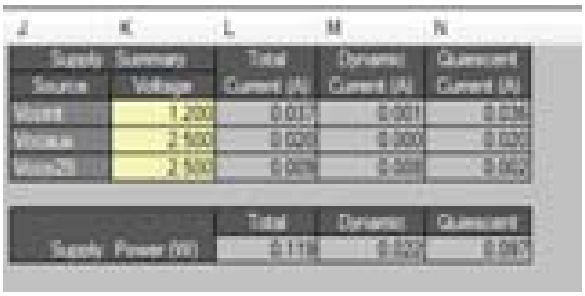

Figure-13. Power report of arrhythmia detection algorithm.

CONCLUSIONS

A new approach for implementing an arrhythmia detection algorithm by analyzing ECG signal is designed and simulated in Xilinx13.1 ISE platform. The low power design is used for developing this algorithm. The proposed method overcomes the disadvantages of many existing methods by utilizing low power and this system can assist physicians in cardiac disease identification and also for long term monitoring with low power consumption.

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