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A LOW POWER, LOW NOISE AMPLIFIER FOR RECORDING NEURAL SIGNALS

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ABSTRACT

The design of a low power amplifier for recording EEG signals is presented. The low noise design techniques are used in this design to achieve low input referred noise that is near the theoretical limit of any amplifier using a differential pair as input stage. To record the neural spikes or local field potentials (LFP's) the amplifier's bandwidth can be adjusted. In order to reject common-mode and power supply noise differential input pair need to be included in the design. The amplifier achieved a gain of 53.7dB with a band width of 0.5Hz to 1.1 kHz and input referred noise measured as 357 nV_{rms} operated with a supply voltage of 1.0V. The total power consumed is around 3.19μW. When configured to record neural signals the gain measured is 54.3 dB for a bandwidth of 100 Hz and the input referred noise is 1.04μ V_{rms}. The amplifier was implemented in 180nm technology and simulated using Cadence Virtuoso.

Keywords: amplifier, neural signals.

INTRODUCTION

To understand the working of brain large scale multi electrode systems were built for recording neural signals [1], [2]. Such systems helped in conducting various experiments and proved that prediction of limb movements by recording neural signals from multiple sites simultaneously and analyzing [3], [4]. As an example a paralyzed person can move wheel chair or a computer cursor using thoughts and to perform such tasks brain machine interfaces are built. These interfaces not only help in monitoring brain activities but also help immovable and physically handicapped people.

A neural signal amplifier is the most important part in the brain machine interface. The signals recorded from the external part of the brain are very weak typically between 10 to few hundred μV. in order to process these signals amplification is needed. Future requirements may demand for implantable recording system requiring large number of neural amplifiers (i.e. one for each electrode). An ultralow power operation is very important for these applications to achieve longer battery life, reduce heat dissipation.

The input referred noise of the amplifier should be low for recording clear neural signal and should be kept below the background noise of the recording site [2]. The differences between the low noise and low power designs must be properly addressed by the designers. The power of a thermal noise limited amplifier having constant bandwidth and supply voltage scales as $1/v_n^2$ where v_n is the input referred noise. Hence, to achieve low noise performance the cost of power steeply increases. Several amplifier designs for recording neural signals were reported in the literature [5]-[9] and most of them for a bandwidth of 5-10kHz and for an input referred noise of about 5μV consumed power of around 100μW. The amplifier design described in [8] achieved 2.2μV of input

referred noise and consumed 80μW of power and the band width obtained was 7.2kHz.

The power consumption of a neural amplifier will become a limiting factor in a multi electrode array neural recording system if such amplifiers consuming power approximately 100μW per amplifier are to be used. In order to avoid this bottleneck a new micro power amplifier design is proposed. This design keeps the power of the amplifier low enough so as to reduce the total power consumption of the multi electrode recording system. Various neural amplifier design techniques are proposed in [8].

To reject large dc offsets present at electrode interface and enabling the amplifier to allow the signals of interest a MOS bipolar pseudo resistor having high resistance value [10] along with dc coupling capacitors on chip can be used. Several off chip components are not needed as high resistance components can be realized in a small area on chip. The design proposed in [8] is standard operational trans-conductance amplifier (OTA) having wide output swing. Capacitive feedback is employed and achieved a gain of nearly 40dB. Various design techniques are proposed to reduce the input referred noise by operating some devices in strong inversion to reduce their noise contributions. However the design obtains tradeoff between power-noise nearer to the theoretical limit, the OTA topology is not power efficient, because most of the current is wasted in current mirror circuits. In a single ended open loop amplifier a common source input stage with resistive load can achieve very low noise if the gain of this stage is greater than 5 for fixed power and bandwidth. However differential pairs are used in neural amplifiers for high rejection of common mode and power supply noise sources.

A conventional differential pair is used in the design for rejection of common mode and power supply



Then MOS current sources are made with large area they produce large $1/f$ noise. In this neural amplifier the $1/f$ noise is from the differential pair and hence in this design to achieve low $1/f$ noise the differential pair is made with large area PMOS transistors.

Device sizing for maximizing G_m

By maximizing the trans conductance of the OTA for a given current, low input referred noise can be achieved. In a standard folded cascoded OTA the maximum trans conductance is equal to that of the trans conductance of one of the transistor in the input differential pair. Hence the transistors M1 and M2 are operated in sub threshold region where g_m is maximum for a given current. The aspect ratio of M1 and M2 need to be large and this requires lengths of M1 and M2 need to be small so as to keep their widths relatively small and the input capacitance of the OTA is not large.

The input differential pair transistors are cascoded with M3 and M4 to increase their output impedances and also to ensure the incremental current goes through the sources of M7 and M8. The transistor-resistor combinations of M5 and M6 forms the source degenerated current sources are designed to have large output impedances. To keep G_m near to g_{m1} , the impedance looking into the sources of M7 and M8 must be much smaller than the impedances of the cascoded differential pair and the source degenerated current source.

Table-1.

Operating Points for Transistors in the Ota with $I_d = 3.19\mu$ a devices and current scaling ratio.

Devices	Current division ratio's
$M_{b1}:M_{b2}$	7:1 ($2I_B/14$)
$M_{1}:M_{2}, M_{3}:M_{4}$	$7I_B/14$
$M_{5}:M_{6}$	$8I_B/14$
$M_{7}:M_{8}, M_{9}:M_{10}, M_{11}:M_{12}$	$I_B/14$

Device s	W(um)/ L(nm)	I_b	Operating region
$M_{1,2}$	7/180	1.26uA	Sub-threshold region
$M_{3,4}$	45/180	1.26uA	Sub-threshold region
$M_{5,6}$	8/180	1.44uA	Sub-threshold region
$M_{7,8}$	2/180	180nA	Sub-threshold region
$M_{9,10}$	2/180	180nA	Sub-threshold region
$M_{11,12}$	2/180	180nA	Sub-threshold region

MEASUREMENT RESULTS

The amplifier schematic given in Figure-4 is similar to that given in [8]. The MOS bipolar pseudo resistor component formed by $M_a - M_b$ and the capacitance C decides the low frequency high pass cutoff of the gain stage. The amplifier mid band gain so obtained is around 54 dB. The amplifier can record either LFP (Local Field Potentials) having frequencies 1-100 Hz or neural spikes of frequencies 100 Hz-1KHz.

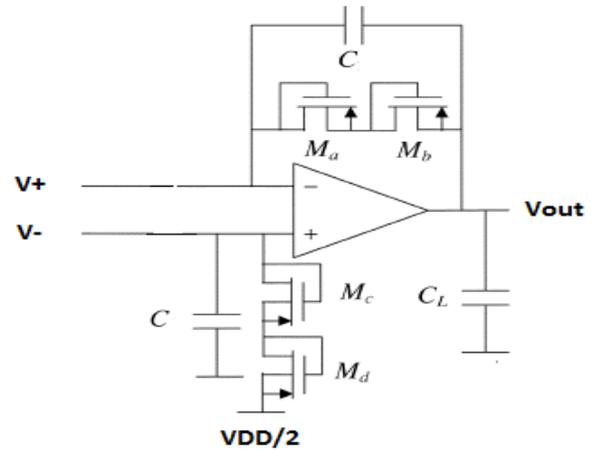


Figure-4. Neural amplifier schematic.

For recording LFP whose band width is low, the bias current in the gain stage can be reduced to lower the power and the cutoff frequency of the high pass must be kept as low as possible. To create high pass filter a weak inversion MOS transistor is placed in parallel with C with few hundred Hz as cutoff frequency [7]. The input transistors noise currents at gates are low pass filtered by C and MOS bipolar pseudo resistor and introduces low frequency noise that rolls off as $1/f^2$. This noise also gets amplified which degrades the detectable signal. The impedance of MOS bipolar pseudo resistor is higher than a weak inversion MOS transistor hence the filter pole created by the Pseudo resistor element will be at a very low frequency [7]. The noise current introduced with this element and the shot noise due to leakage current at the gates are filtered before the pass band and will not appear in the frequency band of interest.

The amplifier was implemented in 180nm CMOS process and is simulated using Cadence Virtuoso. All the capacitors were implemented poly-poly capacitors. The amplifier is designed to give a gain of 50dB and operate at a supply voltage of $\pm 1V$. The total current consumed is $3.19\mu A$. The -3dB cutoff frequencies are adjusted as 0.5Hz and 1.1 kHz. The plot of the measured gain and phase response is given in Figures 5 and 6 below.

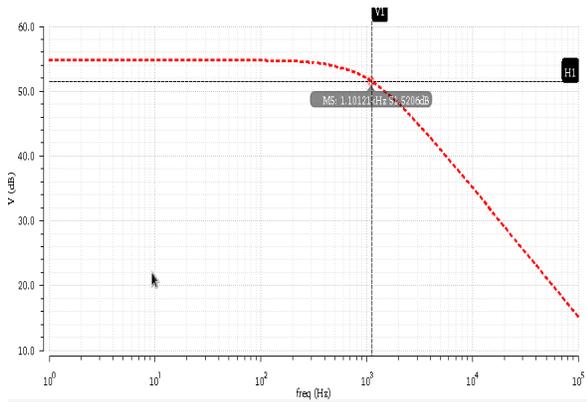


Figure-5. Gain plot of OTA.

Table-2.

Parameter	Measured
Supply Voltage	$\pm 1V$
Total Current	3.19uA
Gain	53.7 dB
Bandwidth	0.5Hz-1.1 KHz
Input referred Noise	357 n V _{rms}
CMRR	78.7 dB
PSRR	95.7 dB
Power Dissipation	3.19 μ W

The measured parameters are given below in Table-2:

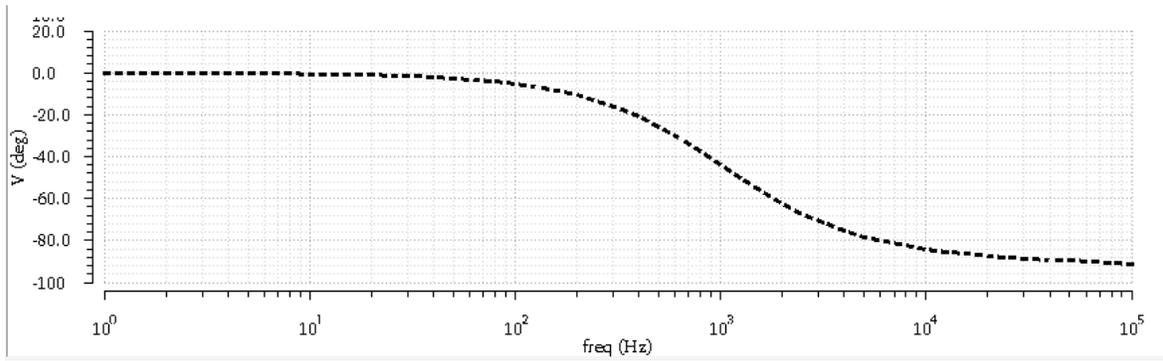


Figure-6. Phase response of OTA for BW of 1kHz.

In some of the brain machine interfaces Local field potentials are often recorded instead of action potentials. The performance characteristics of this amplifier are measured by configuring with lower bandwidth. The energy of LFP lies in the frequency range

of 1-100Hz, the 3dB low pass and high pass cutoff frequencies are lowered by reducing the supply current of the OTA. The OTA is adjusted to have a band width of 0.5 Hz to 100Hz for LFP recording. The Magnitude of gain and phase response measured is given in Figure-7.

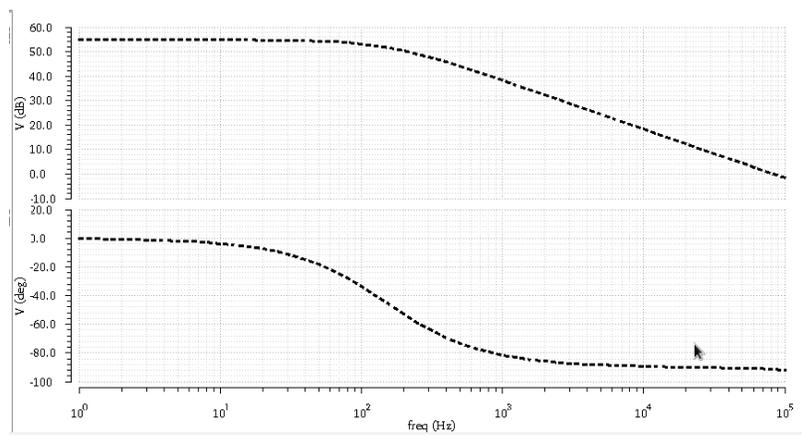


Figure-7. Magnitude and phase response of OTA for BW of 0.5-100Hz.



The measured parameters of the OTA for the bandwidth of 0.5-100Hz are given in below in Table-3.

Table-3.

Parameter	Measured
Supply Voltage	1V
Total Current	3.19uA
Gain	54.3 dB
Bandwidth	0.5Hz-100Hz
Input referred Noise	1.04u V _{rms}
CMRR	79.3dB
PSRR	96.3dB
Power Dissipation	3.19uW

CONCLUSIONS

A low noise low micro power amplifier to record neural signals is presented. To keep the input referred noise of the amplifier near to the theoretical limit of the input differential pair low noise design techniques were employed. As per the measurements it appears that the amplifier had lowest power and energy efficient. Either action potentials or Local field potentials can be recorded by suitably configuring the amplifier's band width. This can be used in many almost all the systems used for recording and processing brain signals.

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