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ENERGY EFFICIENT DESIGN OF LASER DRIVER USING FIELD PROGRAMMING GATE ARRAY

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ABSTRACT

The laser drivers are extremely important to be used to provide safe interface for the optical components attached to the laser. In this paper, energy efficient laser driver circuit is design using field programming gate array (FPGA). The laser driver is first designed using current mode logic (CML) technique, which is widely used for designing the optical components. Then this design is implemented on FPGA using very large scale integration (VLSI). The laser driver produces the energy efficient output using voltage scaling technique in which the core voltage of FPGA virtex-7 board is reduced from 2.2 V (Peak core voltage of FPGA) to 0.5 V (base voltage of FPGA). By reducing core voltage of FPGA virtex-7 from peak to base voltage the power consume by laser drivers is reduced up to 90% for 15 THz frequency. Similarly, for less than 15 THz frequencies the power consumption is also reduced. The main advantage of designing this energy efficient laser driver is that it will control the output of any high frequency semiconductor laser up to 15 THz frequency. This energy efficient design of laser driver will be integrated with high frequency semiconductor laser to produce green optical output for communication systems.

Keywords: current mode logic, core voltage of FPGA, voltage scaling technique, laser driver, power reduction, field programming gate array.

INTRODUCTION

It is quite precarious, when laser is directly interfaced with the optical system ahead. When input operating frequency of laser is increase above 1 GHz, the power consumption is increased drastically. At 20 THz, the power consumption is increased up to 98%. This increase in power may destroy the attached device forever (Belfiore, Szilagyi, Henker, and Ellinger, 2015)].

Laser driver works as interface between laser and additional devices attached to laser. Laser output is very sensitive at high frequency the power of device is increasing drastically and this must be controlled to protect other devices connected to laser using laser driver (Capellini, Wenger, Schroder, and Kozlowski, 2015). When laser frequency is exceeded the power and current of the laser also increased. This increased power may cause the permanent disability to the additional components attached to the laser(Camilotti *et al*., 2015). Laser driver provides the switching for laser to shield the additional devices attached to laser. The efficient designing of the laser driver only provides the switching when laser output is out bound from ranges. Energy efficient design of laser driver means with the switching it must save the power when laser crosses outbound operating ranges(Eimerl et al., 2014). There are various techniques are available to control the output of power of laser driver such as manually change the input voltage source of laser, provides the bias circuit between laser and additional components and etc. but none of them has potential to provide energy efficient output (Kostamovaara *et al*., 2015). This is because the laser driver circuit is not saving the power and each time replacing the physical components to produce the laser output is also costly and time wasting and this process is not advisable practically(K. Liu *et al*., 2014).

In this work above, mentioned problems are encountered. This research provides the high frequency switching between laser and additional devices and consume less power when operating at high frequency. Furthermore, the designed is realized using the System on Chip (SoC) configuration on FPGA to avoid the components replacement and saves times to produce the different laser output(Lim, Kong, Kwon, and Lim, 2014). The high frequency switching of 15 THz and between laser and additional components is achieved. Additionally, power consumption is reduced for different high operating frequency of laser(Cundiff, Wahlstrand, Zhang, and Choi, 2014). The current stability and high frequency switching is performed by designing the laser driver circuit for high frequency laser using current mode logic technique. After incorporating the CML based laser driver circuit in FPGA using VLSI, the power consumption is reduced by applying the voltage scaling technique. In FPGA, voltage scaling is performed by changing the core voltage of FPGA viretx-7(Kastensmidt *et al*., 2014). The complete energy efficient design of laser driver is experimentally demonstrated using FPGA Virtex-7.

LITERATURE REVIEW

Laser are widely used optical sources due to its exceptional size, spectral region of procedure and high efficiency (Gu *et al*., 2015) to transmit data over optical fiber. Currently, high frequency operation at low power consumption is in demand (Xu, Gu, Wu, and Chang,

2015). However, when the laser output is uncontrollable it causes interruption for the transmission systems so direct interface of laser with system is not be use. For this purpose the laser driver are to used that works as a switch that reacts over an input signal modulated by the data pulses (Smith, Mozzanica, and Schmitt, 2015). There are several techniques are available to design the laser drivers such as source coupled logic, differential digital logic, Diode–transistor logic (DTL), Diode-transistor logic (DTL), Direct-coupled transistor logic (DCTL), Emitter-coupled logic (ECL), Gunning transceiver logic (GTL), Integrated injection logic (I2L), NMOS logic and etc (Soni and Naiyar, 2014). Among these NMOS logic is widely used for optical components design. Current mode logic technique exist due to NMOS logic (Ng, Choi, and Wang, 2014). These laser drivers are utilized in LAN, MAN and Fiber take to home (Latal *et al*., 2015). The hardware realization of laser driver is complicated and requires circuit redesign many times until meet the requirement. Nevertheless, FPGA provides the system on chip facility using VLSI design to design any component in real time without circuit redesign in terms of components, in this way the hardware cost of redesigning and costly is efficient saved (Zhang, Scherjon, and Burghartz, 2015). Furthermore, the VLSI design of components provides many features such to perform power optimization, voltage control, frequency control and many physical parameters can easily be controlled (Zhang *et al*., 2015).

In this work, semiconductor laser's (edge emitting laser) output is controlled using current mode logic the reason why this technique is chosen from above mentioned techniques is that it provides fast switching at high frequency and this technique gives the possibility to design optical components. Furthermore, FPGA based realization is demonstrated CML based due to the advantages of FPGA discussed above.

Current mode logic technique

NMOS logic style used in the design of digital integrated circuits due to its benefits such as very low static-power dissipation, high packing density that provides high frequency operation(Gaur and Budakoti, 2014) (Raghav, Maheshwari, and Gupta, 2014). A current mode logic (CML) is constructed using differential architecture. The differential circuit is easily neutralized using a pair of capacitors that will diminish the deleterious effects of input-output coupling through the device overlap capacitance, CGD. The reason of using CML is because a CML circuit is a low-voltage circuit where the differential voltage swing is around the device threshold voltage. Figure-1 describes the schematic diagram of NMOS logic (Zimmermann and Fichtner, 1997) (Razavi, 2015) (Bulzacchelli and Kim, 2015).

Laser driver is designed using current mode logic because its transmission is point-to-point and is usually terminated at the destination on both differential line; large current is regulated by eliminating unwanted common mode noisy signals (Chang, 2008). If signals are symmetrical during propagation can reduced cross talk, their symmetrical behavior improves the wide band transmission. Current mode logic also provides differential circuit operation with low voltage swing, suitable for high speed, robust performance and better noise immunity, constant current drawn from the power source, does not generate significant switching noise (Chang, 2008). There is limitation of current mode logic that is static power dissipation it mean when the laser is not in active mode still the some power dissipates but this is very small and negligible (Jankowski and Napieralski, 2014) (S. Liu, Li, and Wilson, 2015) when dealing with GHz frequency but it may causes other saturation problem if it is not deal separately.

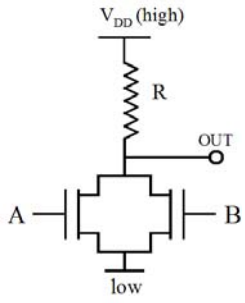

Figure-1. Schematic diagram of NMOS logic.

Voltage scaling technique

Voltage scaling (VS) technique is used to reduce the power consumption of circuit, by varying the voltage of the circuit (Kumar, 2015; Pal, 2015). For best results, the circuit should operate at the voltage that reduces power consumption as much as possible, while maintaining reliable operation. Finding this threshold is difficult, however, since the optimum operating voltage is required to save the power. There are different types of voltages are prerequisite for typical power supply requirement for semiconductor laser driver and its operation using FPGA (Y. Li, Chuang, Kennings, and Sachdev, 2015). The different voltages used in FPGA includes core supply voltage (VCCINT), auxiliary voltage (VCCAUX), output driver supply voltage (VCCO), reference voltage for IO standards (VREF) and others (F. Li, Lin, and He, 2007). Power consume by laser drier is directly proportional to the square of the voltage applied to the circuit, as shown in equation(1), where C is the gate load capacitance (output capacitance), VDD is the supply voltage and f is the clock frequency (Dickson, 1976). In this work, the core voltage of FPGA is varied from peak voltage to base voltage to reduce the power consumption for laser driver at high frequency operation.

$$P_{NMOS} = CV_{core}^{2} * f \quad (1)$$

Method for design the energy efficient laser driver using FPGA

Laser driver design using current mode logic

In this work, using NMOS logic the laser driver circuit is designed for high frequency laser. In which two parallel network are created. One network provides the source and other network creates the threshold for the laser(K. Li, Thomson, Wilson, and Reed, 2015). After this, laser output is compared with threshold output. If the laser output is greater than threshold the circuit reaches in cut-off region and if the laser output is less than threshold the circuit reaches in saturation and in between, the circuit operates in active region. The CML based design of laser driver produces the stability of generating 1.2 mA to 6.1 mA up to the maximum frequency of 15 THz. Laser driver is designed to modulate a laser output with serial data pulses and provides DC bias (reference) current to the laser. Figure-2 articulates, the CML based design of laser driver in Matlab. The current produced by laser driver is shown using equation (2);

$$\Delta I_D = I_{GS} - I_{DD} = \frac{1}{2}\mu_n \Delta I_{SOURCE} \sqrt{\frac{4I_{SOURCE}}{\mu_n}} - \sqrt{\Delta I_{SOURCE}^{\ 2}} \quad (2)$$

ΔID in equation (2), is the laser driver current, which controls the current of semiconductor laser. This laser driver provides the safe interfacing of laser with other optical components. The laser driver produces the continuous laser light at frequency of 10 GHz as an input DC source driven by CML.

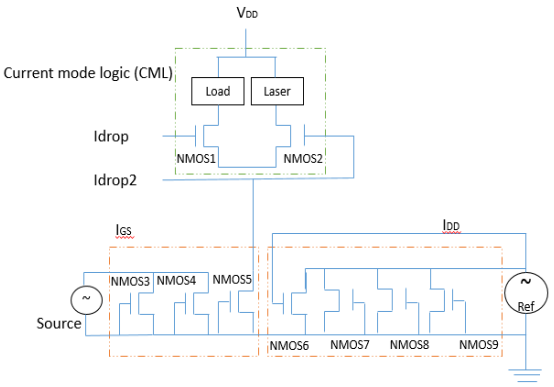

Figure-2. Semiconductor laser driver circuit using current mode logic in Matlab.

Energy efficient design of CML based laser driver using FPGA

After designing the laser driver using current mode logic technique, the design is simulated using Hardware descriptive language (HDL) for VLSI design. The voltage scaling is applied over VLSI design of laser driver to make laser driver energy efficient. Finally, this VLSI based design of laser driver is transferred to FPGA vertex-7 board to demonstrate the energy efficient design of laser driver. Figure-3 describes the RTL schematic diagram of laser driver in Xilinx 14.3 suite.

The parameters used for FPGA based realization of laser driver includes the device model XC6VCX75T, programming method VHDL, ambient temperature of 32ºC. FPGA vertex-7 is used in this experiment because high-density fabrication, digital signal processing, default IO standard facility that support high bandwidth up to 70 GHz(Pandey, Karmakar, Shekhar, and Gurunarayanan, 2015). Using voltage scaling technique when laser driver is operated at frequency ranges from 12 GHz to 15 THz, the power reduction is recorded.

Voltage scaling of laser driver

Laser driver is operated at 12 GHz, 150 GHz, 900 GHz and 15 THz at different core voltage of FPGA vary from 2.2 V to 0.5 V. The power consumption is recorded for all frequency ranges over each core voltage. Here the five different values are taken for voltage scaling these are 2.2 V, 1.8 V, 1.4 V, 0.9 V and 0.5 respectively. The total power consumption includes clock power, logic power, signal power, IO power and leakage power in terms of Watt [W]. The total power is also called the dynamic power.

Power consumption of laser driver at core voltage of 2.2 V

Table-1 shows, the values for the power consumption of laser driver. The values are recorded for different operating frequencies of 12 GHz, 150 GHz, 900 GHz and 15 THz at core voltage of 2.2 V. The power consumption consist of clock, logic, leakage and other powers. Similarly, the power consumption will be recorded for same frequencies but ad different core voltages and finally, the power values are compared to check the effect of decreasing the core voltage of laser driver.

Table-1. Power consumption in W at 2.2 V FPGA core voltage.

Frequency→ Power↓	12 GHz	150 GHz	900 GHz	15 THz
Clock	0.099	0.846	5.433	49.90
Logic	0.005	0.02	0.06	0.67
Signal	0.006	0.04	0.589	2.9
IO	0.098	0.98	2.989	19.255
Leakage	2.778	2.954	3.021	3.199
Total	2.986	4.84	12.092	75.926

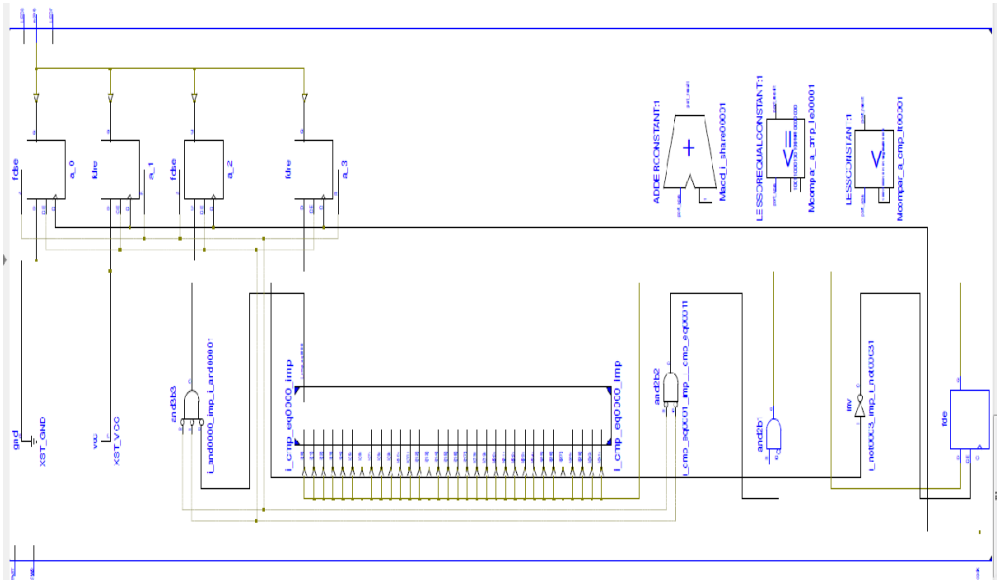

Figure-3. RTL schematic diagram of laser driver.

Power consumption of laser driver at core voltage of 1.8 V

When core voltage is changed from 2.2 V to 1.8 V, the power consumption is recorded for different frequency 12 GHz, 150 GHz, 900 GHz and 15 THz as shown in Table-2. It is observed that when core voltage is changed reduction in power consumption is recorded for different frequency. For 12 GHz, 150 GHz, 90 GHz and 15 THz 30 %, 33%, 24% and 44% power reduction is recorded in comparison with power values of at core voltage of 2.2 V respectively. It is analyzed that by varying core voltage of FPGA the power reduction can be achieved even for high frequency values.

Table-2. Power consumption in W at 1.8 V FPGA core voltage.

Frequency→ Power↓	12 GHz	150 GHz	900 GHz	15 THz
Clock	0.076	0.729	4.427	23.001
Logic	0.004	0.013	0.038	0.361
Signal	0.004	0.027	0.487	1.798
IO	0.078	0.498	2.197	15.301
Leakage	1.924	1.954	1.978	1.91
Total	2.086	3.221	9.127	42.371

Power consumption of laser driver at core voltage of 1.4 V

When laser driver is operated at different frequency for reduced core voltage of 1.4 V. The power reduction is noted that for 12 GHz 62%, for 150 GHz 62%, for 900 GHz 45% and for 15 THz 62% power reduction is achieved on contrary to power consumption at core voltage of 2.2 as shown in Table-3.

Table-3. Power consumption in W at 1.4 V FPGA core voltage.

Frequency→ Power↓	12 GHz	150 GHz	900 GHz	15 THz
Clock	0.061	0.634	3.781	13.352
Logic	0.002	0.006	0.022	0.221
Signal	0.002	0.014	0.345	1.003
IO	0.059	0.19	1.421	12.811
Leakage	1.008	0.98	0.974	1.099
Total	1.132	1.824	6.543	28.486

Power consumption of laser driver at core voltage of 0.9 V

Table-4 shows the laser driver operating at different frequency at core voltage of 0.9 produces the power reduction in comparison with the power consumption at 1.4 V. It is observed that for 12 GHz, 150 GHz, 900 GHz and 15 THz the 69%, 70%, 58% and 86% power reduction is achieved respectively.

Table-4. Power consumption in W at 0.9 V FPGA core voltage.

Frequency→ Power↓	12 GHz	150 GHz	900 GHz	15 THz
Clock	0.049	0.541	3.243	3.81
Logic	0.001	0.004	0.013	0.167

Signal	0.001	0.009	0.178	0.43
IO	0.049	0.09	0.801	5.08
Leakage	0.801	0.795	0.775	1.005
Total	0.901	1.439	5.01	10.492

Power consumption of laser driver at core voltage of 0.5 V

When laser driver is demonstrated at core voltage of 0.5 V that is the base voltage of FPGA. In comparison with the power values at core voltage of 2.2 V or peak voltage of FPGA for 12 GHz, 150 GHz, 900 GHz and 15 THz, 71%, 82%, 68% and 90% power reduction is achieved as mentioned in Table-5. With the help of core voltage of power consumption of laser driver is reduced.

Table-5. Power consumption in W at 0.5 V FPGA core voltage.

Frequency→ Power↓	12 GHz	150 GHz	900 GHz	15 THz
Clock	0.21	0.341	2.443	2.81
Logic	0.001	0.002	0.007	0.102
Signal	0.001	0.005	0.100	0.203
IO	0.029	0.07	0.644	3.08
Leakage	0.601	0.405	0.575	0.905
Total	0.842	0.832	3.769	7.100

RESULTS AND DISCUSSIONS

Energy efficient design of laser driver is achieved using the current mode logic and FPGA based voltage scaling. The laser driver is operated at 12 GHz, 150 GHz, 900 Hz and 15 THz frequencies, at different core voltages of 2.2 V, 1.8 V, 1.4 V, 0.9 V and 0.5 V.

The results in Figure-4 states that clock power is reduced for 12 GHz 50%, 150 GHz 36%, 900 GHz 40% and 15 THz 92% in comparison with clock power of peak and base core voltages of FPGA. Figure-5 describes the power reduction in logic power by comparing the power values at peak core voltage and base core voltage 80%, 78%, 75% and 75% for 12 GHz, 150 GHz, 900 GHz and 15 THz respectively. Signal power, IO power and leakage power are also reduced for power values of different frequencies over 2.2 V core voltage and 0.5 core voltage. Signal power is reduced 83%, 77%, 69% and 85%, IO power is reduced 50%, 90%, 73% and 73% and leakage power is also downed 71%, 73%, 74% and 68% for all respective frequencies as shown in Figure-6, Figure-7 and in Figure-8 respectively. Overall, when laser driver is operated at peak core voltage and base voltage significant power reduction is achieved on contrary to both voltages. For 12 GHz, 150 GHz, 900 GHz and 15 THz, 71%, 82%, 68%, and 90% power reduction is achieved by comparing the both core voltages as shown in Figure-9.

Laser driver itself operates in the range of 2.5 to 0.3 V. When core voltage FPGA is varied from 2.2 V to 0.5 V it is actually falls in the range of laser driver operating voltage. Additionally, the relation discussed in equation (1) is the main reason for decreasing the power consumption when decreasing the core voltage of FPGA at high frequencies. It is to be noted that working of laser driver at below base core voltage of FPGA divert the laser driver in halt mode and system is unable to generate the output for this each time we have to rest the board and again have to set the programing for voltage scaling. In future the laser driver can be implemented using the ultra-scale FPGA, the power can be still downed for 500 THz or more frequency ranges.

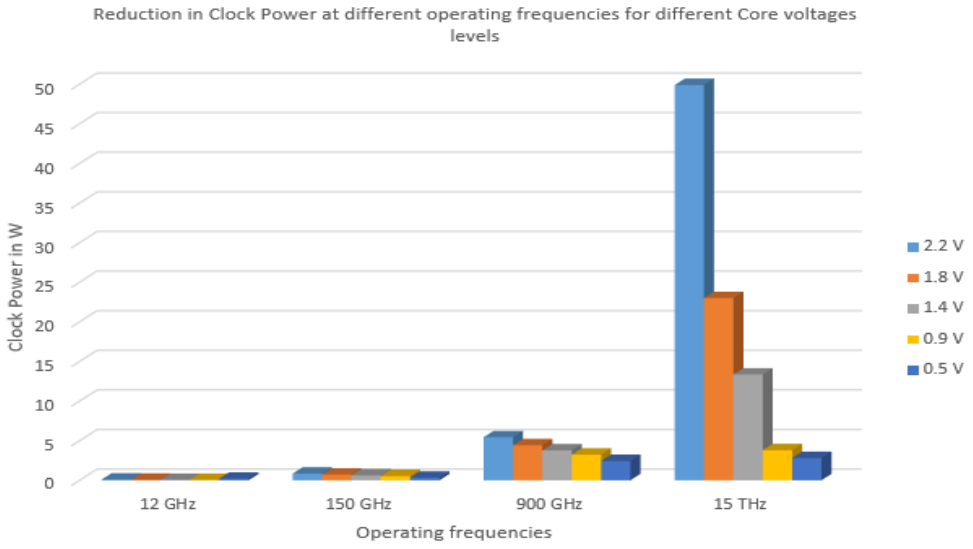

Figure-4. Decline in clock power in [W].

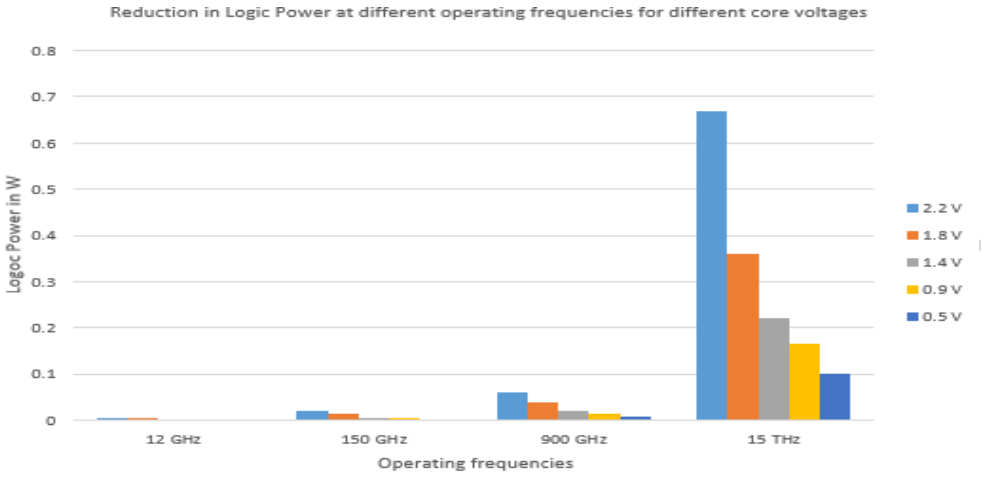

Figure-5. Decline in logic power in [W].

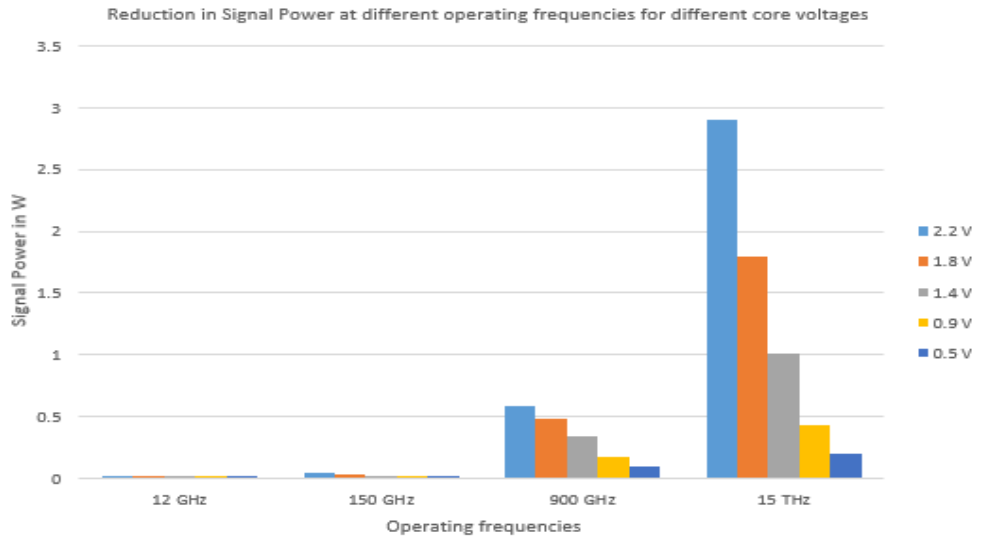

Figure-6. Decline in signal power in [W].

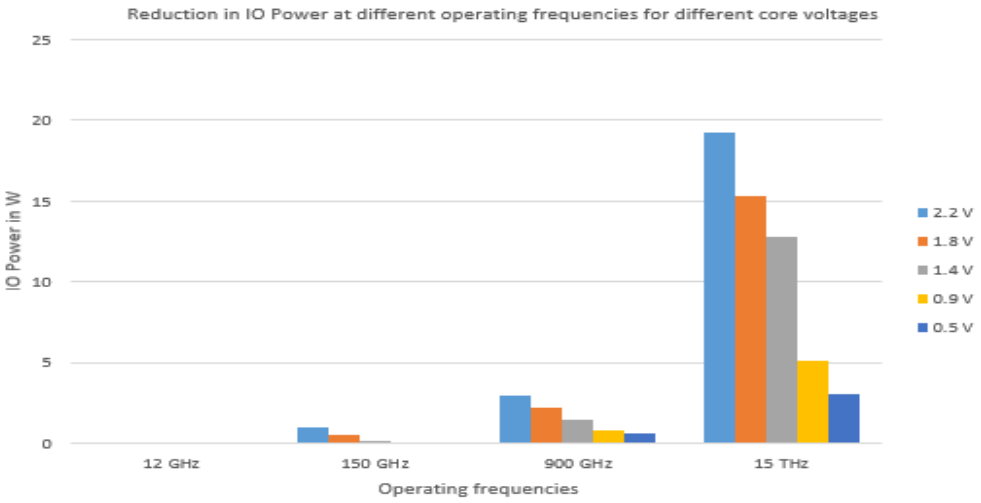

Figure-7. Decline in IO power in [W].

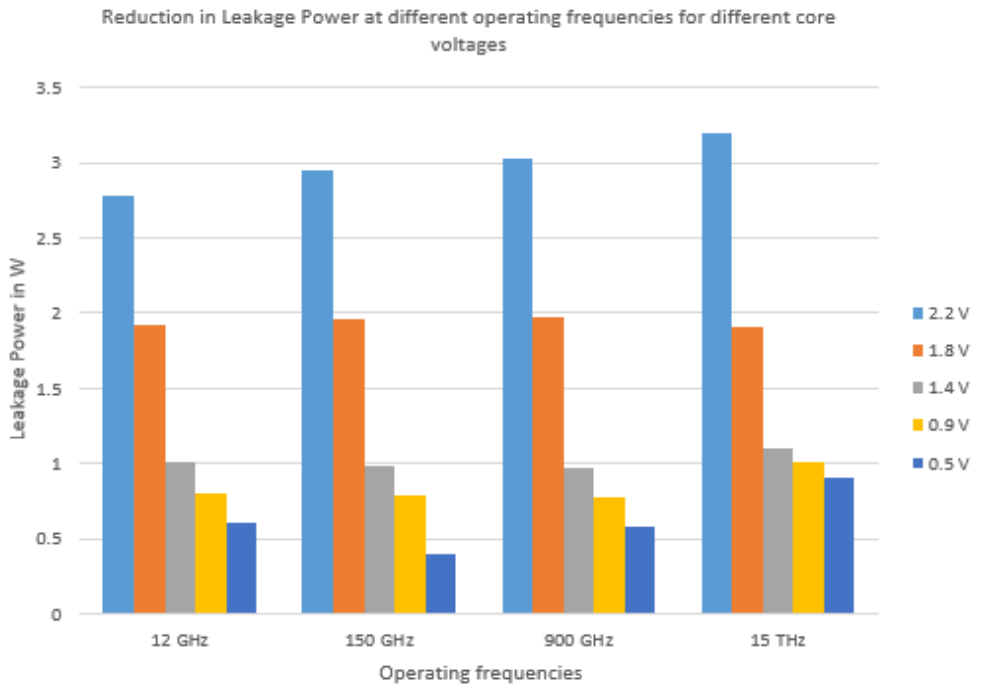

Figure-8. Decline in leakage power in [W].

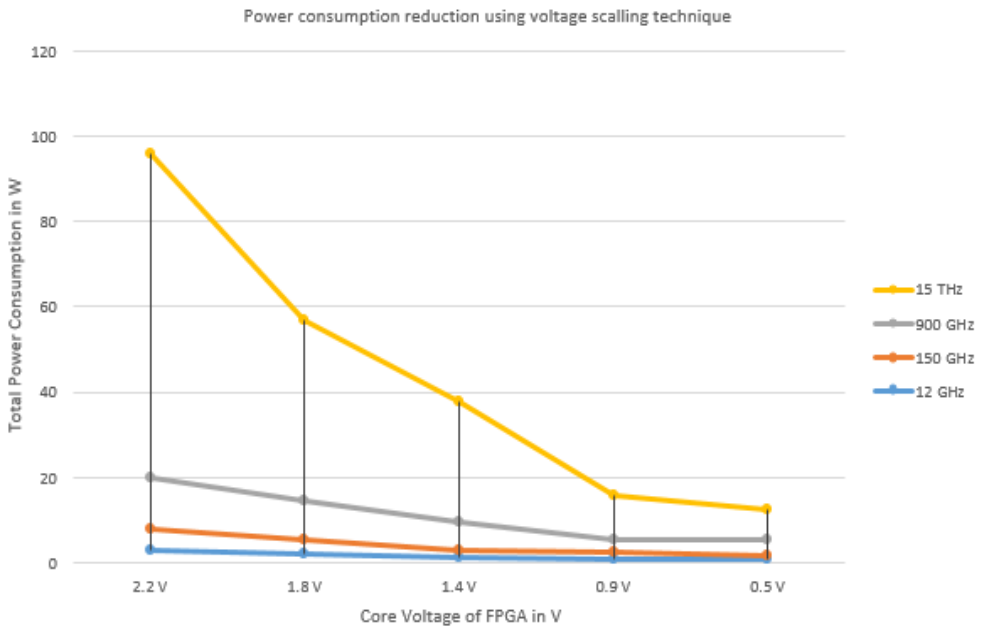

Figure-9. Total power reduction in [W].

CONCLUSIONS

In this work, demonstration of energy efficient laser driver is performed using FPGA based scaling and current mode logic. It is concluded that, significant power is reduced for the laser driver. With this research work, laser driver can be safely interfaced with other optical components in the system up to the frequency of 15 THz. This energy efficient laser driver can be integrated with optical components to make green optical communication systems. There is also a choice to redesign this laser driver using other latest FPGA series to increase the energy efficiency. In the society there is always need to save the power at low cost and this research will surely open the doors for designing the low power, low cost optical components.

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