VOL. 11, NO. 6, MARCH 2016 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

OPTIMIZATION OF PROCESS PARAMETER VARIATIONS ON THRESHOLD VOLTAGE IN ULTRATHIN PILLAR VERTICAL DOUBLE GATE MOSFET DEVICE

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ABSTRACT

In the fabrication of MOSFET devices, the process parameters play a very important role in deciding the MOSFET device's characteristics. The process parameter variations may contribute a significant impact on the dopant profiles that directly affect the device characteristics. These variations cause significant unpredictability in the power and performance characteristics of the device that may cause the degradation of the device performance. Therefore, a special technique involving design and analytical experiments is required to identify the process parameters that contribute the most of these variations In this current study, the L_{27} orthogonal array of Taguchi method was utilized to optimize the variability of process parameters on threshold voltage (V_{TH}) in Ultrathin Pillar Vertical Double Gate MOSFET Device. This work was initially performed by using Silvaco technology computer-aided design (TCAD) simulator consisted of a process simulator (ATHENA) and a device simulator (ATLAS). These two simulators were combined with the L_{27} orthogonal array of Taguchi method in order to obtain the robust design recipe. The results revealed that the halo implant tilt was the most dominant process parameter that had the strongest effect on threshold voltage (V_{TH}). Meanwhile, halo implant dose was selected as an adjustment factor in order to obtain the desired threshold voltage (V_{TH}) value. The most optimum V_{TH} value was observed to be 0.443 V and it is only 0.89% lower than the target or nominal value (0.447 V). This value is still within the predicted range of ITRS 2013 for low power (LP) multi-gate (MG) technology requirement in the year 2020.

Keywords: analysis of variance, taguchi method, threshold voltage, signal-to-noise ratio.

INTRODUCTION

Over the past decades, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has continually been scaled down in dimension and in channel length from micrometer to nanometer range as predicted by Moore's law. The MOSFET's size reduction is demanded due to the mass production of micro-technology devices. Furthermore, the size reduction of the MOSFET's device makes great improvement in MOSFET's operation (Taur and Ning, 1998). The main reason why MOSFET device has been attempted to be scaled down is to pack more and more MOSFET devices in a given chip area.

Designing a conventional planar MOSFET device with a very small channel length, especially for below the 22nm technology node is very complicated and difficult. An attempt of reducing the physical gate (Lg) of conventional MOSFET device has resulted in the drain region to be much closer to the source region, thereby introducing the short channel effects (SCEs) which eventually lead to the increase of leakage current (I_{OFF}). One of the popular methods to circumvent this matter is by implementing a combination of high permittivity (high-k) dielectric material and metal gate in MOSFET's structure. However, in this current work, the traditional silicon dioxide (SiO_2) and polysilicon material are still being used by utilizing vertical DG-MOSFET design concept.

The vertical DG-MOSFET device consists of ultrathin silicon (Si) pillar that isolates the two polysilicon gates as depicted in Figure-1. The main purpose of double gates is to control the channel from both sides in order to produce a better electrostatic control over the channel (Kaharudin *et al.*, 2014). The vertical shape of the ultrathin Si-pillar will boost the saturation current or the drive current (I_{ON}).

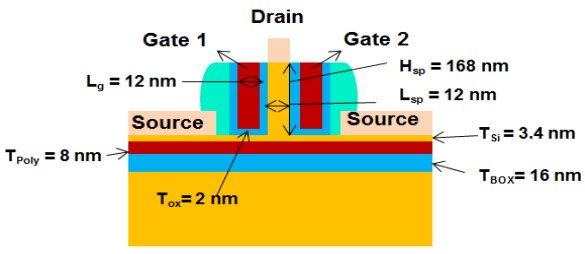

Figure-1. Vertical DG-MOSFET layout.

Since the drain region of vertical DG-MOSFET device is located at the top, the effective channel length

(Lc) does not depend on the physical gate length (Lg). Therefore, the SCEs phenomenon will be well mitigated and suppressed. Another advantage of vertical DG-MOSFET device is it can be easily integrated with planar MOSFET as depicted in Figure-2 (Masahara *et al.*, 2004).

At present day, MOSFET's process invariability utilizes ion implantation into the channel region, which eventually alters the doping profile near the surface of silicon substrate (Kang and Leblebici, 2003). Ion implantation technique involves doping concentration, doping energy and tilt angle. By altering the dosage, energy and rotation of these implants, the profile and characteristics of the MOSFET device will also be affected (Ninomiya *et al*., 2009), (Wang *et al*., 2005). One of the most important electrical characteristics of MOSFET's device is its threshold voltage (V_{TH}). V_{TH} is defined as the minimum voltage that is required to create a channel between the source and the drain. In other words, it is the minimum voltage required for strong inversion to occur (Croon *et al.*, 2002). V_{TH} value is strongly influenced by process parameters variation. Therefore, the analysis of variability has become a very important tool in order to predict the response variation in a very early design cycle due to process parameter spreads (Nassif *et al.*, 1984). The variations will impact the performance of device which may lead to the degradation of yield in modern technologies and application (Sylvester et al., 2008).

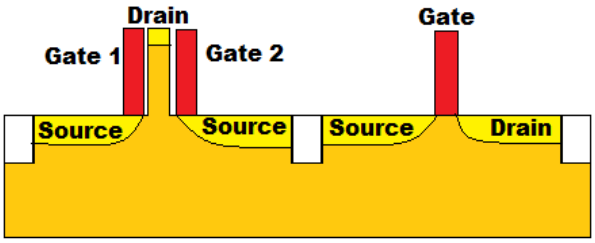

Figure-2. Integration with planar MOSFET.

In the previous research, the L_{12} orthogonal array of Taguchi method has been utilized to optimize the process parameter variations for higher on-current (I_{ON}) in the vertical double-gate MOSFET device (Kaharudin *et al*., 2014). The result shows that Taguchi method was capable of predicting the robust process recipe for the device in obtaining the highest I_{ON} value. This paper emphasizes on utilizing L_{27} orthogonal array of Taguchi method that consists of thirteen process parameters which are substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, halo implant energy, halo implant tilt, source/drain (S/D) implant dose, compensation implant dose, compensation implant energy and etc. The gate oxide temperature and polysilicon oxidation temperature are selected as noise factors in order to get the optimum results. The main objective of the current work is to acquire the nominal value of V_{TH} as predicted by International Technology Roadmap Semiconductor (ITRS) 2013. Specifically, the threshold voltage (V_{TH}) value must be within ±12.7% of low power (LP) multi-gate (MG) technology requirement in ITRS 2013 prediction (0.447V) for year 2020 as listed in Table-1 (ITRS, 2013).

Table-1. ITRS 2013 Prediction for Multi-gate (MG) Technology (ITRS, 2013).

Device characteristic	ITRS 2013 Prediction for low power (LP) Multi-gate (MG) requirement in year 2020
Physical Gate Length (L_g)	12.2 nm
Threshold Voltage (V_{TH})	0.447 V
Drive Current (I_{ON})	≥ 533 μA/μm
Leakage Current (I_{OFF})	≤ 20 ρA/μm

MATERIAL AND METHODS

Virtual fabrication

The process started with selection of a p-type silicon with <100> orientation as the main substrate by implanting 1 x 10^{14} atom/cm^3 of boron into silicon substrate. Buried oxide (BOX) of 16nm (t_{BOX}) was then developed beneath the silicon substrate. The remaining silicon substrate at the top was etched in order to form an ultrathin Si-pillar with length of 12 nm (Lsp) and height of 168 nm (Hsp). The function of ultrathin Si-pillar was to form a very sharp vertical channel that could increase the drive current (I_{ON}). The virtual process was followed by the gate oxidation process at temperature of 920^o C. Since the device was an n-channel type, 9.81 x 10^{12} atom/cm^3 of boron was implanted into the substrate at 20 Kev energy and 7^o tilt in order to form p+ region.

Polysilicon material was then deposited at the top of the gate oxide. After that, both polysilicon and polysilicon oxide were etched away to form a very thin gate with length of 12nm (Lg). In order to enhance performance of the device, 2.61 x 10^{13} atom/cm^3 concentration of indium was doped at energy level of 170 Kev and tilt angle of 24^o (Halo implantation). Halo implantation was followed by depositing sidewall spacers. Sidewall spacers were used as a mask for source/drain implantation process. Arsenic atom with concentration of 1.22 x 10^{20} atom/cm^3 was implanted in order to supply free electron to form n+ region as conductive channel.

Compensation implantation was utilized later by implanting phosphor dosage of 2.51 x 10^{12} atom/cm^3 with energy level of 60 Kev and tilt angle of 7^o. The function of compensation implantation was to reduce parasitic effects that could increase the leakage current (I_{OFF}). Next, silicide (CoSi) was formed on the source and drain region by sputtering cobalt on silicon surface. The vast majority of the silicide exhibit metallic conductivity and the silicide-

silicon junction will behave as a metal-semiconductor contact (Chen, 2005).

This device was then connected with aluminum metal. The aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts (Kaharudin *et al.*, 2014), (Salehuddin *et al*., 2014). The procedure was completed after the metallization and etching were performed for electrode formation, and the bonding pads were opened. The final structure of the device was completed by mirroring the right-hand side structure. The completed structure of ultrathin Si-pillar vertical DG-MOSFET device is illustrated as in Figure-3.

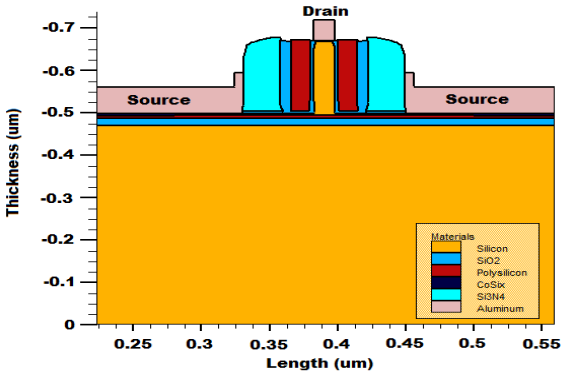

Figure-3. Structure of vertical DG-MOSFET device.

Taguchi L_{27} orthogonal array method

Taguchi method was utilized in order to optimize process parameter variations on threshold voltage (V_{TH}) in vertical DG-MOSFET device. The Taguchi method consists of a special orthogonal array that consists of twenty seven rows of the experiment. The Taguchi method has a capability of selecting the best level's combination of process parameters with less number of experiments. In the current research, Taguchi L_{27} orthogonal array was used to investigate the impact of 13 process parameters on threshold voltage (V_{TH}). The design of experiments (DoE) of 27 experiment rows with a different combination level of process parameters was constructed in Table-2.

Table-2. L_{27} Orthogonal array Taguchi method.

Exp No.	Process parameter level												
	A	B	C	D	E	F	G	H	J	K	L	M	N
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
2	1	1	1	1	2	2	2	2	2	2	2	2	2
3	1	1	1	1	3	3	3	3	3	3	3	3	3
4	1	2	2	2	1	1	1	2	2	2	3	3	3
5	1	2	2	2	2	2	2	3	3	3	1	1	1
6	1	2	2	2	3	3	3	1	1	1	2	2	2
7	1	3	3	3	1	1	1	3	3	3	2	2	2
8	1	3	3	3	2	2	2	1	1	1	3	3	3
9	1	3	3	3	3	3	3	2	2	2	1	1	1
10	2	1	2	3	1	2	3	1	2	3	1	2	3
11	2	1	2	3	2	3	1	2	3	1	2	3	1
12	2	1	2	3	3	1	2	3	1	2	3	1	2
13	2	2	3	1	1	2	3	2	3	1	3	1	2
14	2	2	3	1	2	3	1	3	1	2	1	2	3
15	2	2	3	1	3	1	2	1	2	3	2	3	1
16	2	3	1	2	1	2	3	3	1	2	2	3	1
17	2	3	1	2	2	3	1	1	2	3	3	1	2
18	2	3	1	2	3	1	2	2	3	1	1	2	3
19	3	1	3	2	1	3	2	1	3	2	1	3	2
20	3	1	3	2	2	1	3	2	1	3	2	1	3
21	3	1	3	2	3	2	1	3	2	1	3	2	1
22	3	2	1	3	1	3	2	2	1	3	3	2	1

23	3	2	1	3	2	1	3	3	2	1	1	3	2
24	3	2	1	3	3	2	1	1	3	2	2	1	3
25	3	3	2	1	1	3	2	3	2	1	2	1	3
26	3	3	2	1	2	1	3	1	3	2	3	2	1
27	3	3	2	1	3	2	1	2	1	3	1	3	2

The nominal or target value of V_{TH} is expected to be closed to 0.447 V as predicted by ITRS 2013 for low power (LP) multi-gate (MG) technology in the year 2020. A total of 108 runs are required in order to optimize the process parameters variation in Vertical DG-MOSFET device. All the values of process parameters and noise factors with their corresponding levels are listed in Table-3 and Table-4.

Table-3. Process parameters and their levels.

Sym.	Process parameter	Units	Level 1	Level 2	Level 3
A	**Substrate Implant Dose**	**atom/cm^3**	**1E14**	**1.03E14**	**1.06E14**
B	V_{TH} Implant Dose	atom/cm^3	9.81E12	9.84E12	9.87E12
C	V_{TH} Implant Energy	kev	20	21	22
D	V_{TH} Implant Tilt	degree	7	10	13
E	Halo Implant Dose	atom/cm^3	2.61E13	2.64E13	2.67E13
F	Halo Implant Energy	kev	170	172	174
G	Halo Implant Tilt	degree	24	27	30
H	S/D Implant Dose	atom/cm^3	1.22E20	1.25E20	1.28E20
J	S/D Implant Energy	kev	43	45	47
K	S/D Implant Tilt	degree	80	83	86
L	Compensation Implant Dose	atom/cm^3	2.51E12	2.54E12	2.57E12
M	Compensation Implant Energy	kev	60	62	64
N	Compensation Implant Tilt	degree	7	10	13

Table-4. Noise factors and their levels.

Symbol	Noise factor	Units	Level 1	Level 2
U	**Gate Oxidation Temperature**	**C^o**	**920**	**923**
V	Polysilicon Oxidation Temperature	C^o	870	873

RESULTS AND DISCUSSIONS

The electrical characterization of the device was then simulated by using ATLAS module. Next, the L_{27} orthogonal array of Taguchi method was implemented in order to obtain the possible nominal value of the threshold voltage (V_{TH}).

Characterization of vertical DG-MOSFET device

Figure-4 shows the graph of drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05 V and voltage V_D = 1.0 V for vertical DG-MOSFET device. The expected nominal value of threshold voltage (V_{TH}) for this device is 0.447 V (ITRS, 2013). However, the V_{TH} value extracted from the graph was only 0.401 V. There was a decrease of 0.046 V from the nominal or target value.

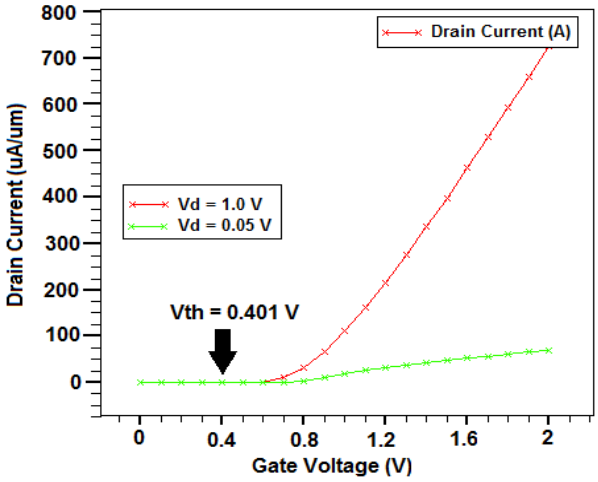

Figure-4. Graph of drain current (I_D) versus gate voltage (V_G).

Figure-5 shows the graph of subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05V and V_D = 1.0V for vertical DG-MOSFET device. The value of off-leakage current (I_{OFF}) and drive current (I_{ON}) were extracted from the graph.

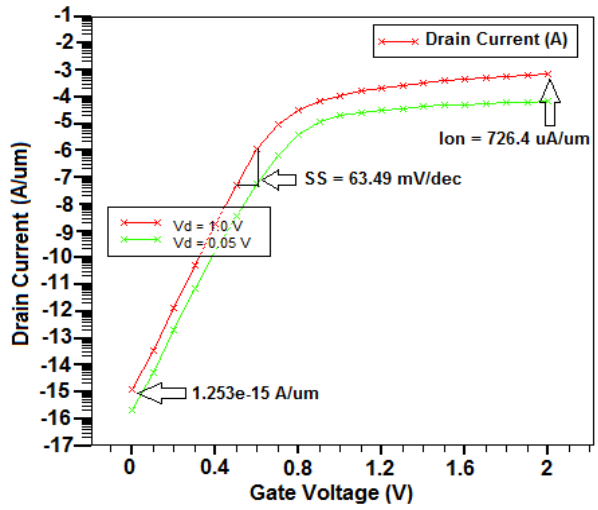

Figure-5. Graph of subthreshold drain current (I_D) versus gate voltage (V_G).

From the graph, it was observed that the value of drive current (I_{ON}) was 726.4 µA/µm. Meanwhile, the off-leakage current (I_{OFF}) was observed to be 1.253e-15 A/µm. A very low leakage current (I_{OFF}) indicates a better suppression of short channel effect (SCE) problems. The value of subthreshold swing (SS) was calculated by using (1) (Ferrain *et al*., 2013):

$$SS = \left[\frac{dV_{GS}}{d(\log_{10} I_{DS})}\right] \quad (1)$$

The initial value of subthreshold swing (SS) was observed to be 63.49 mV/dec. Subthreshold swing (SS) is regarded as an important characteristic in MOSFET's device as it indicates how fast the switching transition from "ON" to "OFF" state or vice versa.

Signal-to-noise ratio (SNR) analysis

After 27 runs of experiment have been performed, the next step is to determine the most significant process parameters that contribute the most impact on device characteristics. The L_{27} orthogonal array analysis for threshold voltage (V_{TH}) values recorded in Table-5.

Table-5. Threshold voltage values for vertical DG-MOSFET device.

Experiment no.	Threshold voltage , V_{TH} (V)			
	V_{TH1} (U1V1)	V_{TH2} (U1V2)	V_{TH3} (U2V1)	V_{TH4} (U2V2)
1	0.401	0.412	0.419	0.434
2	0.389	0.402	0.407	0.423
3	0.347	0.358	0.364	0.38
4	0.396	0.407	0.413	0.429
5	0.371	0.384	0.39	0.407
6	0.339	0.351	0.357	0.373
7	0.38	0.392	0.399	0.414
8	0.375	0.388	0.392	0.41
9	0.329	0.341	0.348	0.363
10	0.31	0.322	0.328	0.342
11	0.412	0.424	0.431	0.447
12	0.381	0.423	0.4	0.414
13	0.317	0.328	0.335	0.35
14	0.422	0.435	0.444	0.46
15	0.397	0.439	0.417	0.431
16	0.325	0.336	0.342	0.357
17	0.416	0.428	0.435	0.451
18	0.406	0.448	0.425	0.439
19	0.369	0.381	0.387	0.403
20	0.317	0.328	0.335	0.349
21	0.421	0.433	0.442	0.454
22	0.375	0.387	0.394	0.407
23	0.338	0.349	0.356	0.37

24	0.433	0.445	0.454	0.468
25	0.374	0.385	0.393	0.408
26	0.327	0.338	0.346	0.359
27	0.433	0.446	0.456	0.47

After obtaining all the results, all the process parameters of Vertical DG-MOSFET device were optimized by using Taguchi method. Taguchi method was assigned to analyze the V_{TH} values using SNR analysis of Nominal-the-best. The SNR (Nominal-the-better), η can be expressed as (Phadke, 1998):

$$\eta = 10 Log_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (2)$$

Where as:

$$\mu = \frac{Y_i + ...+ Y_n}{n} \quad (3)$$

and

$$\sigma^2 = \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1} \quad (4)$$

where n is number of tests and yi is the experimental values of V_{TH}. By utilizing formula given in (2), the SNR for each row of experiments were computed and recorded in Table-6.

Table-6. SNR for threshold voltage in vertical DG-MOSFET Device.

Exp. No	Mean	Variance	SNR (Mean), dB	SNR (Nominal-the-best), dB
1	0.417	1.91E-04	-7.61	29.58
2	0.405	1.98E-04	-7.85	29.20
3	0.362	1.90E-04	-8.82	28.40
4	0.411	1.90E-04	-7.72	29.50
5	0.388	2.23E-04	-8.22	28.29
6	0.355	2.00E-04	-9.00	27.99
7	0.396	2.02E-04	-8.04	28.91
8	0.391	2.09E-04	-8.15	28.65
9	0.345	2.02E-04	-9.24	27.72
10	0.326	1.77E-04	-9.75	27.77
11	0.429	2.14E-04	-7.36	29.34
12	0.405	3.35E-04	-7.86	26.89
13	0.333	1.91E-04	-9.56	27.63
14	0.440	2.55E-04	-7.13	28.81
15	0.421	3.39E-04	-7.51	27.19
16	0.340	1.78E-04	-9.37	28.13
17	0.433	2.14E-04	-7.28	29.42
18	0.430	3.35E-04	-7.34	27.41
19	0.385	2.00E-04	-8.29	28.70
20	0.332	1.80E-04	-9.57	27.89
21	0.438	1.95E-04	-7.18	29.92
22	0.391	1.79E-04	-8.16	29.31
23	0.353	1.80E-04	-9.04	28.42
24	0.450	2.18E-04	-6.94	29.68
25	0.390	2.05E-04	-8.18	28.71

26	0.343	1.82E-04	-9.31	28.10
27	0.451	2.45E-04	-6.91	29.20

Generally, the experiment row, which has the highest SNR will be recognized as the best performance characteristics. Based on Table 6, it was observed that experiment row 21 had the highest SNR value for V_{TH} which was observed to be 29.92dB. This indicates that experiment of row 21 possessed the best insensitivity for V_{TH}. Since the design of experiment (DoE) was orthogonally constructed, the SNR of each process parameters can be separated out. The SNR (Nominal-the-best) was summarized in Table-7.

Table-7. SNR of process parameters in vertical DG-MOSFET device.

Process parameters	Signal-to-noise ratio (SNR)			Overall mean SNR
	Level 1	Level 2	Level 3	
A	28.69	28.06	28.88	28.55
B	28.63	28.54	28.47	
C	28.84	28.42	28.38	
D	28.53	28.58	28.52	
E	28.69	28.68	28.27	
F	28.21	28.72	28.71	
G	29.37	28.26	28.00	
H	28.57	28.58	28.50	
J	28.49	28.65	28.50	
K	28.63	28.52	28.49	
L	28.43	28.56	28.65	
M	28.42	28.60	28.61	
N	28.62	28.48	28.54	

Based on Table-7, the factor effects graph for SNR (Nominal-the-best) was plotted as illustrated in Figure-6. The dashed horizontal lines in both graphs represent the overall mean of SNR (Nominal-the-best) and SNR (Mean) which were 28.55 dB and -8.20 dB.

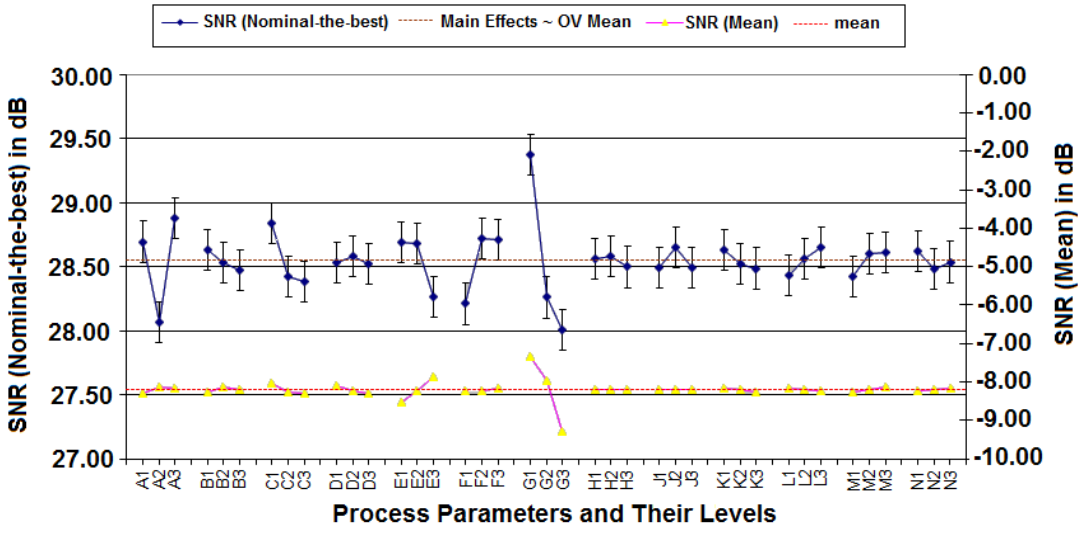

Figure-6. Factor effect plot for SNR (Nominal-the-best) and SNR (Mean) for threshold voltage.

From Figure-6, it was observed that factor A3, B1, C1, D2, E1, F2, G1, H2, J2, K1, L3, M3 and N1 have been selected as the optimum value for V_{TH} due to their highest SNR. Factor A, B, C, D, E, F, G, H, J, K, L, M and N represents Substrate Implant Dose, V_{TH} Implant Dose, V_{TH} Implant Energy, V_{TH} Implant Tilt, Halo Implant dose, Halo Implant Energy, Halo Implant Tilt, S/D Implant Dose, S/D Implant Energy, S/D Implant Tilt, Compensation Implant Dose, Compensation Implant Energy and Compensation Implant Tilt accordingly.

Analysis of Variance (ANOVA)

The common practical method in investigating the relative effect of different process parameters on V_{TH} were realized by decomposition of variance which was called analysis of variance (ANOVA) (Salehuddin *et al*., 2013). ANOVA computes parameters which are known as sum of squares (SSQ), degree of freedom (DF), variance or mean square (MS), F-value and percentage of effect on each factor or process parameter. The results of ANOVA for V_{TH} in Vertical DG-MOSFET device are listed in Table-8. F-test was statistically conducted in order to provide a decision at some confidence level to determine the significance of certain factor (process parameter). A larger F-value implies that the variation of certain process parameter has contributed a large effect on the device performance (Kamaruddin *et al*., 2010).

Table-8. Results of ANOVA for V_{TH} in vertical DG-MOSFET device.

Sym.	DF	SSQ	MS	F-value	Factor effects on SNR (%)	Factor effects on mean (%)
A	2	3	2	9402	19	1
B	2	0	0	333	1	0
C	2	1	1	3316	7	2
D	2	0	0	54	0	1
E	2	1	1	3030	6	9
F	2	2	1	4361	9	0
G	2	10	5	27290	55	87
H	2	0	0	95	0	0
J	2	0	0	413	1	0
K	2	0	0	274	1	0
L	2	0	0	598	1.20	0.07
M	2	0	0	597	1	0
N	2	0	0	239	0	0

At least 95% confidence

According to Table-8, the most dominant process parameters with respect to output response (V_{TH}) were observed to be factor A (Substrate Implant Dose = 19%) and G (Halo Implant Tilt = 55%). Therefore, these factors should be set at "best setting" and cannot be used as adjustment factor. Meanwhile factor C (V_{TH} Implant Energy = 7%), E (Halo Implant Dose = 6%) and F (Halo Implant Energy = 9%) were observed to be significant factors. Whereas, factor E (Halo Implant Dose) was described as an adjustment factor due to its large effect on mean (9%) and small effect on variance (6%) if compared to other factors. The percentage of factor effects on SNR indicates the priority of a factor (process parameter) to reduce variation (Salehuddin *et al.*, 2014). A factor with high percentage of contribution and a small variance (mean square) has a great influence on device's performance (Nalbant *et al*., 2007). The percentages of factor effect on SNR of all factors are visualized as in the pareto chart in Figure-7.

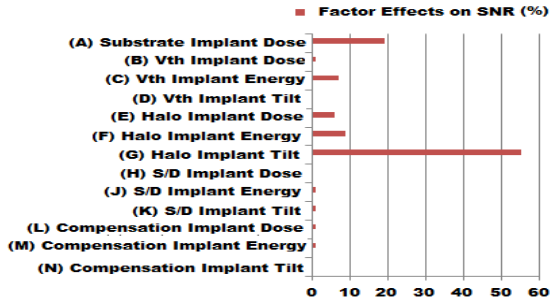

Figure-7. Pareto plot of factor effects on SNR for V_{TH}.

CONFIRMATION RUN

Confirmation run is the final step in the design of experiment (DoE) process. The main purpose of the confirmation run is to validate the results retrieved during analysis phase (Phadke, 1998). Confirmation run was performed by conducting an actual simulation test while using the overall best level setting of process parameters as predicted by Taguchi method before. Table-9 shows the overall best setting of process parameters in Vertical DG-MOSFET device.

Table-9. Overall best setting of process parameters.

Sym.	Process parameter	Units	Best value
A	**Substrate implant dose**	**atom/cm^3**	**1.06E14**
B	V_{TH} Implant Dose	atom/cm^3	9.81E12
C	V_{TH} Implant Energy	kev	20
D	V_{TH} Implant Tilt	degree	10
E	Halo Implant Dose	atom/cm^3	2.61E13
F	Halo Implant Energy	kev	172
G	Halo Implant Tilt	degree	24
H	S/D Implant Dose	atom/cm^3	1.25E20
J	S/D Implant Energy	kev	45
K	S/D Implant Tilt	degree	80
L	Compensation Implant Dose	atom/cm^3	2.57E12
M	Compensation Implant Energy	kev	64
N	Compensation Implant Tilt	degree	7

The confirmation run was then conducted by utilizing ATHENA and ATLAS module. The electrical characteristic results of the confirmation run are listed in Table-10. Before the optimization approaches, the best SNR (Nominal-the-best) was 29.92 dB at experiment row 21 in Table-6. Whereas the variance was 1.95E-04 V and mean for V_{TH} was 0.438 V. There was a decrease of 2.01% in this V_{TH} value from the nominal value, 0.447 V (ITRS, 2013).

Table-10. Final results of confirmation run for threshold voltage.

Threshold voltage (V)				**SNR** (Mean)	**SNR** (Nominal-the-best)
V_{TH1}	**V_{TH2}**	**V_{TH3}**	**V_{TH4}**		
0.409	0.421	0.429	0.443	-7.50	30.32

After the optimization approaches, the SNR (Nominal-the-best) and SNR (Mean) of V_{TH} for Vertical DG-MOSFET device was observed to be 30.32 dB and -7.50 dB respectively. These values are well within the predicted range. For SNR (Nominal-the-best), 30.32 dB is within the predicted SNR range of 30.74 to 29.89 dB (30.32±0.42 dB). Meanwhile, for SNR (Mean), -7.50 dB is within the predicted SNR range of -7.24 to -7.77 dB (-7.50±0.27 dB). The SNR (Nominal-the-best), 30.32 dB is observed to be the highest value among the others in Table VI which indicates the process parameters variation have been statistically optimized by Taguchi method.

The variance and threshold voltage (V_{TH}) for the device after optimization approaches were 2.04E-04 and 0.443 V respectively. The results show that the variance is slightly increased and V_{TH} value is closer to the nominal value (target). The V_{TH} value is only 0.89% lower than the target or nominal value (0.447 V). This V_{TH} value (0.443 V) is still within the predicted range of ITRS 2013 for low power (LP) multi-gate (MG) technology requirement in year 2020. These show that Taguchi method is able to predict the optimum solution in finding the Vertical DG-MOSFET fabrication recipe with appropriate threshold voltage (V_{TH}) value.

Several device characteristics of the vertical double-gate MOSFET device were recorded and compared to the ITRS 2013 prediction and the real fabrication results. The detail comparison of the results with the ITRS 2013 prediction and the real fabrication process is listed in Table-11. It was observed that there is a slight improvement of the device characteristics when the Taguchi method was applied for optimization approach.

The subthreshold swing (SS) value is desired to be small (55-65 mV/dec) for faster switching operation. Meanwhile, the on-current (ION) is desired to be as large as possible for better drive capability.

Table-11. Comparison of the results with ITRS 2013 and the real fabrication process.

Electrical responses	Results from this works	Results from real fabrication (Masahara *el al*., 2004)	ITRS 2013 Prediction (ITRS, 2013)
V_{TH} (V)	0.443	0.430	±12.7% of 0.447
I_{ON} (μA/μm)	696.6	570	≥ 533
SS (mV/dec)	63.64	69.8	-

CONCLUSIONS

In conclusion, the optimum solution in obtaining the desired threshold voltage (V_{TH}) value was successfully predicted by the combination of process simulation, device simulation and the L_{27} orthogonal array of Taguchi method. These tools are capable of predicting the process recipe of the device before it undergoes to real fabrication. Thus, the cost and time can be saved efficiently by the early prediction of the robust recipe. The threshold voltage (V_{TH}) is the main response investigated in this project as it is regarded as the main factor in determining the functionality of Vertical DG-MOSFET device. The L_{27} orthogonal array of Taguchi method design is utilized to be a systematic platform in studying the main effect of multiple factors (process parameters) upon threshold voltage (V_{TH}). Based on ANOVA method, the process parameters that contribute the most impact on threshold voltage (V_{TH}) were found to be and halo implant tilt (55%), substrate implant dose (19%), Halo Implant Energy (9%), V_{TH} Implant Energy (7%) and Halo Implant Dose (6%) whereas the halo implant dose was described as an adjustment factor. The final results indicate that the V_{TH} value is closer to the nominal value (target). The V_{TH} value (0.443 V) is observed to be only 0.89% lower than the target or nominal value (0.447 V) and it is still within the predicted range of ITRS 2013 for low power (LP) multi-gate (MG) technology requirement in the year 2020.

ACKNOWLEDGEMENT

The authors would like to thank to the Ministry of Higher Education (MOHE) and Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for sponsoring this study under the research grants (PJP/2014/FKEKK (6B)/S01341) and FRGS (RACE)/2012/FKEKK/TK02/02/2 F00148.

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