VOL. 11, NO. 6, MARCH 2016 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

HIGH EFFICIENCY CMOS CLASS-E POWER AMPLIFIERS IN GIGAHERTZ FREQUENCIES USING ADVANCED SEMICONDUCTOR PROCESS: A REVIEW

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ABSTRACT

This paper reviews of high efficiency CMOS class-E power amplifiers (PAs) in gigahertz (GHz) frequencies for wireless applications. The study is focused on the challenges in designing class-E PA especially in GHz frequencies. Problems and limitations in high efficiency class-E PA and the circuits' topologies are reviewed. Several works on CMOS class-E PA from year 1999 to 2014 are discussed in this paper. Recent developments of CMOS class-E PAs are examined and a comparison of the performance criteria of various topologies is presented.

Keywords: high efficiency, CMOS class-E, power amplifier, circuit topology, performance criteria.

INTRODUCTION

The class-E power amplifier (PA) was first introduced by N.O. Sokal and A. D. Sokal in year 1975 (Sokal, 1975). Theoretically, the class-E PA can achieve a 100% of drain efficiency, thus becoming an interested topic of the most research area in designing PAs. Class-E PA is the most popular candidate among all classes of switching type power amplifiers such as class-D and class-F due to high efficiency and simpler circuitry (Sohiful Anuar Zainol Murad *et al*., 2010). As kind of switching type amplifiers, it's has a potential for providing greatly power added efficiency (PAE) compared with linear amplifiers i.e. a class-A and class-B PA (Sohiful Anuar Zainol Murad *et al*., 2010). Ideally, the high efficiency can be achieved by shaping the voltage waveform and current waveform so that they are not overlapping to each other [3-7]. Generally, class-E PAs are well suited to systems with constant envelop modulation scheme such as FSK (or FM) due to the linearity is very poor because of the switching nature (Murad, S.A.Z *et al*., 2010). Late 1995, the demands for compact, low-cost, and low power wireless portable devices were increasing. These demands have promoted to realize a single chip radio transceiver in a low cost CMOS technology with extra functionality (K.C. Tsai and P.R. Gray, 1999, Murad, S.A.Z *et al*., 2010) (P.Gray, R. Meyer, 1995). There have been reported several fully integrated class-E PAs in CMOS since 1999 for wireless applications (A. Rofougaran *et al*., 1998, Hyuk Su Son, 2013).

This paper is organized as follows. The problems and limitation in class-E PA is discussed in Section II. Section III deals with the proposed PA circuits techniques for high efficiency with the solving of problems as explained in section II. A summarized finding is discussed in Section IV and the conclusion is given in Section V.

PROBLEM AND LIMITATION

Much research has been focused on switching type PAs, class-E in particularly due to easy implementation and integratable on single chip CMOS transceivers. The switching operation and zero voltage switching condition allows a strong reduction of power losses, hence increase the efficiency of transmitting power (A. Mazzanti *et al*., 2006). The designing and implementing of CMOS PAs is a major challenge particularly when designing in GHz frequencies range. In addition, realizing high efficiency class-E PAs are impeded due to the problem such as low oxide breakdown voltage, low current drive capability, substrate coupling, low quality and high tolerances of on chip passives (A. Mazzanti, L. Larcher, R. Brama and F. Svelto, 2006, Tirdad Sowlati and Domine M.W. Leenaerts, 2003). As a down scaling of MOS devices continues, the CMOS PA is not the optimum technology of choice.

Technology down scaling

The safe operating voltage is decreased as the minimum channel length of the MOS transistor scales down. Therefore, the supply voltage of the power amplifier should be reduced accordingly to avoid stress on active device. Since the relationship between output power (Pout) is proportional to the square root of supply voltage (V_{dd}) and inversely proportional to the load resistance ($RL_{\_opt}$) (Changsik Yoo, 2001), requires the optimum load resistance $RL_{\_opt}$ seen by the power amplifier to be reduced for the given output power. It's quite hard to realize a good PA with the lower supply voltage and load resistance. Such a low optimum load resistance of the power amplifier is realized by a matching network to be matched with antenna input impedance, usually 50 Ω. The power loss due to the impedance matching network is proportional to the impedance transformation ratio of m =

$50/RL_{\_opt}$ as given in equation (1) in (Changsik Yoo, 2001), if a simple low-pass L-section matching network is used, where Q is the reactive components' quality factor. Thus, the smaller load resistance $RL_{\_opt}$ required for a down-scaling CMOS technology results in larger losses in impedance matching network thus lower efficiency (Changsik Yoo, 2001). This is one of the major problems of efficiency degradation.

The second losses is coming from the finite switch on-resistance r_{on} as a technology scale down the efficiency is degraded. In triode region, the finite switch on-resistance r_{on} can be represented in equation (5) as in (Ping Song and Howard, C.L., 2005). If the technology is scaled down, ron is reduced due to the decreasing channel length and increasing transconductance coefficient. However, for the given output power and supply voltage, the reduction of r_{on} is slower than the reduction of the $RL_{\_opt}$ (Changsik Yoo, 2001). Therefore, the ratio of r_{on} / $RL_{\_opt}$ is increased, thus degrade the power efficiency of the amplifier as shown in equation (6) in (Ping Song and Howard, C.L., 2005). However, the ration of ron/ $RL_{\_opt}$ can be neglected if the switch transistor wide enough to alleviate this problem but the switch transistor cannot be made wide because it could cause too large parasitic capacitance to be absorbed into the shunt capacitance of the load network. Therefore, the power loss due to the parasitic resistance in the inductor and capacitance also decreases the efficiency achievable as the technology scales down (Changsik Yoo, 2001).

Inductor parasitic

The gain of a simple amplifier topology with on-chip resonant LC tank is shown in equation (7) in (Ping Song and Howard, C.L., 2005). Normally, in CMOS technology, the quality factor (Q) of on-chip inductors is around 6, and the on-chip capacitors is higher than 20. However, the maximum gain and the power efficiency are limited by the low Q of the on-chip inductors. For example, a simple LC resonant circuit using low Q on-chip inductors are used as the loading of the input stage is not sufficient for the high gain since a large switching signal is required to drive the amplifier stage. Moreover, in a class-E PA, the amplifier stage switching transistor should have very large size to minimize the turn-on resistance, which in turn results in a large parasitic capacitor and limits the operation frequency (Ping Song and Howard, C.L., 2005). Therefore, the loading inductance of the first stage could be reduced to increase the frequency; however, that solution would decrease the gain in the first stage of class-E PA.

CLASS-E CIRCUIT TOPOLOGY

In general, a class-E PA consists of drive amplifier, switching stage and output matching network stage for both single-ended and fully differential topologies. The drive amplifier is needed to provide sufficient input power to properly switch a transistor so that there is no overlapping between drain voltage and current, thus increase the efficiency. The switching stage will perform switching action by turn-on and turn-off the transistor to ensure the drain voltage and current are never simultaneously nonzero, thus the switch is ideally lossless causing the potential for high efficiency operation. The output matching network is essential to transform the optimum output resistance for class-E amplifier to the load resistance of 50 Ω, which is normally the antenna impedance.

Single-ended cascode topology

The single-ended cascode topology is the simple circuitry for class-E PA. Moreover, the components driven by the PA and the antenna input are still single-ended; such a topology is easy to be implemented. Most of the switching stage class-E PAs are implemented cascode topology which consists of common-source (CS) transistor connected in series with the common-gate (CG) transistor to relax the device stress (A. Mazzanti *et al.*, 2006, Murad, S.A.Z *et al.*, 2010, Yonghoon Song *et al.*, 2009, Yonghoon Song *et al.*, 2010, Yamshita, Y. *et al.*, 2013, Hyuk Su Son *et al.*, 2013).

Figure-1 shows the schematic of single-ended cascode topology including driver and output stage (A. Mazzanti *et al.*, 2006). The proposed PA has been implemented in a 0.13-µm CMOS technology. All transistors have a think gate oxide to allow 2.8 V maximum supply voltage. The width of the CG device is selected to 3000 µm / 0.28 µm in order to minimize power loss due to r_{on} while the CS transistor is sized to 1800 µm / 0.28 µm. The output stage consists of LC network matching and the inductors are realized using bond wires except for L_p. The driver stage is biased in class-C. The proposed PA achieves power added efficiency (PAE) of 67 % with output power of 23 dBm. The supply voltage is 2.5 V at 1.7 GHz. However, this PA includes off-chip capacitor.

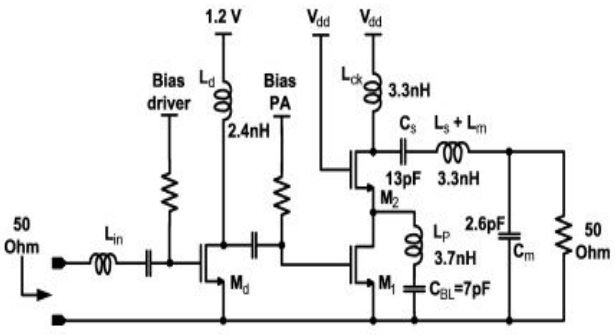


Figure-1. Complete schematic of class-E PA including driver and output stage (A. Mazzanti *et al.*, 2006).

The CS class-E amplifier with the cascode topology as a driver stage is proposed in (Saari, V. *et al.*, 2005). The biasing was implemented using current mirrors. The power stage consists of four transistors with 61 fingers were used, and low pass LC network was

implemented using an external microstrip and a surface mounted capacitor (Saari, V. *et al*., 2005). Figure-2 shows the implemented schematic of two-stage class-E PA. The proposed class-E PA delivers 21.3 dBm output power with 40% PAE at 3.3 V supply voltage. The disadvantage of this PA is implemented the off-chip capacitors, inductors and microstrip lines as a matching network.

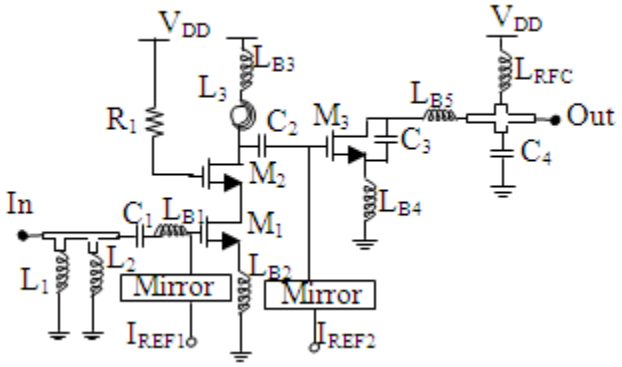


Figure-2. Schematic of two-stage class-E PA.

A new topology class-E PA is proposed in (Hyoung-Seok Oh *et al*., 2006) employs the power injection-locked in order to minimize the driving power as well as DC power consumption in the driver stage, while maintaining the class-E PA stage fully driven with high efficiency. The proposed PA can achieve high PAE with no degradation from high drain efficiency in the output stage (Hyoung-Seok Oh *et al*., 2006). The simplified circuit of injection-locked class-E PA is shown in Figure-3. The proposed PA obtains 43% of PAE with lower output power of 9.3 dBm at 1 V supply voltage.

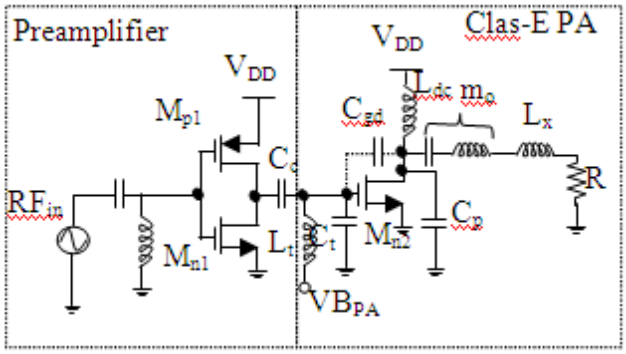


Figure-3. Schematic of the proposed injection-locked class-E PA.

The reduction of efficiency due to the shunt capacitance of class-E amplifier stage can be improved by tuning out the parasitic drain capacitance of amplifier stage. Therefore, a cascode class-E PA using negative capacitance to tune out parasitic capacitance without adding external circuits is proposed in (Yonghoon Song *et al*., 2009). The proposed circuit consists of cascode topology with difference gate-oxide thickness in order to get best performance with class-E driver stage. The proposed schematic is depicted in Figure-4. The proposed class-E PA with negative capacitance successfully obtained high efficiency of 63 % PAE and delivers 29 dBm output power at 1.8 GHz using 0.13-µm CMOS process. The supply voltage is 3.3 V and the matching network is off-chip.

In (Yamashita, Y, 2012), the design of 5 GHz CMOS class-E PA is proposed. The PA employs the cascode topology with a self-biasing technique to overcome device stress which is similar with the previously proposed PAs. The authors tried to implement three cascade class-D drive amplifiers in order to provide square-wave signal to the amplifier stage for high efficiency, however; the PA achieves only 35.4 % PAE and 16.4 dBm output power at 2.3 V supply voltage. The proposed schematic is shown in Figure-5. The authors also proposed a new class-E PA operating at the same frequency (Yamashita, Y, 2013). The proposed PA employs injection-locking technique to reduce required input power, and enable switches is used to turn ON or OFF PA stage with band pass filter at the output stage to eliminate harmonic distortion. The PA delivers 15.4 dBm output power with 40.6 % PAE at 2.0 V supply voltage.

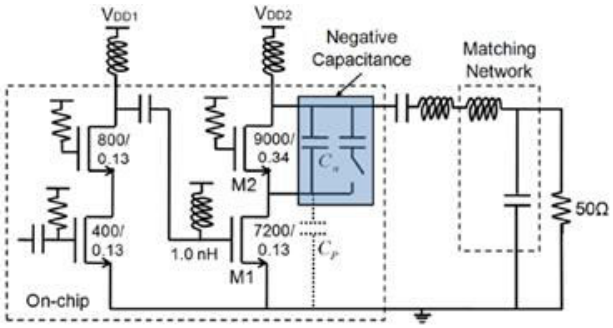
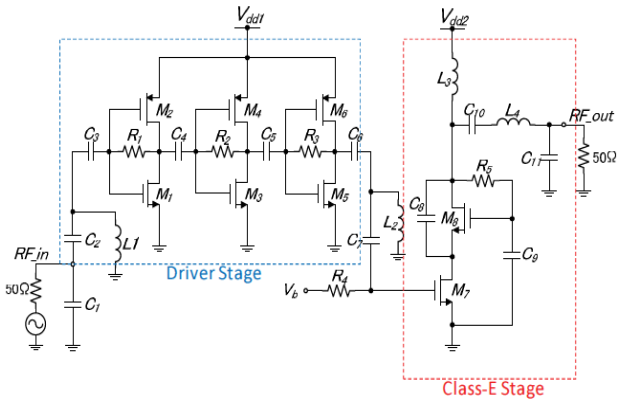
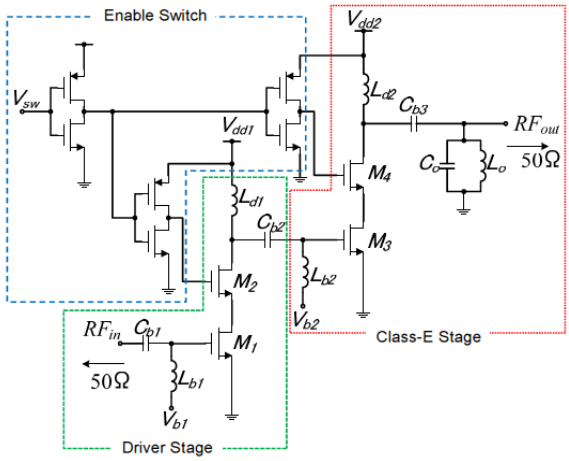


Figure-4. Schematic of proposed class-E PA with driver stage (Yonghoon Song *et al*., 2009).



(a)



(b)

Figure-5. Schematic of proposed class-E PA, (a) with three cascade class-D drive stage (Yamashita, Y, 2012), (b) with injection-locking technique and enable switch (Yamashita, Y, 2013).

The latest proposed work on a single-ended Class-E PA design is used power level control to swept voltage supply for increasing the efficiency (Montes, L.A.A. *et al*, 2014). The proposed PA obtains 59.2% of PAE and 18 dBm of output power. Figure-6 shows the self-biased class-E PA with power control.

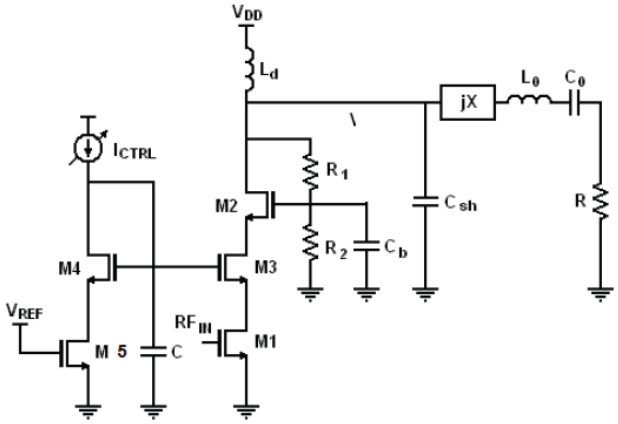


Figure-6. Schematic of the proposed differential class-E PA (Montes, L.A.A. *et al*, 2014).

Differential cascode topology

The differential cascade topology is composed of a common source amplifier and a common gate amplifier. Therefore, the problem of low breakdown voltage can be solved due to the drain output voltage can be spread over both transistor, thus almost twice of the supply voltage can be handled. It means that the load resistance can be four times large for a given output power (Zhisheng Li *et al*., 2012, Hyuk Su Son *et al*., 2013). In addition, this configuration is used to alleviate the problem of substrate coupling due to the current is discharged to ground twice per cycle. This remove the substrate noise component from the desired signal frequency to twice the signal frequency resulted in a reducing the interference problem (K.C. Tsai and P.R. Gray, 1999). Another advantage of this topology, with the same supply voltage and output power, the current passing through each transistor (switch) is lower than it in a single-ended topology. Therefore, a smaller transistor can be used on each side without increasing the total switch loss (K.C. Tsai and P.R. Gray, 1999).

The first CMOS differential class-E PA is proposed by King-Chun Tsai and Paul R. Gray in year 1999 (K.C. Tsai and P.R. Gray, 1999). The concept of mode locking is used in the design with off-chip microstrip balun for converting the output differential to single-ended signal. The proposed PA operate at 1.98 GHz achieves 48% of PAE and degradation about 7 % of PAE when combine with the off-chip balun. Figure-7 shows the schematic of the complete PA proposed in (K.C. Tsai and P.R. Gray, 1999).

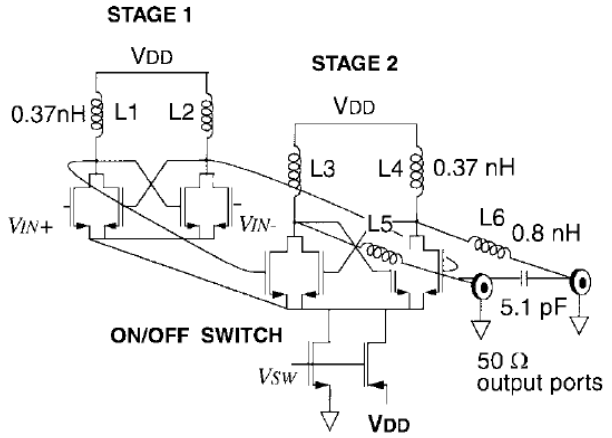


Figure-7. Schematic of the proposed differential class-E PA (K.C. Tsai and P.R. Gray, 1999).

In (Ka Wai Ho and Howard C. Luong, 2003), the fully differentiate PA employs driver stage with positive feedback to provide large swing for high efficiency and all inductors are realized using bond wires is proposed. Bond wires inductors are used to implement high Q to obtain a higher efficiency. However, the proposed PA need single ended to differential conversion at the input terminal and the differential to single-ended conversion at the output terminal, thus cannot be realized in a single chip transceiver. The PA delivers 18 dBm output power with 33% PAE at a single 1-V supply voltage. The lower efficiency is due to the experiment used power splitter and power combiner to provide differential signal and to convert back the signal to single-ended signal. The complete schematic is shown in Figure-8.

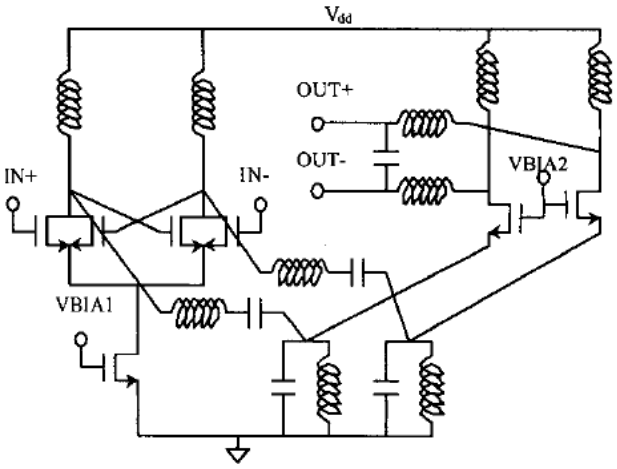


Figure-8. Complete schematic of the proposed class-E PA with positive feedback driver stage (Ka Wai Ho and Howard C. Luong, 2003).

The critical requirement in the implementation of CMOS RF class-E PAs is the need of high Q factor inductors. Therefore, the bonding wires with high Q with limited length control and more accurate length control are proposed (Tang Tat Hung and El-Gamal, M.N., 2003). The operating frequencies are centered at 1.2 GHz and 2.65 GHz with 24-26 dBm output power using mode locking techniques for both designs. However, the proposed PA requires off-chip baluns to be used at both input and output for converting signals from single-ended to differential and vice versa (Tang Tat Hung and El-Gamal, M.N., 2003). The measured PAE of the 1.2 GHz PA is 62 % while for the 2.65 GHz is 38 % when operated from a 1.7 V supply voltage. The schematic of the proposed PA is shown in Figure-9.

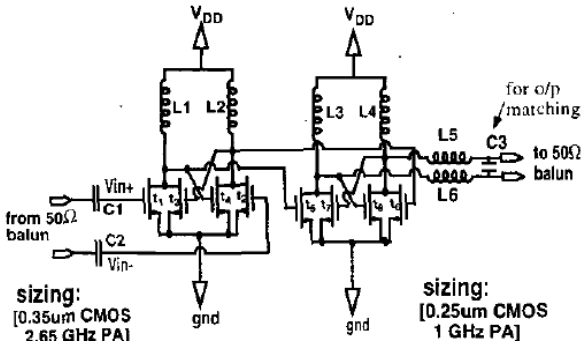


Figure-9. Complete schematic of the proposed class-E PA with positive feedback driver stage (Tang Tat Hung and El-Gamal, M.N., 2003).

An on-chip transformer-feedback topology is applied in the pre-amplifier in order to provide a high swing to drive the second stage and injection-mode-locking topology is employed in the second stage to achieve high output power and high efficiency is proposed in (Ping Song and Howard, C.L., 2005). The amplifier delivers the maximum output power of 20.3 dBm with 43% PAE at a 1.8-V supply.

In (Brama, R. *et al*., 2007), a fully differential topology with off-chip input and output baluns is proposed. The measured show that the PA can deliver 31 dBm output power with 58% PAE at 1.7 GHz. The authors further improve the proposed design by integrating the output balun on chip as published in (Riccardo Bramal *et al*., 2008). However, the experiments prove that only 30.5 dBm power is delivered with 48 % PAE at 1.6 GHz. There is no improvement in the performance of PAE even though the balun is integrated on chip. The proposed PA is shown in Figure-10.

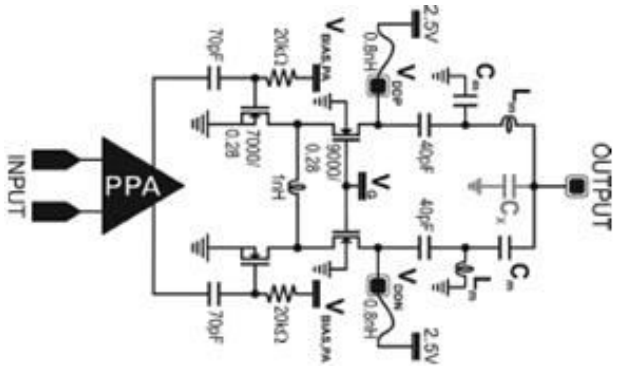


Figure-10. Schematic of the proposed single-ended output PA with on-chip embedded balun (Riccardo Bramal *et al.*, 2008).

AN *et al.* has proposed a new topology of class-E PA consists of input balun, two driver stages, a power stage and output network with a balun function. The proposed PA is targeted to obtain enough gain and power driving, as well as to provide high efficiency. The proposed schematic diagram is shown in Figure-11. The PA is implemnted in a CMOS 0.18-µm process delivers 31.2 dBm output power with 41% PAE (Kyu Hwan An *et al.*, 2008). Unfortunately, the proposed PA could not achieve high efficiency even though with a very complicated design.

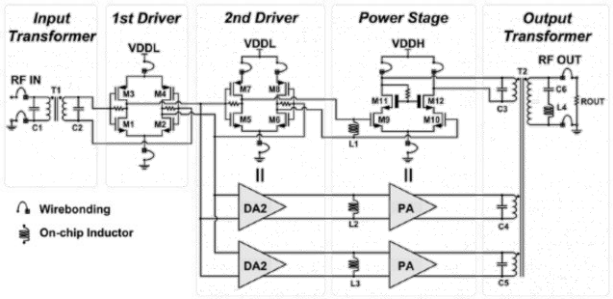


Figure-11. Schematic diagram of the proposed power combining transformer techniques for class-E PA (Kyu Hwan An *et al.*, 2008).

In (Park, C. and Seo, Cl., 2010) proposed class-E PA with additional thin film technology in a separete substrate to design the output matching network for high efficiency. The additional thin film technology is implemented in the transformer and MIM capacitor at the output network to reduce the paracitics resistance for high efficiency PA. This amplifier achieved approximately 46% of PAE with the maximum output power is 31.6 dBm at 1.8 GHz. The supply voltage is 3.3 V. The additional thin film technology contributes in increasing the chip size about 0.63 mm^2 and the total chip size for this PA is 1.17 mm^2.

The class-E PA with double-resonance circuit to reduce voltage stress and a negative capacitance is also implemented for efficiency enhancement is proposed as shown in Figure-12 (Yonghoon Song *et al.*, 2010). The proposed PA class-E is fabricated using a 0.13-µm CMOS process that delivers 31.5-dBm output power with 51% PAE at 1.8 GHz (Yonghoon Song *et al.*, 2010). Finally, the recent class-E PA is proposed in (Hyuk Su Son *et al.*, 2013). The fully integrated PA consist of consists of an input balun, a driver stage, a power stage, and two output transformers for dual-band PA operation is designed and fabricated in a 0.18-µm CMOS technology and has a chip size of 1.5 × 1.85 mm^2 including all pads. The schematic of the proposed PA is shown in Figure-12. The PA delivers the output power of 28.1/27.4 dBm with PAE of 37.8/31.6 % at 1.9 GHz and 2.6 GHz, respectively (Hyuk Su Son *et al.*, 2013).

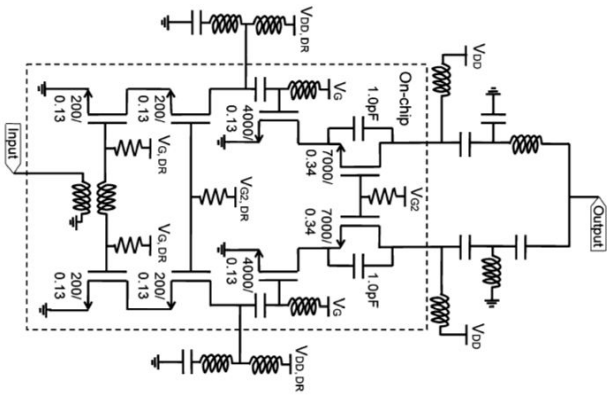


Figure-12. Schematic of the proposed class-E including driver amplifier and input balun (Yonghoon Song *et al.*, 2010).

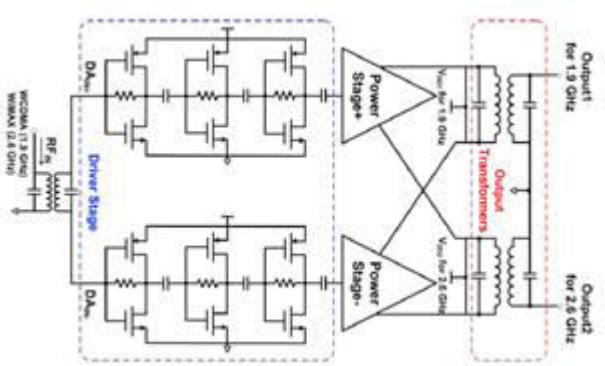


Figure-13. Schematic of the proposed class-E dual-band PA (Hyuk Su Son et. al., 2013).

Recently, in (Chenxi Zhai, Khwo-Keung M. Cheng, 2014) proposed the design of differential 1.8 GHz fully-integrated CMOS class-E PA based on transformer-based balun. The proposed design achieves 29 dBm output power and power-added efficiency of 38.7 %. In addition, a novel output circuit is developed to serve as both the power combining device as well as waveform-shaping network, which offers smaller footprint and reduced power

loss in the proposed architecture using 0.35-µm CMOS technology. Figure-14 shows the proposed design by Chenxi Zhai and Khwo-Keung M. Cheng.

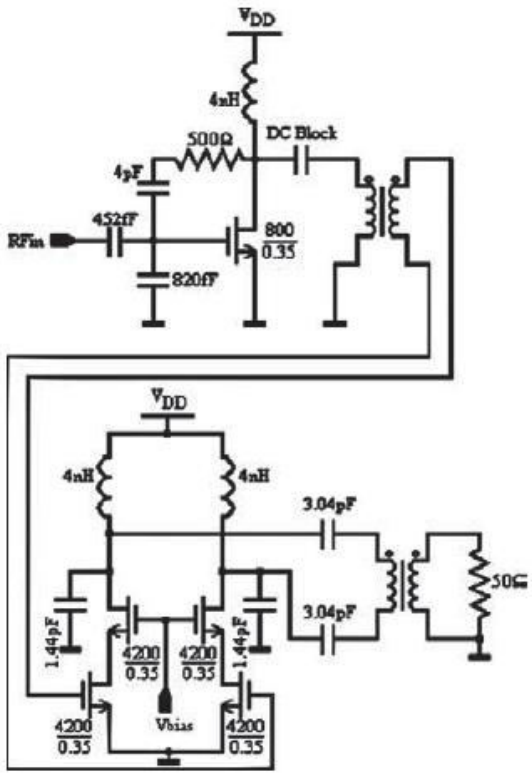


Figure-14. Differential class-E PA (Chenxi Zhai, Khwo-Keung M. Cheng, 2014).

SUMMARY OF FINDINGS

In general, the PAE of class-E PA is decreased when the frequency is increased. This is due to the increasing of parasitic losses. Most of the proposed PAs employs cascode topology in order to relax the device stress and implemented inductors by using bond wire for high Q factor, thus increase the efficiency. The transistor size in amplifier stage is made large to reduce the losses in ron resistance and the supply voltage is proportional to the output power.

The single-ended topology is the simpler circuitry of class-E PA and the higher PAE could achieve about 67 % (A. Mazzanti *et al*., 2006). However, the circuit includes off-chip components as an output matching network. A few works done on fully integrated PAs, unfortunately the PAs did not achieve more than 50 % of PAE. In contrast, the fully differential topology class-E PAs are the popular topology employed by the researchers. This topology can deliver high output power with high PAE. The higher PAE is obtained about 67 % and the higher output power can be deliver about 31.6 dBm (Riccardo Bramal *et al*., 2008, Park, C. and Seo, Cl., 2010). However, the baluns are needed in order to convert the single-ended input signal to the differential signal and vice versa for the output signal. Integrated balun on-chip contributes more losses as compare with off-chip balun (Riccardo Bramal *et al*., 2008). Therefore most of the proposed differential PAs implemented off-chip baluns (K.C. Tsai and P.R. Gray, 1999, Tang Tat Hung and El-Gamal, M.N., 2003, Ping Song and Howard, C.L., 2005, Hyuk Su Son *et al*., 2013).

CONCLUSIONS

A review of high efficiency CMOS class-E power amplifier in Gigahertz frequencies range for wireless applications has been discussed. Current published data indicates that CMOS class-E PA can obtain the highest PAE about 67 % only. The device stress, inductors losses, driver stage, and technology scaling down have been considered in designing class-E PA, however the efficiency still could not achieved as higher as theoretically efficiency of 100%. This is clearly shown from the works on the CMOS class-E PA in GHz range frequencies is hard to obtain high efficiency if the frequency is increased while the output power is limited around 1 W range only. Selection of technology seems not important as up to year 2013, the work is still employed 0.18µm CMOS process as the best choice for CMOS class-E PA. Authors believe a new approach of increasing the efficiency class-E PA could be realize in the future and the class-E still is the best choice of candidates among switching PAs especially for constant envelop modulation transceivers.

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