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PERFORMANCE ANALYSIS ON VARIOUS LOW POWER CMOS DIGITAL DESIGN TECHNIQUES

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ABSTRACT

With the advent of portable and high-density microelectronic devices, the power dissipation of very large scale integrated (VLSI) circuits is becoming a critical concern. In this paper, three low power CMOS digital design techniques have been compared in terms of their speed, power consumption and area. For comparison purposes, 1-bit full adder circuits are constructed based on each of the design technique in 0.35 µm CMOS technology using Mentor Graphics tools.

Keywords: low power, CMOS, digital design.

INTRODUCTION

As VLSI devices has grown in complexity and density as well as with the growing use of portable and wireless electronic systems, their power consumption has become a major challenge in today's VLSI circuit and system designs (Chandra and Brodersen, 1992, Meindl, 1995, Najm, 1997). These issues have forced designers to aggressively pursue low-power design methodologies.

The expression for CMOS power consumption is given by (Sakurai & Kuroda, 1997):

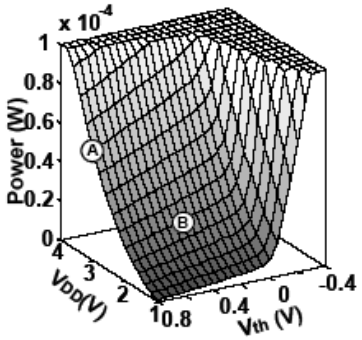
$$Power = (p_t \bullet C_L \bullet V_s \bullet V_{DD} \bullet f_{CLK}) + (I_o \bullet 10^{\frac{V_{th}}{S}} \bullet V_{DD})$$

The first term represents dynamic power dissipation due to charging and discharging of the load capacitance, where p_t is the switching probability, C_L is the load capacitive, V_s is the voltage swing of a signal and f_{CLK} is the clock frequency. The second term is the subthreshold leak term and S is typically about 100mV/decade.

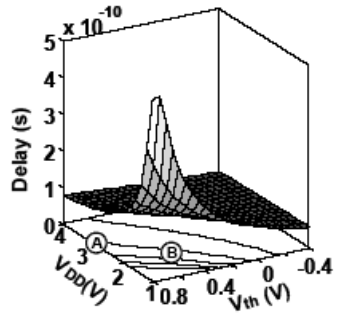
Figure-1 shows the plot for power and delay based on 0.5 µm technology (Sakurai andKuroda, 1997). As seen from the figure, lowering the V_{DD} could achieve low power system but the delay might increases. To reduce this undesirable effect, threshold voltages also need to be lowered. However, lowering threshold voltages may increase the subthreshold leakage power dissipation. In order to overcome the problem, there are many techniques have been proposed for controlling the threshold voltages (Wei and Vivek, 2000, Mohab and Elmasry, 2003, Inukai and Sakurai, 2001, Aswale and Chopade, 2013, Sangwan and Kedia, 2013).

In this paper, the experimental results of three different low power CMOS digital design techniques were discussed in terms of their speed, power consumption and area. We have tested the system on the 1-bit full adder benchmark circuit.

The paper divided into 4 sections. In the following section (Section 2), we present the low power CMOS design methodologies. In Section 3, the experimental results are discussed. Discussion and conclusion are presented in Section 4.



(a)



(b)

Figure-1. (a) Power dependence on V_{th} and V_{DD} (b) Delay dependence on V_{th} and V_{DD}.

LOW POWER CMOS DESIGN TECHNIQUES

Since dynamic power is approximately proportional to the square of supply voltage and static power is proportional to V_{DD}, lowering supply voltage is obviously the most effective way to reduce power consumption. Threshold voltage is also one of the most important parameters in technology and circuit design.

Since the propagation delay decreases with the reduction of threshold voltage, the transistor threshold voltage should also be scaled in order to satisfy the performance requirements. At present, there are several multiple thresholds CMOS design techniques have been developed.

Multi-threshold voltage CMOS (MTCMOS)

MTCMOS circuit was proposed by inserting high threshold devices in series to low- V_{th} circuitry (Mutoh *et al.*, 1995). Commonly, high V_{th} devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. In fact, through utilizing high V_{th} devices, it can actually reduce static leakage by 10 times compared with low V_{th} devices.

Figure-2 shows the schematic of 1-bit full adder MTCMOS circuit. A sleep control scheme is introduced for efficient power management. During active mode, SL is set to 'low' and sleep control transistors (MP and MN) are turned on. Since their on-resistances are small, the virtual supply voltages (V_{DDV} and V_{SSV}) almost function as real power lines. In the standby mode, SL is set to 'high' and MN and MP will be turned off thus the leakage current is low.

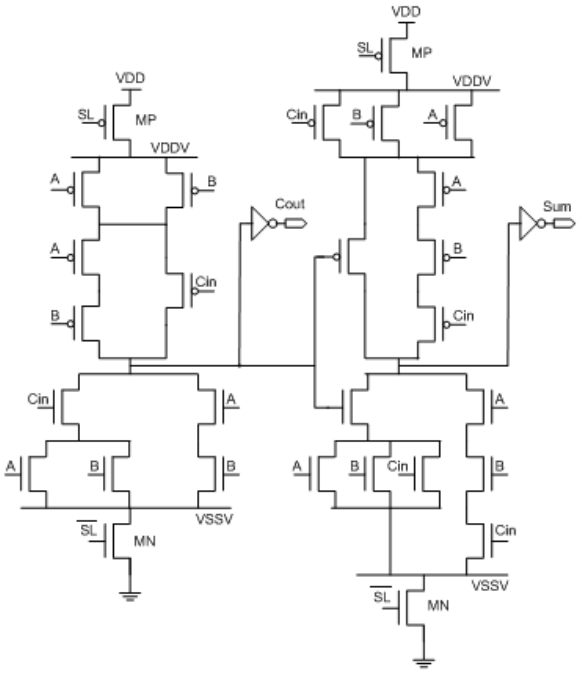


Figure-2. 1-bit full adder MTCMOS circuit.

Variable threshold CMOS (VTCMOS)

VTCMOS is a body-biasing design technique (Kuroda *et al.*, 1996). In the VTCMOS scheme, V_{th} is controlled by substrate bias using the body effect. V_{th} is set to a high value in the stand-by mode and is set to a low value in the active mode to attain high speed and low stand-by power at the same time.

Figure-3 shows the 1-bit full adder VTCMOS scheme. In order to achieve different threshold voltages, a self-substrate bias circuit is used to control the body bias. During active mode, a nearly zero body bias is applied. While in standby mode, a deeper reverse body bias is applied to increase threshold voltage and cut off leakage current. This scheme has been used in two dimensional discrete cosine transform core processor [9]. Furthermore, in active mode, a slightly forward substrate bias can be used to increase the circuit speed while reducing short channel effect.

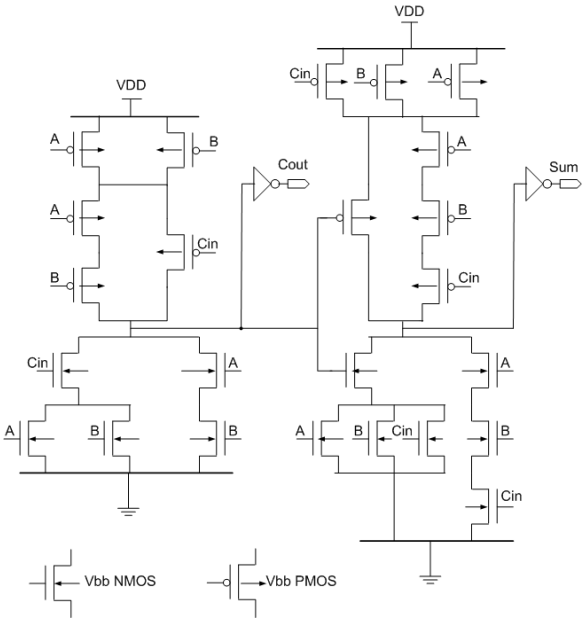


Figure-3. 1-bit full adder VTCMOS circuit.

Super cut-off CMOS (SCCMOS)

Instead of using high V_{th} sleep control transistors as MTCMOS, SCCMOS circuit uses low- V_{th} transistors with an inserted gate bias generator (Kawaguchi *et al.*, 2000). SCCMOS technique capable to reduce the leakage whilst increase the overall performance. In addition, it can't save the circuit logic state during standby mode; hence the technique results in destruction of circuit logic state.

Figure-4 shows the 1-bit full adder SCCMOS circuit using PMOS insertion transistor. In the active mode, the gate is applied to 0V (V_{DD}) and the virtual V_{DD} line is connected to supply V_{DD}. In the standby mode, the gate is applied to V_{DD}+0.4V to fully cut off the leakage current. Compared to MTCMOS, SCCMOS circuits can operate at low power supply voltages.

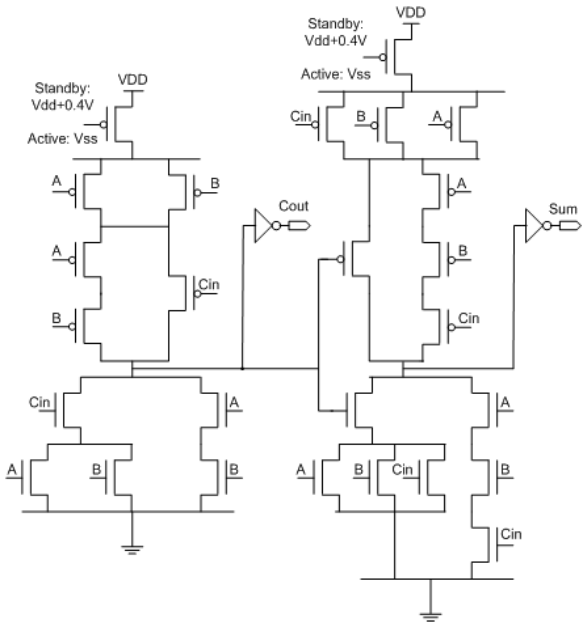


Figure-4. 1-bit full adder SCCMOS circuit.

Experimental results

Several metrics are available for comparative analysis of digital circuits. For example, power consumption, delay or speed, power delay product and circuit area. In this paper, we are primarily interested in analyzing the circuit in terms of their dynamic power consumption, speed as well as area.

Table-1 depicts some of the simulation parameters. For this study, Mentor Graphics CAD tool (Design Architect) and TSMC 0.35 µm CMOS technology are used in designing the circuit. There are three different number of supply voltages are inserted: *V_{DD}=3V, 2.5V and 2.0V*. All simulations are carried out at room temperature (25° C), during active and inactive mode with the switching activity set for the most critical condition (A = '1', B = '1', C_{in} = '1').

Table-2 shows the dynamic power consumption versus NMOS and PMOS body-biasing voltages which based on three different power supplies in the active and inactive mode. The speed and area of the system based on three different techniques as mentioned in section 2 is shown in Table-3.

DISCUSSIONS

With various setting on body bias voltage and power supply, MTCMOS technique consumes the most data power in this study during active mode. However, in the inactive mode, MTCMOS sleep transistors technique capable to reduce the standby power efficiently due to during this mode, it will cause the virtual ground line to float and so limit the leakage current to that sleep transistor. Although this technique can be easily implemented on existing circuits, it has low performance and requires additional area due to the large inserted MOSFETs.

Despite of having a bit more power dissipation during inactive mode comparing to the others, VTCMOS found to be the most power efficient in the active mode. Its superior low power performance is mainly due to ability for dynamically varies V_{th} through substrate bias, V_{bb}. Typically; V_{bb} is controlled so as to compensate V_{th} fluctuations in the active mode hence reduces power consumption in the circuit. Furthermore, it has greater performance and requires fewer transistors.

SCCMOS tends to be the best solution for today's low power applications. By over-driving the MOS gate in a standby mode, it is possible to completely cut off the leakage current of insertion transistor thus decreases power dissipation in the circuit. Its performance does not also degrading tremendously when the supply voltage scaled down from 3V to 2V. Even though it has two extra transistors compared to VTCMOS, SCCMOS circuits already proven can work at lower supply voltages (Kawaguchi *et al*., 2000).

Table-1. CMOS simulation parameters.

CAD tools	:	Mentor Graphics (Design Architect)
CMOS technology	:	TSMC 0.35 µm
MOSFET model	:	BSIM3 Level 51
Power supply voltage	:	3.0V, 2.5V, 2.0V
Temperature	:	25° C
Data activity	:	A = '1', B = '1', C_{in} = '1'

Table-2. Power consumption dependence on body-biasing voltages

Power supply	Vbb PMOS	Vbb NMOS	Power Consumption (nW)		
			MTCMOS	VTCMOS	SCCMOS
3V	2.8	0.2	4.150	4.003	4.141
	2.9	0.1	1.469	1.466	1.469
	3.0	0	0.891	0.891	0.891
	3.1	-0.1	0.116	0.563	0.224
	3.2	-0.2	0.115	0.383	0.237
2.5V	2.3	0.2	3.312	3.189	3.303
	2.4	0.1	1.122	1.119	1.122
	2.5	0	0.675	0.675	0.675
	2.6	-0.1	0.089	0.425	0.156
	2.7	-0.2	0.088	0.288	0.146
2V	1.8	0.2	0.816	0.810	0.814
	1.9	0.1	0.816	0.814	0.816
	2.0	0	0.487	0.487	0.487
	2.1	-0.1	0.065	0.305	0.108
	2.2	-0.2	0.064	0.206	0.166

Table-3. Speed and area dependence on supply voltage.

Design technique	Speed (GHz)			Area (in number of transistors)
	Vdd = 3V	Vdd = 2.5V	Vdd = 2V	
MTCMOS	1.43	1.33	1.18	32
VTCMOS	2	1.81	1.54	28
SCCMOS	1.92	1.85	1.67	30

CONCLUSIONS

Three low power CMOS digital design have been analysed and compared in terms of speed, area and power consumption. The results show that MTCMOS is conceptually simple and easy to implement and VTCMOS is better performance-wise. However, SCCMOS has been shown to operate the most efficiently at low supply voltage hence recommended to be applied for low power low voltage circuits.

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