



EFFECT OF BULK DOPING LEVEL AND WAFER THICKNESS ON THE PERFORMANCE OF MONOCRYSTALLINE SILICON SOLAR CELL

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ABSTRACT

Focus of solar cell industry is to reduce production cost as much as possible while maintaining solar cell performance at a desirable level. The largest share of solar cell production cost comes from wafer price. Currently wafer-based solar cell uses about 300 μm wafer thickness for its daily production. It is therefore very important to reduce wafer thickness as part of effort to reduce production cost of solar cell. This research is focused to examine the effect of bulk doping level and wafer thickness reduction on the performance of wafer-based silicon solar cell. Research was performed by simulating the effect of bulk doping level and wafer thickness on the output parameters of solar cell. Optimization was done on phosphor emitter doping level of $7.50 \times 10^{18}/\text{cm}^3$, junction depth of 1.56 μm , cell surface area of 1 cm^2 and illuminated under AM1.5G spectrum with the intensity of 100 mW/cm^2 .

Simulation result showed that solar cell with efficiency between 18.15-18.7% was achieved by using wafer thickness between 300 and 320 μm and boron doping level (bulk doping level) between $1.84 \times 10^{17} - 2.68 \times 10^{17}/\text{cm}^3$. On this condition solar cell had short circuit current density, J_{SC} of 0.32 A/cm^2 , open circuit voltage, V_{OC} of 0.70 V, maximum output power, P_{MAX} of 0.0182 W/ cm^2 , and fill factor, FF of 0.829.

Keywords: monocrystalline solar cell, wafer thickness, bulk doping level.

INTRODUCTION

Solar cell is a device that converts sunlight into electricity. Currently the majority of solar cell productions come from wafer-based silicon solar cell [1]. Despite its price that is higher than the other technologies such as thin film or amorphous solar cell, wafer-based solar cell offers advantages than its competitor such as higher efficiency. In wafer-based monocrystalline silicon solar cell, its laboratory efficiency has reached above 20% while its commercial efficiency is between 15 and 17% [2].

Despite offers virtually no limit in the term of its energy sources, solar cell still has to compete with the other renewable energy sources such as wind power, hydro power, or geothermal power. In order to be competitive, solar cell price should be lower than its current level. Currently almost 40% of solar cell production cost comes from wafer price [3]. Therefore wafer thickness reduction offers solution to decrease production cost.

Reduction on wafer thickness will reduce recombination sites, however it will also decrease the probability of minority carriers production. Generally, solar cell efficiency will not being affected by wafer thickness if the thickness is above 200 μm [4]. Solar cell efficiency could be increased by some methods such as adding back surface field (BSF) on the rear surface of the cell to reduce surface recombination velocity [5,6], produces anti reflection coating (ARC) on the front surface [7], and textures the surface to enhance light trapping process [8,9].

Bulk doping level is a parameter that affects bulk recombination on wafer-based solar cell. The value of bulk doping level will control minority carrier lifetime. Finding optimum bulk doping level and wafer thickness are therefore very essential to increase cell efficiency. This research is intended to find optimal bulk doping level and

wafer thickness. The optimization process will be done on p-type monocrystalline silicon wafer. This wafer has refractive index and reflectance of 2.1 and 3%, respectively. Emitter layer has phosphor concentration of $7.50 \times 10^{18}/\text{cm}^3$ with junction depth of 1.56 μm . The surface of wafer is kept flat and is coated with anti-reflection coating. Test of the solar cell will be performed using AM1.5G spectrum.

THEORY

One of key parameters of solar cell performance is short circuit current (I_{SC}). The value of I_{SC} will be affected by junction depth. To find best junction depth for certain solar cell, minority carrier lifetime should be considered. For semiconductor wafer with minority carrier diffusivity D_e and minority carrier lifetime τ_e , junction depth should not exceed minority carrier diffusion length L_e . Diffusion length L_e could be expressed as

$$L_e = \sqrt{D_e \tau_e} \quad (1)$$

In general, τ_e will decrease as the value of doping concentration increases. There are three mechanisms that produce decrease in τ_e i.e. radiative recombination, Shockley-Reed-Hall (SRH) recombination, and Auger recombination. Radiative recombination is the most basic recombination process. When electron and hole recombine, energy is released in the form of radiation. Radiative recombination lifetime, τ_{nr} for minority carrier in semiconductor wafer with acceptor doping concentration N_A and radiative recombination constant B is given by



$$\tau_{nR} = \frac{1}{2BN_A} \quad (2)$$

When semiconductor wafer has higher doping level, there is a possibility that minority carrier will recombine through mechanism that is known as Auger recombination. For semiconductor wafer with acceptor doping level N_A , auger recombination lifetime τ_{nA} , will be given by

$$\tau_{nA} = \frac{1}{DN_A^2} \quad (3)$$

If defects present in semiconductor wafer in significant amount, another recombination events might occurs via defect sites because defect sites could act as trapping sites for minority carriers. This type of recombination process is known as Shockley-Reed-Hall (SRH) recombination. Minority carrier lifetime for this type of recombination process, τ_{nT} , is given by

$$\tau_{nT} = \tau_{n0} \left(1 + \frac{m_1}{N_A} \right) \quad (4)$$

If all recombination processes are considered, then total minority carrier lifetime, τ_n could be given by

$$\frac{1}{\tau_n} = \frac{1}{\tau_{nT}} + \frac{1}{\tau_{nA}} + \frac{1}{\tau_{nR}} \quad (5)$$

Equations 2, 3, and 4 show that acceptor doping concentration, N_A will affect minority carrier lifetime. From those equations it is understandable that an increase on N_A will reduce minority carrier lifetime. Direct effect of reduction on minority carrier lifetime is a decrease on short circuit current I_{SC} .

Another parameter that becomes performance indicator of solar cell is open circuit voltage, V_{OC} . The value of V_{OC} depends on saturation current I_0 , photogenerated current I_L , and ambient temperature T , as given by following equation.

$$V_{OC} = \frac{kT}{q} \ln \left(\frac{I_L}{I_0} + 1 \right) \quad (6)$$

Equation 6 shows that in order to increase V_{OC} the value of I_0 should be lowered. To reduce I_0 , it is necessary to understand factors that affect the value of I_0 . Equation 7 shows that I_0 will depend on diffusivity, diffusion length, doping concentration of both electron and hole, and intrinsic concentration of semiconductor.

$$I_0 = qA \left(\frac{D_e n_i^2}{L_e N_A} + \frac{D_h n_i^2}{L_h N_D} \right) \quad (7)$$

From equation 7 it can be shown that reduction on I_0 will happen if N_A and N_D is as higher as possible. If

solar cell is made from wafer that has background doping N_A , emitter layer will have doping concentration of N_D . For highly doped emitter layer, or $N_D \gg N_A$, then it could be concluded that approximately I_0 will only depend on N_A .

By examining and comparing equations 2, 3, 4, 6, and 7 a pattern could be drawn. According to equations 2,3, and 4 an increase on I_{SC} will happen if minority carrier lifetime also increases, and this could be done by reducing N_A . On the other hand, equation 6 requires that V_{OC} could be increased by reducing I_0 . Meanwhile, equation 7 shows that reducing I_0 could be done by lowering N_A . From this situation, it could be seen that design requirement to have higher I_{SC} and V_{OC} has opposite behaviour. Therefore a trade-off mechanism is required to find acceptable value for both I_{SC} and V_{OC} .

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METHODOLOGY

Optimization process will be performed by simulation using PC1D software. In this software, all necessary solar cell properties and geometry are set to replicate real solar cell that will be produced. Comparison between simulation result and real solar cell test could be used to find correction factor to improve next simulation.

This simulation uses p-type monocrystalline silicon wafer and n-type phosphor-doped emitter layer. Initial design parameter could shown on Table 1. These parameters will be kept constant during the simulation process. Output of solar cell will be optimized by varying bulk doping level and wafer thickness. Bulk doping level and wafer thickness will be varied according to the range as follows:

1. Boron concentration is varied from $1 \times 10^{14}/\text{cm}^3$ to $1 \times 10^{18}/\text{cm}^3$
2. Wafer thickness is varied from 100 μm to 320 μm

Analysis will be focused to examine the effect of boron concentration and wafer thickness on the performance of solar cell. Output variable such as short circuit current density, J_{SC} , open circuit voltage, V_{OC} , maximum output power, P_{MAX} , fill factor, FF , and efficiency, η . Analysis on solar cell structure will be



stressed on recombination rate distribution as function of position and boron concentration. By describing the relation between variables aforementioned above, it could be expected that optimum bulk doping level could be found and minimum recombination rate could be reached and finally optimum solar cell performance could be achieved.

Table-1. Initial parameter for optimization.

Parameter	Value	Unit
Light spectrum AM1.5G	100	mW/cm ²
Cell area	1	cm ²
Junction depth	1,56	μm
Emitter doping (phosphor concentration)	7.5×10^{18}	cm ⁻³
Net Low Level Injection (LLI) Front Surface	100	cm/sec
Net Low Level Injection (LLI) Rear Surface	10^5	cm/sec
Net LLI elektron and hole Base	51	μsec
Top Surface Broadband Reflectance	3	%
Inner Layer Optical Coating	90	nm
Refractive index	2.1	-
Series Resistance Emitter	0.3	Ω.cm ²
Series Resistance Base	0.1	Ω.cm ²

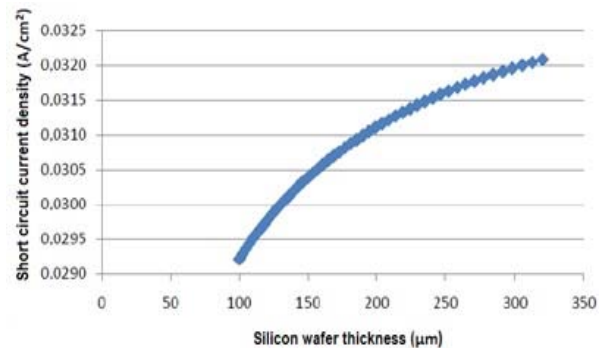
RESULTS AND DISCUSSION

a) Effect of wafer thickness on short circuit current density and open circuit voltage

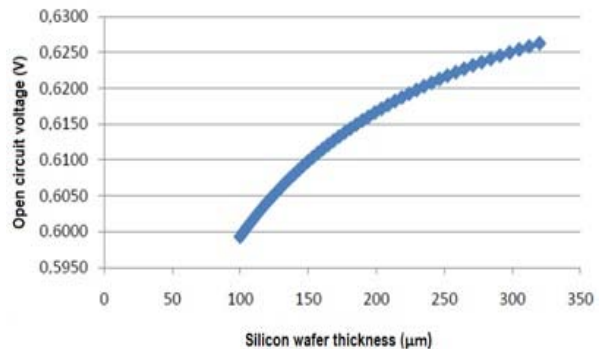
Figure-1 showed effect of wafer thickness on short circuit current density and open circuit voltage at boron doping level of $1.5 \times 10^{16}/\text{cm}^3$. Simulation results showed that short circuit current density and open circuit voltage showed an increase within the range of 0.0292 – 0.0321 A/cm² and 0.5993 – 0.6263 V, respectively. An increase on short circuit current density and open circuit voltage has been achieved for wafer thickness from 100 to 320 μm. Increasing wafer thickness will enhance the interaction probability between photon and solar cell. Larger interaction probability will produce more electron-hole as far as photon energy is higher than energy gap of semiconductor. However due to the exponential nature of photon absorption, any increase on thickness of more than 300 μm will give insignificant number of photon absorption and short circuit current production. Moreover, nominal wafer thickness that is used in solar cell

production is around 300 μm, and after chemical process such as etching, the thickness of the wafer will be reduced a few microns to discard dangling bond on the surface of the wafer.

Figure-2 showed cumulative electron-hole generation for bulk doping concentration range between $2.02 \times 10^{17}/\text{cm}^3$ and $2.15 \times 10^{16}/\text{cm}^3$. An increase on electron-hole pair will enhance collection probability of the solar cell. As the result, short circuit current density will also increase.



(a)



(b)

Figure-1. Effect of wafer thickness on short circuit current density (a) and open circuit voltage (b) both at boron doping concentration of $1.5 \times 10^{16}/\text{cm}^3$.

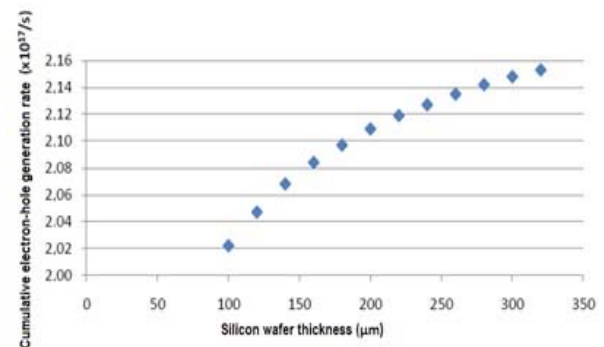


Figure-2. Effect of wafer thickness on cumulative electron-hole generation rate



b) Effect of boron doping level on short current density and open circuit voltage

Figure-3 showed effect of boron concentration on short circuit current density and open circuit voltage for solar cell with 300 μm thickness. From Figure-3, it can be seen that an increase on boron concentration reduced short circuit current density within the range of 0.0338 – 0.0294 A/cm^2 . Furthermore, open circuit voltage showed an increase between 0.4743 and 0.6991 V as boron doping level increased. Open circuit voltage began to decrease when boron doping concentration is above $4.80 \times 10^{17}/\text{cm}^3$.

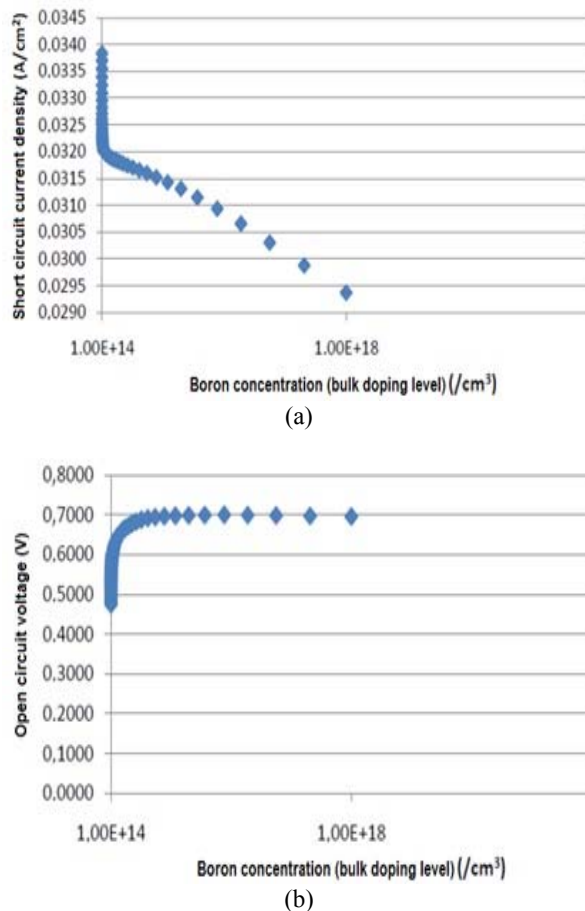


Figure-3. Effect of boron doping level on short current density (a) and open circuit voltage (b) for wafer thickness of 300 μm .

Higher boron doping level will increase recombination process through Auger recombination mechanism. This fact could be shown on Figure-4 where higher boron doping concentration within silicon wafer increased cumulative recombination rate.

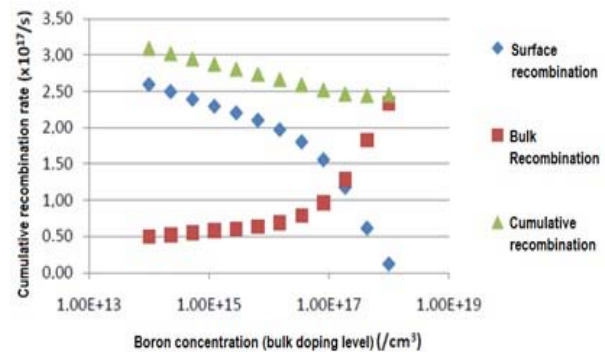


Figure-4. Effect of boron concentration (bulk doping level) on cumulative recombination rate for silicon wafer of 300 μm thickness

On the other hand, when boron concentration was increased, open circuit voltage increased. This condition was well predicted by equations 6 and 7 that showed an increase on N_A will reduce I_0 and finally increases V_{OC} .

c) Effect of silicon wafer thickness and boron doping level on solar cell efficiency

Figure-5 showed effect of wafer thickness and boron concentration on solar cell efficiency. The optimum efficiency that could be achieved was between 18.15 and 18.24% if wafer thickness was between 300 and 320 μm and boron doping level was set between 1.84×10^{17} – $2.68 \times 10^{17}/\text{cm}^3$. When optimum efficiency was reached, short circuit current density had value between 0.0314 and 0.0317 A/cm^2 , open circuit voltage was within 0.6936 – 0.6977 V, maximum output power was 0.0182 W/cm^2 , and fill factor was in the range of 0.828 – 0.829.

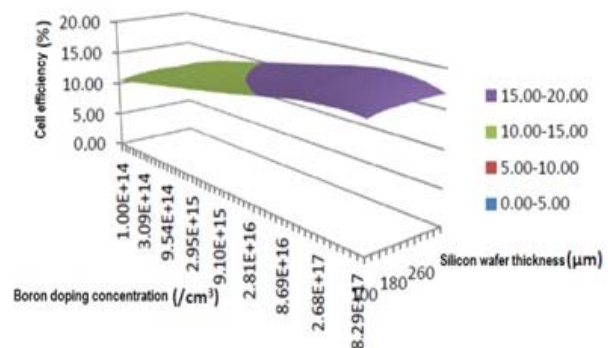


Figure-5. Effect of boron doping concentration and silicon wafer thickness on solar cell efficiency.

d) Optimum solar cell design

Characteristic curve (I-V and P-V curve) for optimum solar cell design was shown on Figure 6. In this design, wafer thickness and boron doping level were 300 μm and $1.84 \times 10^{17}/\text{cm}^3$, respectively.

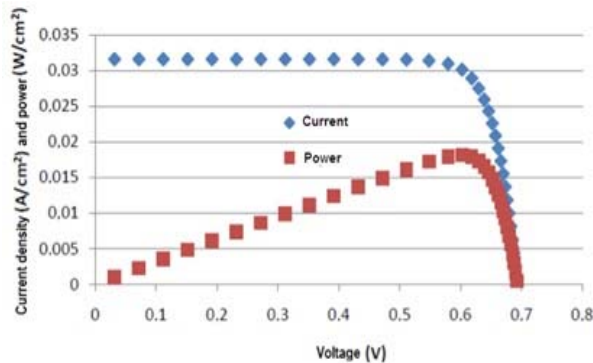


Figure-6. Characteristic curve for optimum solar cell design

From I-V and P-V curve in Figure-6, it can be seen that open circuit voltage (V_{OC}), short circuit current density (J_{SC}), fill factor (FF), and efficiency (η) for optimum solar cell design were 0.6936 V, 0.0316 A/cm², 0.828, and 18%, respectively. Maximum output power (P_{MAX}) would be 0.0182 W/cm². This result is fairly reasonable since there are still some variables that have not been yet optimized such as applying selective emitter, surface texturing and surface passivation. According to the simulation result above, it can be demonstrated that simple solar cell design has potency to reach high efficiency as long as optimum design variables is applied.

CONCLUSIONS

In this study, we examined the effect of bulk doping level and wafer thickness reduction on the performance of wafer-based silicon solar cell. Simulation results showed the dependency of short circuit current density, open circuit voltage, and maximum output power on wafer thickness and boron doping level. In general, thicker wafer and higher boron doping level (bulk doping level) will give higher fill factor and efficiency. Solar cell with efficiency between 18.15 and 18.24% could be produced using 300 – 320 μm wafer thickness and boron concentration from 1.84×10^{17} to $2.68 \times 10^{17}/\text{cm}^3$. This solar cell had efficiency of 18.15 – 18.24%, open circuit voltage between 0.6936 and 0.6977 V, maximum output power 0.0182 W/cm², and fill factor between 0.828 and 0.829.

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