



## HALL INTEGRATED PLATE RESEARCH AND SIMULATION

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### ABSTRACT

The article analyzes an opportunity of the rectangular form Hall plates' application, formed within the CMOS XFB process with the XT018  $\mu\text{m}$  design rules as a part of IC with linear output. The Hall plate simulation in TCAD was carried to optimize the design and size. It is shown that the Hall plate width W and length L balance is within  $1.25 \frac{W}{L} < 1.5$ . The Hall plate simple model was offered and the formula for Hall voltage was developed, explaining the Hall voltage saturation phenomenon with ratio  $W/L > 1.5$ .

**Keywords:** Hall plate, CMOS process, magnetic field, Hall voltage, drain current, carrier mobility, geometrical coefficient, Hall plate model

### INTRODUCTION

Physical quantities sensors such as temperature, pressure, acceleration, angle (of slope), rotation sensors have widely spread in modern microelectronics. Magnetic fields sensors are the most important ones.

Magnetic field sensing element is the main plate of objects and devices, using the magnetic field. Any magnetosensitive plate, transforming magnetic field action to an output electrical signal, can act as magnetic field sensing element. The most well-known magnetic field sensing elements are discrete and integrated Hall plates. As a rule, integrated Hall plates contain signal gain circuits.

Ratiometric circuits with linear output, in which Hall voltage changes proportionally with strength of the magnetic field, are used to measure relatively small changes of magnetic field. Ratiometric circuit's output voltage without magnetic field, taken for the reference level, is usually equal to the half of the supply voltage. The output voltage is higher than reference level when positive direction of the magnetic field is detected, if the

negative one is detected – the voltage is lower, although it remains positive quantity [1].

Hall plate can be realized in standard IC manufacture processes such as bipolar or CMOS processes. Hall plates, based on CMOS, have high reliability, small size, low cost and are compatible with other CMOS plates [2-5]. CMOS-compatible Hall plates are usually formed in n-type well.

The article provides the research results of the Hall plates' application opportunity, formed within the CMOS XFB process with the XT018  $\mu\text{m}$  HV SOI CMOS design rules as a part of IC with linear output. Hall plate is actually a field transistor, otherwise pinch-resistor, doubly bounded by p-n junction. Such structure is the most cumulative radiation doze hardened, i.e. it does not contact any oxide side and that's why it is not affected by stored charge in the oxide.

### MAIN PART

Magnetic field range, effecting the Hall plates is from -640 to 640Gs. Table 1 contains the Hall plate's structure characteristics.

**Table-1.** Hall plate structure parameters

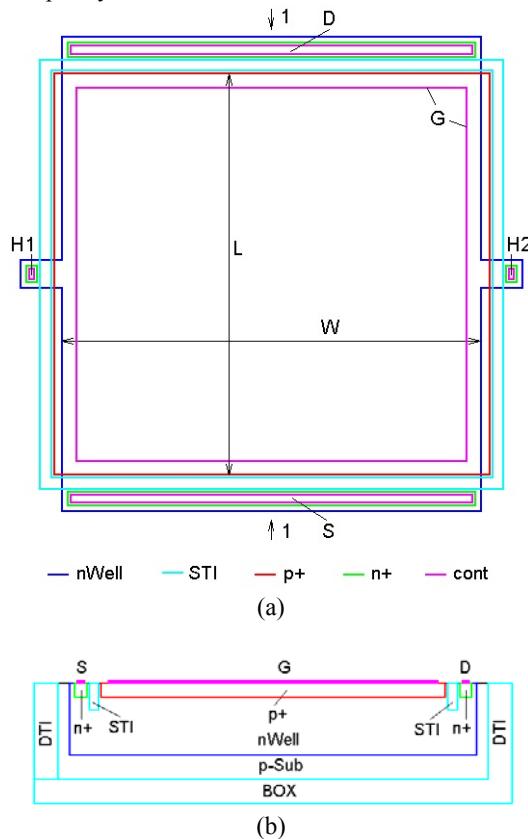
Layer	Sheet resistance $R_s$ , Ohm/sq. (electrical resistivity $\rho$ , Ohm·cm for a substrate)	Depth $x_j$ , $\mu\text{m}$
p-Sub(a substrate)	100	
nWell	1080 (under STI)	1.5
p <sup>+</sup>	135	0.2
n <sup>+</sup>	62	0.2
STI		0.4

Figure-1(a) shows the Hall plate schematic layout, figure 1.b shows Hall plate's structure in cross-section 1. L and W are Hall plate's length and width respectively (actually

channel's length and width), S – source, D –drain, G- gate, H1 and H2 – Hall contacts, STI, DTI and BOX – dielectric



insular layers. Layout does not show DTI and BOX layers for simplicity.



**Figure-1.** Hall plate layout (a) and structure (b)

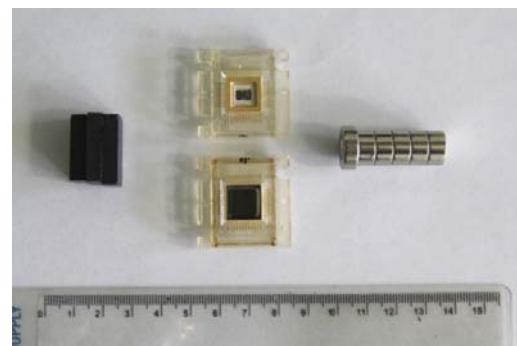
Several test Hall plates were manufactured at one die. Among them there are the following options:

- 1<sup>st</sup> option – continuous full width contacts to source and drain (see Fig. 1);
- 2<sup>nd</sup> option – continuous contact full width to source and 5 contacts to drain, situated at equal distance from each other along the structure;
- 3<sup>rd</sup> option – 2 contacts to source situated at the corners of the source and 4 contacts to drain at equal distance from each other along the structure;

For all options Hall plate's length  $L=500\mu\text{m}$ ,  $W=500\mu\text{m}$ .

The die with Hall test plate is packaged in 42-pincase H14.42-1B. Connection device UK-42-4C, electronic commutator 64x8, voltage supply KEITLEY-2420, multimeter KEITLEY-2000, ferrite and neodymium magnets were used when analyzing test Hall plates.

Electrical mode in the course of Hall plates'' analyzing: source S – grounded, gate G – grounded, 5V voltage was applied to all drains D. The voltage was measured at H1 and H2 outputs (voltmeter's +) without magnetic field VH0 and with magnetic field VHM and current from power supply (drain current ID). The difference VHM – VH0 = VH was calculated that is the real Hall voltage value, conditioned by magnetic field effect. The Hall plate in case without a lid and neodymium magnets were used to obtain maximum Hall voltage value at room temperature. Figures 2 and 3 show Hall plates' photographs in case with and without cover as well as ferrite and neodymium magnets and a work place for Hall plates' analysis.



**Figure-2.** The Hall plates' photograph in case with and without a lid.



**Figure-3.** The photography of the work place for Hall plates' analysis.

## RESULTS OF RESEARCHES

Table 2 contains Hall plates measurement results for options 1, 2 and 3, on exposure to magnetic field 640GS and at room temperature.



**Table-2.** Hall plates measurement results for options 1, 2 and 3, on exposure to magnetic field 640GS and at room temperature.

Option	$I_D$ , mA	$V_{HO}$ , mV	$V_{HM}$ , mV	$V_H$ , mV
1	6.9	-8.0	-21.3	-13.3
2	5.4	-9.0	-20.7	-11.7
3	2.4	-5.5	-11.7	-6.2

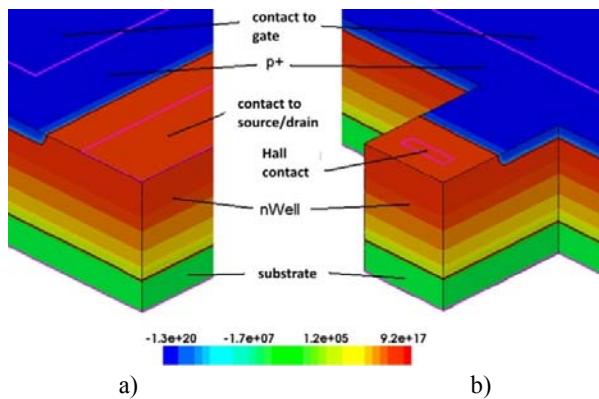
As the Table 2 shows, maximum Hall voltage is for the 1st option. That's why further research and optimization were carried out for this option. Simulation in TCAD was carried to optimize Hall plate's geometry. For simplicity, N+ layers around contacts to source, drain and Hall contacts were not created in Hall plate's model, as far as contact resistance may be set to any value. Dielectric insular layers STI, DTI and BOX were not created as well.

As far as XT018 process documentation contains an information concerning the nWell layer under STI surface resistance (see Table 1), it is necessary to define surface impurity density in nWell layer. Equality of drain current to values specified in the table 2 (for the 2st option  $ID = 6.9$  mA) was used as a criterion. The simulation showed, that such drain current value is provided if the value of surface impurity density in nWell layer is  $NS = 9.2 \cdot 10^{17} \text{ cm}^{-3}$ .

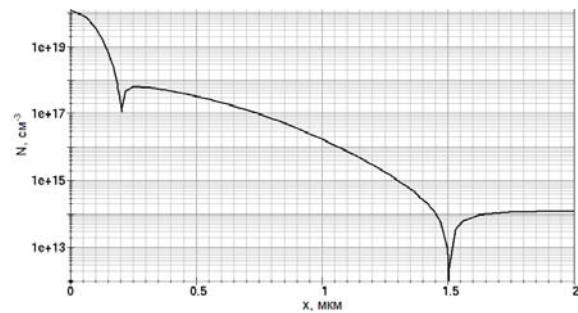
**Table-3.** Simulated Hall plate's structure characteristics

Layer	Surface impurity density $N_S$ , $\text{cm}^{-3}$ (impurity concentration $N$ , $\text{cm}^{-3}$ for a substrate)	depth $x_j$ , mm
p-Sub (a substrate)	$1.3 \cdot 10^{14}$	
nWell	$9.2 \cdot 10^{17}$	1.5 mm
p+	$1.3 \cdot 10^{20}$	0.2 mm

Figure 4a shows a part of three dimensional Hall plate's structure on the contacts to source/drain side, 4b on the Hall contacts side. Figure 5 shows impurity concentration profile in simulation Hall plate's structure



**Figure-4.** A part of three dimensional Hall plate's structure from the contacts to source/drain side, 4b from the Hall contacts side



**Figure-5.** Impurity concentration profile in simulation Hall plate's structure

When simulating, one should take into account the following physical effects:

- Silicon band gap narrowing with doping impurity concentration growth;
- Phonon and impurity ions carrier scattering, and large fields saturation of carrier drift velocity;
- Shockley-Reed-Hall recombination when excess charge carrier lifetime depends on doping impurity concentration, as well as Auger recombination.

These effects' detailed description is set in [6]



Hall voltage VH simulation results under the magnetic field influence with 640 Gs induction and voltage between source and drain VD = 5 are set in the

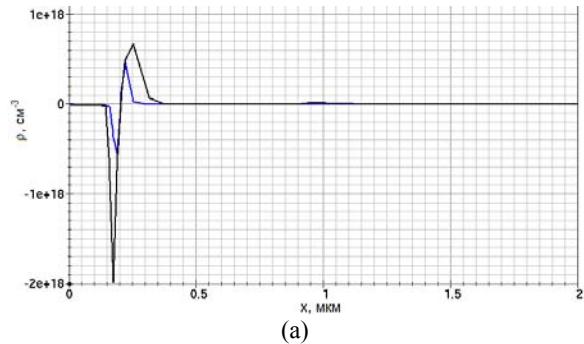
Table-4, for convenience in comparison with the measurement results for the 1st option at L = W = 500  $\mu\text{m}$ .

**Table-4.** Voltage VH simulation results under the magnetic field influence with 640 Gs induction and voltage between source and drain VD = 5

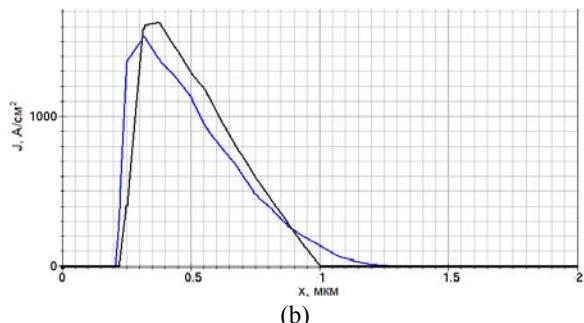
Option	Measurement		Simulation	
	$I_D$ , mA	$V_H$ , mV	$I_D$ , mA	$V_H$ , mV
1	6.9	-13.3	7.0	-13.5

As the Table shows, simulation results conform well to the experimental measurements results.

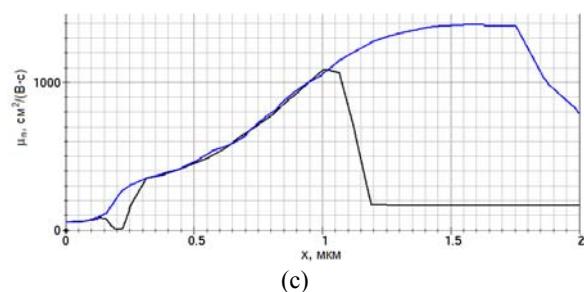
Figure-6 below shows space-charge region diagram (a), current density (b) and electron mobility (c) along Hall plate's width on the source side (black diagrams) and on the drain side (blue diagrams).



(a)



(b)



(c)

**Figure-6.** Space-charge region diagrams (a), current density (b) and electron mobility (c) along Hall plate's width on the source and drain sides.

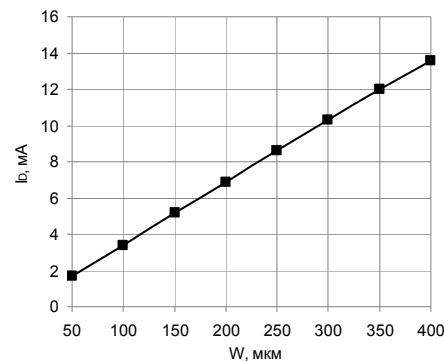
As Figure-6(a) shows space-charge region (SCR) width in junction nWell – p+ layer from the drain side is 0.16  $\mu\text{m}$ , from the source side is 0.08  $\mu\text{m}$ . SCR width in junction nWell – substrate from the drain side is 0.5  $\mu\text{m}$ , from the source side is 0.3  $\mu\text{m}$ . thus, effective channel width from the drain side is 0.64  $\mu\text{m}$ , from the source 0.92  $\mu\text{m}$ .

As Figure-6(b) shows, maximum current density is reached on the drain side under SCR of nWell – p+ junction and it is 1620  $\text{A}/\text{cm}^2$ . To the nWell- substrate junction direction – current density substrate is almost linearly decreasing. On the source side, under the SCR of nWell – p+ junction maximum current density is 1500  $\text{A}/\text{cm}^2$ . To the nWell- substrate junction direction current density also almost linearly decreases, but near nWell-substrate junction it decreases more smoothly.

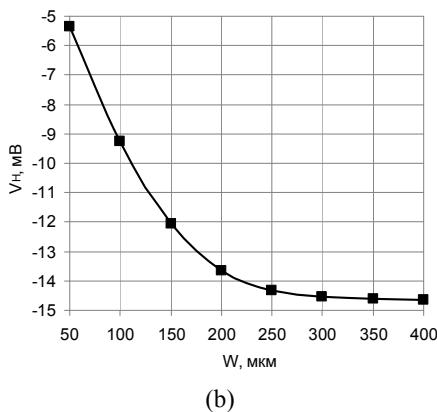
As Figure-6(c) shows, in SCR nWell – p+ junction electron mobility is 300-400  $\text{cm}^2(\text{V}\cdot\text{s})$  and it increases to nWell – substrate junction and near that SCR is more than 1000  $\text{cm}^2(\text{V}\cdot\text{s})$ .

Thus, if current density is maximum (more than 1000  $\text{A}/\text{cm}^2$ ), electron mobility does not exceed 500  $\text{cm}^2(\text{V}\cdot\text{s})$ . Relatively low Hall plates' Hall voltage values can be explained by this.

Influence of Hall plates' geometrical dimension Hall voltage was simulated further. Figure-7 shows drain current (a) and Hall voltage on Hall plate's width dependences diagrams if Hall plate's length is L=200  $\mu\text{m}$ .



(a)



(b)

**Figure-7.** Drain current (a) and Hall voltage on Hall plate's width dependencies diagrams if Hall plate's length is L=200  $\mu$ .

As the diagram in Figure-7(a) shows, the drain current on Hall plate's width dependence is linear. The diagram in Figure-7(b) shows that Hall voltage on Hall plate's width dependence is nonlinear and if  $W/L > 1.5$  dependence saturation occurs.

Such dependency is usually explained by geometrical factor influence that is included into formula for the Hall voltage [7]:

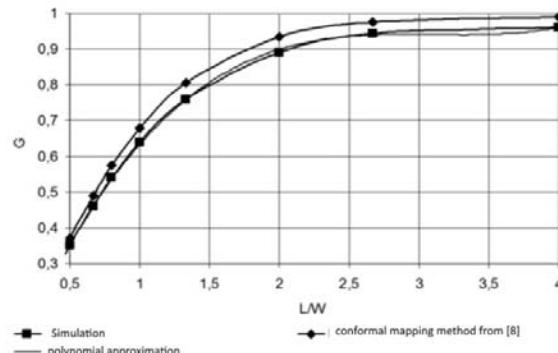
$$V_H = G \mu_H V_B \frac{W}{L}, \quad (1)$$

Where G - is a geometrical coefficient ( $0 < G \leq 1$ );  
 $\mu_H$  - Hall mobility;  
 $V$  - applied voltage (in this case between drain and source  $V_D$ );  
 $B$  - magnetic field induction;  
 $L$  - Hall plate's length;  
 $W$  - Hall plate's width.

According to the results of the simulation geometrical coefficient G on L/W ratio dependency is constructed. It is shown in Figure-8. This diagram is well approximated by third degree multinomial:

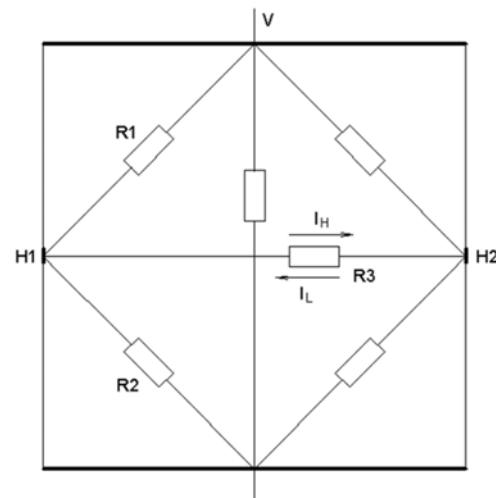
$$G \approx 0.033 \left( \frac{L}{W} \right)^3 - 0.311 \left( \frac{L}{W} \right)^2 + 0.966 \left( \frac{L}{W} \right) - 0.054, \quad (2)$$

to a precision of 2%. For the comparison, the figure shows a diagram for the geometrical coefficient G from [8] that was calculated by conformal mapping method. It appears that diagrams of geometrical coefficient dependence, derived by simulation and obtained by conformal mapping method differs no more than 5%



**Figure-8.** Geometrical coefficient G on L/W ratio dependence diagrams.

The Hall voltage saturation phenomenon if  $W/L > 1.5$  can be explained by a simple model. The voltage, appearing in a cross section leads to vertical field redistribution in the Hall plate. The farther from center the larger is the Hall field and the greater is redistribution of vertical current and field. Hall plate can be presented as 4-port network that has an input resistance to Hall contact while other contacts grounded. The voltage in Hall contacts leads to current flowing through these equivalent resistances. This process model is Figure-9. The cross current is determined by magnetic induction and opposite drift current is determined by Hall voltage. Differential current is cross current that is equal to drift ground current due to horizontal current destabilization. The simple model gives us a good result close to experiment obtained in [8].



**Figure-9.** Hall plate model.

For current density created by Lorentz force, one can write

$$J_L = n \mu_H F_L, \quad (3)$$



Where  $q$  = electron charge,  
 $n$  = carrier density (in this case electrons')  
 $FL$  = Lorentz force  
 Applying I to (3) it results to

$$J_L = qn\mu^2 EB = qn\mu_H^2 \frac{V}{L} B, \quad (4)$$

The current created by Lorentz force is

$$I_L = J_L dw_{eff} = qn\mu_H^2 dw_{eff} \frac{V}{L} B, \quad (5)$$

Where  $d$  = Hall plate's thickness (nWell layer under p+ layer in this case)

$w_{eff}$  = effective width depending on Hall plate's length and width

Similar to current density, created by Hall voltage, one can write:

$$J_H = qn\mu_H E = qn\mu_H \frac{V_H}{W}, \quad (6)$$

Then the current created by Hall voltage is

$$I_H = J_H dw_{eff} = qn\mu_H dw_{eff} \frac{V_H}{W}, \quad (7)$$

Then one can write:

$$\frac{V_H}{R} = I_L - I_H = qn\mu_H dw_{eff} \left( \mu \frac{V}{L} B - \frac{V_H}{W} \right), \quad (8)$$

Where  $R = R1 \parallel R2 \parallel R3$ .

After some simple rearrangements:

$$\frac{V_H}{R} = \frac{\mu \frac{V}{L} B}{\left( \frac{1}{Rqn\mu_H dw_{eff}} + \frac{1}{W} \right)}, \quad (9)$$

Multiplying numerator and a denominator by  $W$ , we finally get:

$$\frac{V_H}{R} = \frac{\mu VB \frac{W}{L}}{\frac{W}{Rqn\mu_H dw_{eff}} + 1}, \quad (10)$$

The value in denominator  $W/(Rqn\mu_H dw_{eff})$  is dimensionless. Resistance  $R$  is about 1700-2000 Ohm that's why is comparable to 1. It is seen that if  $W/L < 1$  the value  $W/(Rqn\mu_H dw_{eff}) < 1$  and Hall voltage is defined by the numerator in (10) and increases if  $W$  value rises. When  $W/L$  is more than 1,  $W/(Rqn\mu_H dw_{eff})$  also becomes more

then 1 and Hall voltage stops increasing, i.e. it is getting a saturation, as in diagram in Figure-7(b).

## CONCLUSIONS

Another effect was observed as on measurement as on simulation – series Hall plates' connection via Hall contact does not lead to adaptable Hall voltage combining. Moreover Hall plates are rather narrow and their width is narrow enough for Hall voltage saturation. There is a simple explanation to this fact.

Field distortion has different character at Hall plates' edges and inside the plate. Inside the plate, vertical field positions at an angle to vertical. At edges the field becomes vertical, but distracted, conditioned by current changes. Series connection of Hall plates minus Hall contact to the following plus contact causes distortion offields and currents at the Hall plates' edges, which lead to such a phenomenon.

Thus, based on research and Hall plates' simulation one can make the following conclusion:

1. From all manufactured Hall plates test options maximum Hall voltage is reached in 1st option that has a continuous contact along the structure width;
2. Hall plates TCAD simulation to optimize the construction and size showed that the optimal  $W$  and  $L$  ratio is within  $1.25 < W/L < 1.5$ .
3. Hall plates' simple model is offered and Hall voltage formula derived which explain the Hall voltage saturation phenomenon if  $W/L > 1.5$ .

## ACKNOWLEDGEMENT

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