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LOW POWER CODEC CIRCUITS FOR ULTRA PORTABLE DEVICES

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ABSTRACT

The working of the CODEC circuit is to run the battery based portable devices with some of the design constraints, and thereby improving the designing metrics like power, area. The present work object at designing a combined encoder and decoder circuits (CODEC) which is useful in low power devices by modifying the delay buffer, clock gating circuits, multiple bus width consider as single bus width of the encoding and decoding circuits. The synthesis, digital fabricated physical design implemented in SoC Encounter tool using 45nm technology. Comparisons were made between the 32 bit and 64 bit CODEC designs with power, area, timing and error estimation. Results are procured exposition a high performance improvement in the conventional CODEC system when compared with design metrics and power consumption.

Keywords: encoder decoder CODEC encounter tool.

INTRODUCTION

Multimedia and wireless communication devices have experienced an exorbitant growth recently. One of the important factors in the wide spread of these devices is low power and area [1]. In such devices due to technology scaling, bandwidth and speed becomes crucial. The performance of those systems is limited by interconnection bandwidth between chips, boards and networks. A low power delay buffer plays an important portion of the circuit for such devices. The scaling of process technologies to nano meter regime has resulted in a rapid increase in leakage power dissipation [5]. Continued scaling of process technologies has led to smaller device features, faster clock speeds, and rapidly shrinking interconnects [10]. So this results in a huge amount of power consumption. As a result low power designs have become inevitable part of today's devices, hence designing a low power circuits have become an eminent factor in advanced VLSI technology.

Power consumption is one of the major disputes in the design of high-performance logic circuit. Power consumption is an important part of the equation determining the end product's size, weight, and efficiency [2]. For improved performance and low power consumption in VLSI system, a cautious design of storage elements is needed.

In communication and multimedia devices a CODEC plays significant role by encoding and decoding the larger files such as video and audio files. Hence to design an efficient CODEC we need to meet the two major constraints in VLSI i.e. power and area. A Bus - Invert technique [2] is used to meet the challenges that are faced during the power reduction scheme in a CODEC. In Bus-Invert technique, power utilized by the CODEC is reduced by reducing the rate of switching transitions occurred in information byte. The number of transitions in a byte of information are measured and inverted and encoded.

Simulation and synthesis results are very important in the design of encoder and decoder circuits will give idea for real time fabrication which is useful in various applications. Even for before going for real time fabrication if we very the synthesis result we will get complete idea about our designs so that it is possible to do some modification to meet proper design. The present paper we developed and tested different type of encoder and decoder sub circuits for battery based multimedia application

Wireless technology is a costly and more time-consuming process. If we consider a bottom-up strategy, a suitable candidate sub-block in a CODEC system might not necessarily be one that offers significant reduction in power consumption, area, timing but instead would be the one that fits well into the system without demanding drastic changes in the currently agreed and well developed standard. The present and emerging applications that allow for a fully compact design in a quest to provide a superior performance rather than a more complicated design cost. Consequently, following the target application requirements, encoding and decoding circuits can be implemented in many different metrics and using modified bus invert Berger code.

The main target of this work is proposing a low power, area encoding, decoding circuits for Portable Devices (UPD); i.e. compact, small scale, short range and low power multimedia devices that may include wireless sensor systems, asymmetric communications, medical systems or modern hearing aid devices. Such applications do not usually demand very high data rates. In most cases the range of required throughput is from milli watts power

using a 90nm technology up to nano watts using 45nm technology. As a matter of fact, the overall physical layout and power, area is the critical aspects. Small physical dimensions are critical for design devices; therefore, it is desired to reduce implementation costs as well as better portability in on or near body communications. Low power operation is crucial to prolong the battery-driven life-time of the device especially in cases where access is difficult such as medical implants, or as for remotely placed sensor nodes.

DESIGN AND IMPLEMENTATION

Synthesis result

The present combined CODEC (encoder and decoder) design, synthesis results verified from CADENCE SOC encounter tool, CADENCE after defensible simulation with different data bits like 6, 8, 10, 14, 32 and 64 bits with the different technologies and calculated error estimation. The digital process used in this paper, the synthesis tool was a Design CADENCE GUI tool. To obtain the synthesis results, first we developed VHDL code for encoder and decoder then implemented combined as CODEC top level module. The synthesis results are optimized with the physical layout of the design and which will give the complete details about power and area and timing based on the real time digital fabrication process will be developed. In the synthesis process the developed VHDL code would be converted in to logic gates or the hardware module of the design for further implementation. To carry out the synthesis use the basic procedure and the results are shown in Figure-1. In this paper we verified with three technologies like 90nm, 65nm, 45nm, with power area and timing and compared with existing CODEC design with 90nm. Based on these design metrics variations we had developed a digital physical layout for encoder, decoder a with that metrics finally the complete compact fabricated digital physical layout implemented using SoC tool shown in the final result. In addition to that even the number of errors reduced for different bits with checker bits.

Figure-1 shows the synthesis result of 64 bit encoder implemented in SoC encounter using 45 nm technologies. In this paper we implemented individually the design of Encoder and its sub circuit's next decoder and its sub circuits then combined CODEC successfully implemented as per the above technology. Especially in this paper focused on synthesis of CODEC with fabricated digital physical layout and carried out the design metrics for the low power portable devices and reduced errors for even higher order and lower order bits.

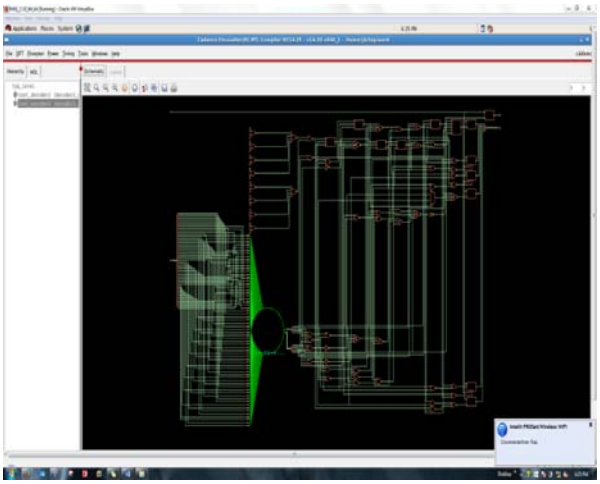

Figure-1. Synthesis result of 64 bit encoder.

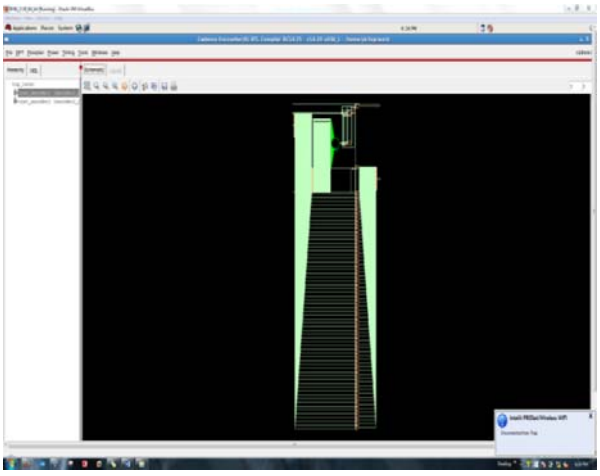

Figure-2. Synthesis result of 64 bit decoder.

DIGITAL PHYSICAL LAYOUT RESULT

The proposed CODEC was synthesized for selected bus widths of 64 bits using the CADENCE tools for 45nm technology. To get a further appreciation about the scalability of the proposed specified architecture in 45nm nano meter technology, synthesis of the proposed complete design with 45nm technology is successfully applied. To reduce the power and area and timing in the present design used delay buffer, clock gating technique in the 45-nm technology. The total reduction of power consumption and is achieved from the CODEC design. One can see that the superiority of the proposed modified designs is still apparently in 45-nm technology in that the power and area is almost trifling.

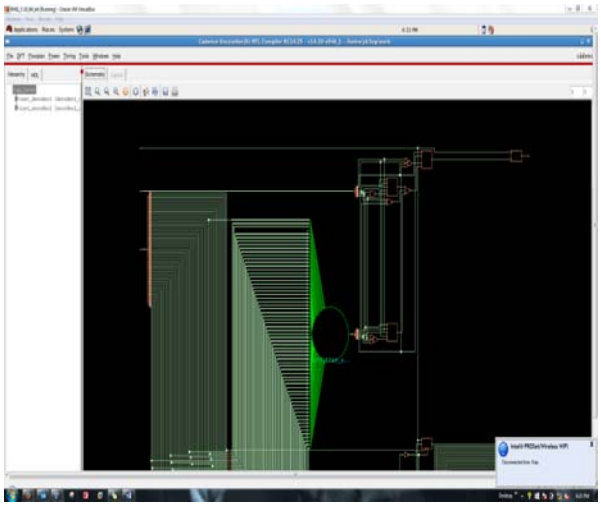

Figure-3. Synthesis result of 64 bit CODEC (encoder and decoder).

In the most modern 45-nm technology, the higher power can be controlled to within an impossible level for simple complicated CODEC design approach. In modern applications specified design is used in modern technology, other area and power reduction techniques are reduced from the current design.

To highlight the result of the proposed specified design, and synthesis and physical layout proved better result for some portable applications. Hence the synthesis and fabricated physical layout of the design results of the existing CODEC design are preceded by the synthesis and power reports of the proposed circuits of encoder and decoder. The existing methodology only is simulated using some basic simulation tools and the analysis is taken out as discussed above which tells that the power and area and the time taken are importantly very high. Fig. 2 shows the physical layout synthesis of the proposed decoder. Physical synthesis, layout design of CODEC for I = 64 is carried out by considering the parameter 45nm. From this come to know that the proposed method consumes less power and area when compared with the existing method. The proportional comparison is done by real time fabricated physical layout in the present, proposed methodology which will show better improved results for power and area.

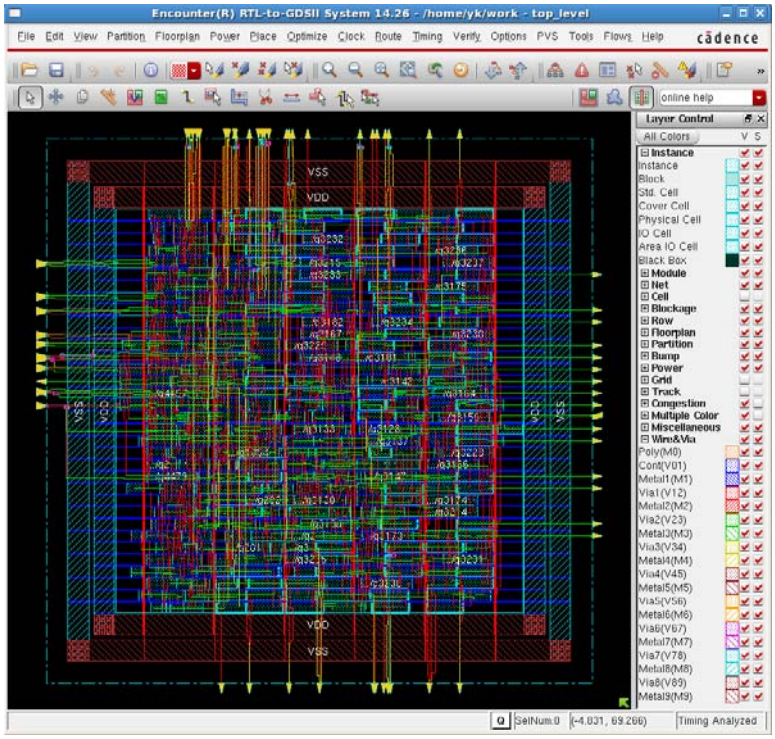

Figure-4. Overall CODEC digital physical layout for I = 64 bit.

Table-1. CODEC 45 nm technology (proposed work).

K	I	CODEC Power (nw)	CODEC Area (μm^2)	CODEC Timing (Ps)
3	6	47479.836	046	2231
4	7	57099.074	096	3143
	10	59656.712	123	4312
	14	634199.235	198	5234
	16	138751.024	228	5672
5	30	138751.024	425	5813
	32	222149.049	468	6432
6	64	346225.247	891	7221

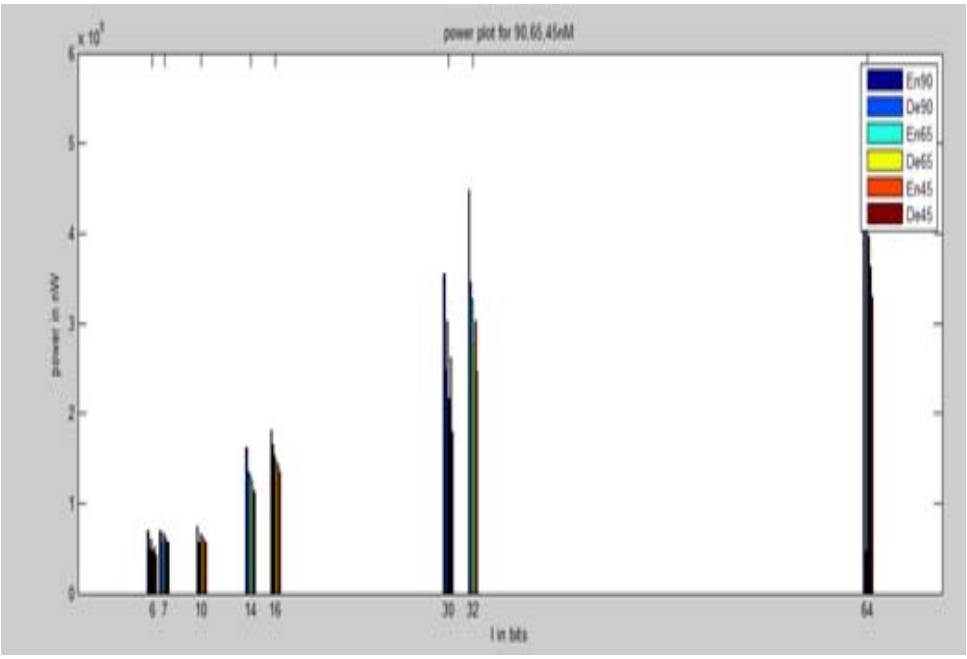

Figure-5. Overall CODEC power bar chart of 90, 65 and 45 nm technology for I = 64.

Table-2. Area estimation (um^2) for various bus widths (I).

K	I	A_{BGIH}		A_{BGIN}		A_{Red}[%]		
		Enc	Dec	Enc	Dec	Enc	Dec	CODEC
3	6	255	265	203	225	20.39	15.09	17.74
4	7	342	220	225	190	34.21	13.63	23.92
	10	660	345	445	267	32.57	22.60	27.58
	14	990	550	725	483	26.76	12.18	19.47
5	16	1950	1021	1300	830	33.33	18.70	26.01
	30	3500	1900	2100	1602	40.00	15.68	27.84
6	32	3700	2158	2800	1928	24.32	10.65	17.48
	64	4215	5217	3409	3237	19.12	37.95	28.53

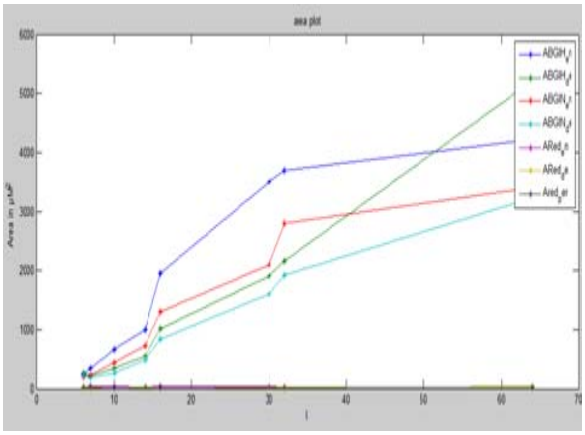

Figure-6. Overall CODEC power plot of 90, 65 and 45 nm technology for I = 64 bit.

CONCLUSIONS

The present work implemented in details the synthesis, digital physical layout design of a compact CODEC system, with design metrics like power, area, and timing. Synthesis physical layout circuits was done and the overall system performances for CODEC system design parameters with power, area was found better when compared to the conventional systems for a random input bits, providing a better design for portable devices and also minimizing error rate.

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