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DESIGN OF A 2.4 GHZ CMOS LOW NOISE AMPLIFIER FOR WIRELESS SENSOR NETWORK APPLICATIONS

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ABSTRACT

This paper presents a design of 2.4 GHz low noise amplifier (LNA) for wireless sensor network (WSN) applications using CMOS 0.13 µm Silterra process. The proposed LNA employs a self-biased inverter to obtain high gain and able to operate at low supply voltage. The simulation results indicated that the proposed LNA achieves an input return loss (S11) of -37.7 dB, output return loss (S22) of -28.1 dB and gain of 10.5 dB. Moreover, the noise figure (NF) of 5.4 dB and the input third order intercept point (IIP3) of -10 dBm is obtained at 0.9 V supply voltage. The chip area is 0.49 mm^2.

Keywords: low noise amplifier, wireless sensor network, self-biased inverter, noise figure, low power.

INTRODUCTION

Wireless sensor network (WSN) have gained extensive used in a variety of many applications such as bio-sensing, industrial control, environmental monitoring and energy monitoring. WSN also is gaining demand in agriculture applications. The emergence of WSN technology requires the transceiver to be small, highly integrated and inexpensive while maintaining very low power consumption.

The main challenges of WSN are device size, low cost and ultra-low power capabilities to allow several months or year of operation. Among these requirements, the power constraint is the most challenging. Furthermore, ultra-low power consumption imposes stringent design constraint for the sensitive radio frquency (RF) and analog circuits (T. Taris, JB. Begueret and Y. Deval, 2011). Low noise amplifier (LNA) is a part of the most important building blocks for displaying receiver chain. Several previous works propose to combine the LNA and the mixer, supplied by the same DC current, to save power consumption and sometimes with the mixer and the oscillator (A. M. Javinen *et al.* 2005), (T. Song *et al.* 2007), (M. Tedeschi, A. Liscidini and R. Castello, 2010)

The first crucial component in RF receiver is LNA. LNAs are used in various applications, for example in, Global Positioning System (GPS) receivers, wireless data systems, satellite communication, cellular handsets, radio systems and etc. The antenna transmitted the weak RF signal with minimum noise contribution to the amplifier. The LNA has significant tradeoff between gain, noise figure (NF), stability, linearity, input impedance matching and power consumption (Baoyong Chi, Bingxue Shi and Zhihua Wang, 2006), (Bo-Shih H and Ming-Dou K., 2006). The noise in the receive chain is reduced by the gain of the LNA and therefore the function is primarily to boost the signal power while adding minimum noise and distortion to the signal. Low NF therefore results in improved reception of the received signal. LNAs can adopt many design topologies and structures, but the input and output impedance must be matched (Chihoon Choi, Joonwoo Choi and Ilku Nam, 2011).

In this paper, a Complementary Metal Oxide Semiconductor (CMOS) LNA is proposed using self-biased inverter at single stage. A 0.9 V is the power supply used to reduce the power consumption while the RLC circuit is used to achieve a good input and output matching.

SELF-BIASED INVERTER

The LNA circuit is biasing the transistor in weak inversion area (A. Azizan *et al.* 2014). Thus, the highest value of transconductance (g_m) is devided by a drain current (i_d) in the transistor is achieved (T.Taris, JB. Begueret, Y. Deval, 2011). In this project, the basic topology of both PMOS and NMOS transistors amplify the input signal is employed. Based on the self-biased inverter the low g_m will perform in moderate inversion mode requires an active load to provide large gain.

Figure-1 shows gain bandwidth of a single stage configuration. The self-biased cell exhibits the larger gain bandwidth compare to single stage transistor as can be seen from Figure-1. An input bias of the self-biased inverter can be controlled via the feedback resistor and the value might be set by changing the size of both transistors of NMOS and PMOS (J. Ayers, K. Mayaram, and T. S. Fiez, 2007).

THE PROPOSED LNA

Figure-2 shows the proposed LNA's block diagram. There are three main important blocks in designing LNA which are input matching, LNA stage and output matching. The input and output matching is essential to ensure that the incoming signal from 50 Ω antenna is match with the impedance of LNA. Similarly, at the output stage of LNA, the output impedance is 50 Ω to be matched with equipment terminal for measurement purpose. The supply voltage V_{DD} is important as a power supply and biasing voltage is used to bias the transistors in the LNA.

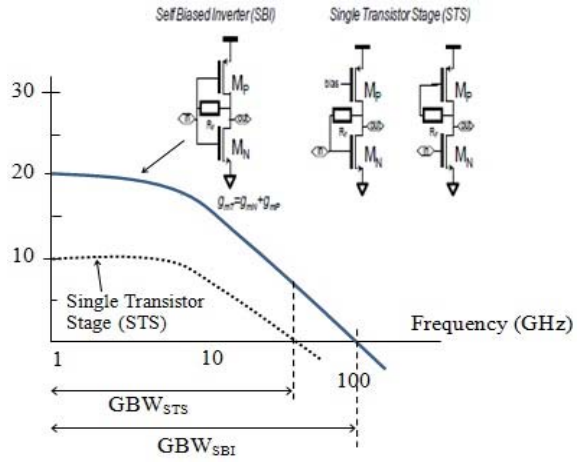

Figure-1. Gain Bandwidth of single stage configurations (T.Taris, JB. Begueret and Y. Deval, 2011).

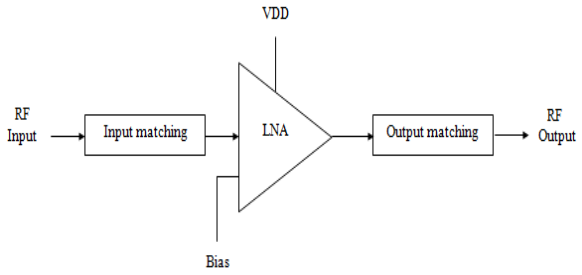

Figure-2. Blok diagram of the proposed LNA.

Based on the preliminary studies, the basic requirements of the LNA includes low noise figure, good gain, high linearity and low power consumption (A. Msolli *et al.* 2012). The design target for the low noise amplifier is specified in the Table-1.

The design of a low noise amplifier presents a considerable challenge because, the above stated requirements of the LNA are all equally important, however to achieve them simultaneously is a difficult task (H. Sahoolizadeh, 2009). As an example like the source impedance, which yields a minimum noise figure, may differ considerably from one that maximizes power gain. Hence it is essential to understand the tradeoffs involved in the LNA design.

Table-1. LNA design specification.

Parameter	Specification
Frequency (G Hz)	2.4
S11 (dB)	<-15
S22 (dB)	<-15
S21 (dB)	>10
Noise Figure(dB)	<5
Power consumption (mW)	<5

CIRUCIT DESIGN

The proposed LNA design is shown in Figure-3. The NMOS transistor of M1 is a common-source amplifier and the PMOS transistor of M2 is based on self-biased inverter together with biasing resistor RF. The transistors size for M1 and M2 are 4.5/0.13 µm/µm and 5/0.13 µm/µm, respectively using 0.13 µm CMOS process. The inductor LL of 1.3 nH, resistor RL of 2 kΩ and capacitor CL of 1 pF helps to increase gain.

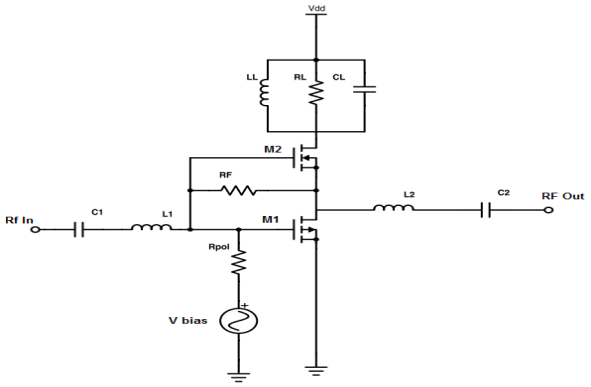

Figure-3. Schematic of the proposed LNA.

The proposed LNA provides an input matching and output matching to be matched with 50 Ω impedance. Therefore, C1 and L1 is part of input matching with values of 10 pF and 10 nH, respectively. Meanwhile, L2 and C2 is part of output matching. The L2 of 10 nH and C2 of 2 pF are used to achieve 50 Ω output matching.

The supply voltage of 0.9 V is used and the biasing voltage (Vbias) for M1 is 0.7 V. The low supply voltage helps to decrease the power consumption of the proposed LNA. The component values of the proposed LNA are summarized in Table-2.

Table-2. Component values of the proposed LNA.

Component (spelling mistake)	Value
C1	10 pF
C2	2 pF
CL	1 pF
LL	1.3nH
L1	10 nH
L2	10 nH
RF	2 kΩ
RL	2kΩ
R_{pol}	2 kΩ
Vbias	0.7 V
VDD	0.9 V

SIMULATION RESULTS

The proposed circuit LNA is simulated using Cadence Virtuoso in 0.13 µm Silterra CMOS technology. The S-parameters simulation results are shown in Figure-4. The input return loss (S11) is -37.7 dB and output return loss (S22) is -28.1 dB at 2.4 GHz. Figure-5 shows a DC gain (S21) of the proposed LNA. The gain of 10.5 dB is obtained.

The noise figure (NF) is presented in Figure-6 which indicates the NF is about 5.8 dB at operating frequency of 2.4 GHz. Figure-7 shows the linearity performance of the proposed LNA. The input third order intercept point (IIP3) of −10 dBm is achieved.

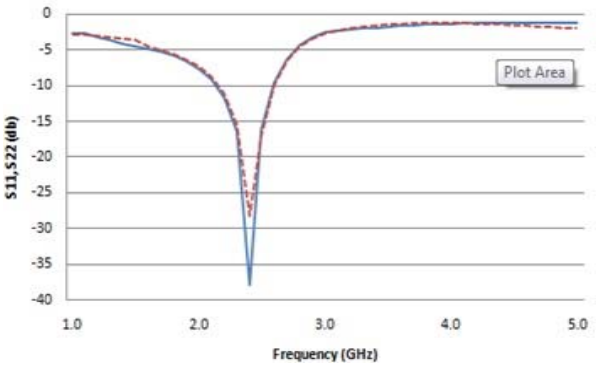

Figure-4. Input return loss, S11 (blue line) and output return loss S22 (dotted red).

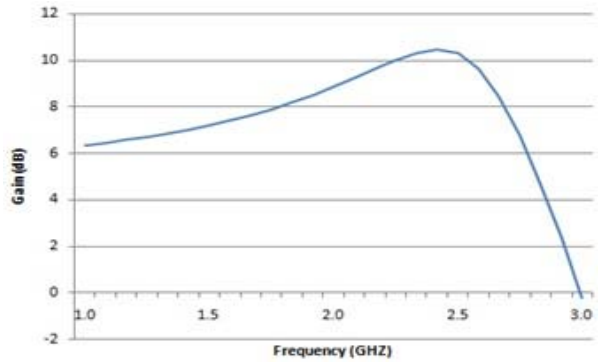

Figure-5. Gain of the proposed LNA.

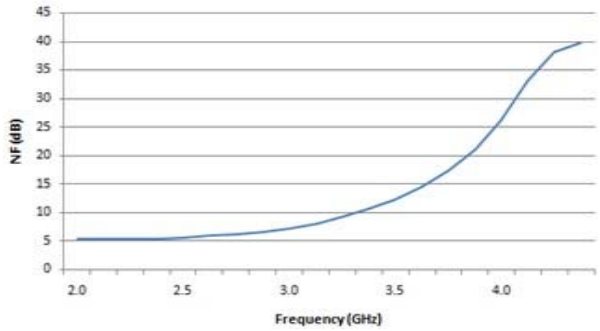

Figure-6. Noise figure simulation result.

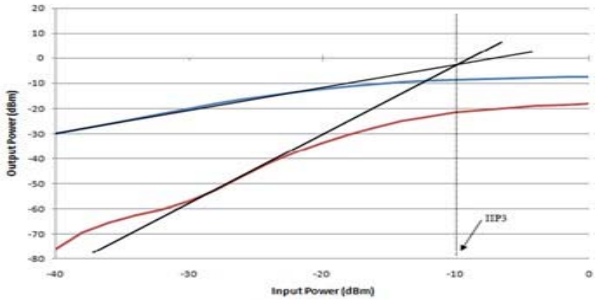

Figure-7. Third order intercepts point (IIP3).

Figure-8 shows the layout of the purposed LNA. The RF input and output ports are placed on opposite sides of the chip to improve port-to-port isolation. Since on-chip probing is used to measure the performance of the LNA, standard Ground-Signal-Ground (GSG) probes are used at both the input and output RF ports. The capacitors are implemented using MIM capacitor while the inductors are on chip spiral inductors. The chip area is 0.7 mm x 0.7 mm including bond pads. The layout will be taped out in the future for testing.

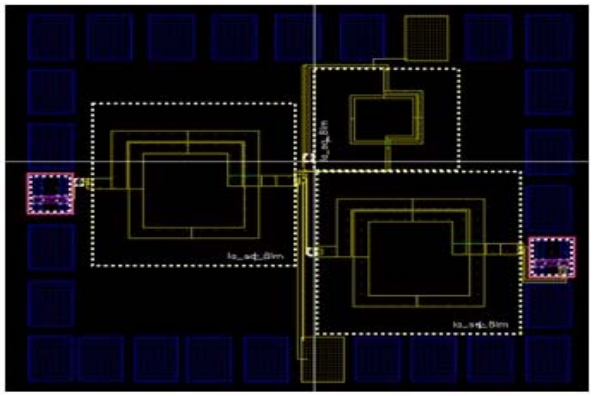

Figure-8. The layout of the proposed LNA.

Table-3. Performance comparison with previously published works.

Reference	T.Taris, 2011	B. Liu, 2009	S.A.Z Murad, 2013	Chihoon Choi, 2011	This work
Technology (µm)	0.13	0.18	0.13	0.18	0.13
Frequency (GHz)	2.4	2.4	2.4	2.4	2.4
Vdd (V)	0.6	0.9	1.2	1.8	0.9
S11 (dB)	-15	-18.1	-26.9	-15	-37.7
S21 (dB)	15.7	14.4	23.9	17	10.5
S22 (dB)	-14	-12.7	-20.6	-7	-28.1
NF (dB)	4.6	1.6	5.6	0.01	5.4
IIP3 (dB)	-12.2	-9	-5.8	N/A	-10
Power (mW)	0.13	0.96	8.1	7.2	2.8
Chip Size (mm^2)	0.62	N/A	0.64	N/A	0.49

Table-3 shows the performance comparison of the proposed LNA with previously published works. The proposed LNA obtained low power with low chip area while other performances are comparable.

CONCLUSIONS

This paper presents a single-stage CMOS low noise amplifier (LNA) using a self-biased inverter for low power using Silterra 0.13 µm technology. The simulation results shows that the LNA achieve the good input and output matching, low NF, high linearity while consumed 2.8 mW power at a supply voltage of 0.9 V.

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