



# PERFORMANCE ANALYSIS OF D-FLIP FLOP USING SINGLE ELECTRON NANODEVICES

S. Rajasekaran and G. Sundari

Faculty of Electronics Engineering, Sathyabama University, Chennai, India

E-Mail: [srsekar7@gmail.com](mailto:srsekar7@gmail.com)

## ABSTRACT

Single electron technology offers the ability to maintain the transport of individual electrons. In this paper, we present a D-Flip flop using CMOS and single-electron Technology which is compare with normal logic D-flip flop. Single Electron Transistor (SET) is distinguished by a very small scale device, low power dissipation, high speed and high performance, is one of the most promising Nano-electronics devices to replace conventional CMOS. The single-electron D flip-flop and CMOS based D-flip flop is designed and studied the comparative analysis with normal flip-flop design. The flip flop design is simulated using SPICE simulator and analysed the performance of its varies parameters.

**Keywords:** Coulomb blockade, logic circuits, CMOS, single electron device (SED), flip-flop.

## 1. INTRODUCTION

The development of complementary metal oxide semiconductor (CMOS) technology is still under downscaling progress and the increase in the power consumption has become a main issue in the constructing large-scale integrated circuits. Consequently, the single-electron transistor (SET) has fascinated considerable attention in the recent years because of its budding for high packing density and low power consumption.[1] The data in the form of bits are represented by the presence or absence of single electrons at the Quantum conducting islands. The fundamental principle of single-electronics is the Coulomb blockade, which was first observed and deliberates by Gorter [2].

It is widely known that falling feature size and increasing the transistor compactness facilitate vast improvement in the semiconductor based technology. Single-electron Technology [3] also attractive features like enormously low power consumption, condensed dimensions, excellent current control and noiseless behaviour. A variety of useful devices and concepts utilizing the single-electron tunnelling features, such as, cellular automata, the binary decision diagram device,[4] and SET logic gates [5,6], single electron memories [7], Control-Control-Not gate [8], analog to digital converter[9], stochastic associative memory [10] have been projected and tested by actual devices. The purpose for computer-aided design and simulation of single-electron circuits has long been recognized for many applications. Several simulators and simulation methods have been developed to support single-electron circuit design. SPICE is such a simulator analysed for varies hybrid circuits [11].

Fabrication of SEDs is a more costly and time-consuming process and, So, the computer-aided design and simulation tools have been developed in order to study these circuits. A key improvement in SED circuits was due to technology and the development of simulator tools like SIMON [12] and SPICE [13], which is a Monte Carlo-based tool capable to design, simulate and study SEDs and circuits.

This paper is described as follows: Section 2 describes principle of Single electron tunneling and device structure. The design of CMOS based and single-electron D flip flop is examined with the Logic gates design is discussed in section 3. Simulation results and discussion are presented in this Section 4. Finally, conclusions are given in section 5.

## 2. SINGLE-ELECTRON TUNNELLING

### 2.1 Coulomb blockade

The transport of single electron charge across the tunnel junction is referred as tunnelling, where the quantum effect of tunnelling is to control and measure of single electron, tunnelling time is approximately  $10^{-15}$  seconds. That tunnel event of electron is described by single electronics box orthodox theory also as the stochastic nature and the energy quantization process is in discrete. If the additional electrons are tunnelled through the energy barrier of the insulating barriers, its control the flow of the system is said to be Coulomb blockade.

The principle of single electronics is that to needs Coulomb energy  $E_C$  to charge an island with an electron. This energy is:

$$E_C = e^2/2C \quad (1)$$

Where  $C$  is the capacitance of the island,  $e$  is the elementary charge [14]. Based on the Coulomb energy the necessary conditions for coulomb blockade are

a) The bias voltage must less than the charged element divided by the self-capacitance of the island.

$$V_{bias} < e/C \quad (2)$$

b)The thermal energy of the source must be lower than the charging energy else the electron will pass the quantum island via thermal excitation.

$$K_B T < e^2/2C \quad (3)$$



c) The electron states are localized on islands all tunnel resistances must be greater than the fundamental quantum resistance

$$R_T > R_Q = h / e^2 \approx 25.813 \text{ K}\Omega \quad (4)$$

Where  $h$  is Planck's constant.

## 2.2. Single-Electron Transistor (SET)

Single-electron Transistor (SET) devices can maintain and to control the motion of individual electrons. These devices formed at the intersection between of two major research trends: mesoscopic physics and the electronic circuits' miniaturizations. Most of the original motivation for the studying of SET Nano-devices came from mesoscopic physics. Mesoscopic physics is the study of artificially designed and constructed systems that exhibit quantum behaviour. Second important research trend is that the attention on SET devices is the electronic circuits miniaturizations. The information based technologies are becoming the most increasingly important in our society are advancing technology so quickly because we keep finding ways to manufacture circuits more and more cheap. The power dissipated by a circuit is one of the factors limiting the electronic circuits'

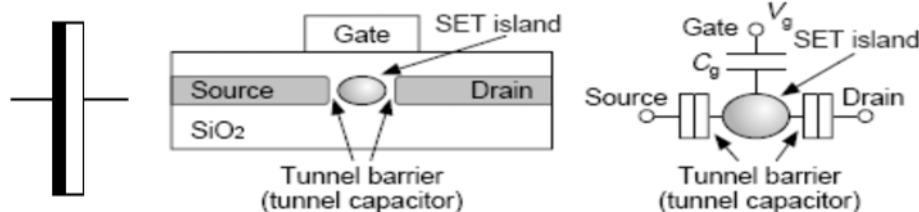
miniaturizations. These circuits can be made very small size and dissipate less power making them potentially useful for high dense integrated circuits. The Coulomb energy in these systems can be characterized by a capacitance which depends on the size of the quantum dot few (~2nm) nanometer scale and also may play in the range of  $10^{-15}$  F or less [14].

Single-electron transistor circuit consists of conducting quantum islands, tunnel junctions, capacitors, and voltage source. The silicon quantum islands are arbitrarily connected between with tunnel junctions, capacitors and voltage sources.

The voltage source is connected to the electrodes like the source, the drain and two gates. Further addition of two gates which are the parasitic capacitance and background charge  $Q_0$ . Normally the current flow under the control of gate capacitance  $C_g$ , so they maintain average current flow through the transistor. The charge on the island is calculated under electrostatics.

$$V(n) = (ne + Q_0 + C_1V_1 + C_2V_2 + C_{g1}V_{g1} + C_{g2}V_{g2}) / C_{\Sigma} \quad (5)$$

Where  $e$  - Positive elementary charge,  $n$  - Number of elementary charges that have been added on the island,  $C_{\Sigma}$  - Total capacitance

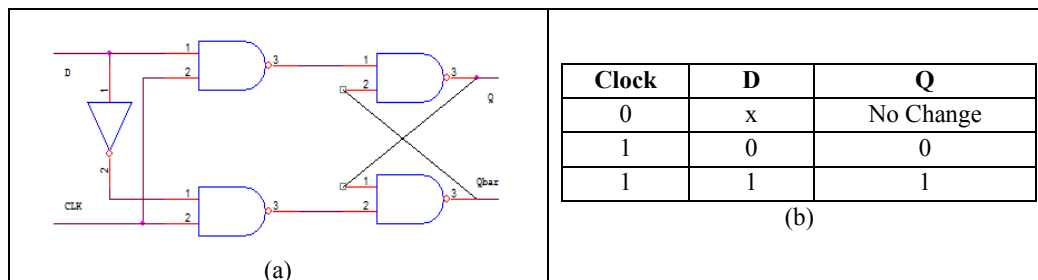


**Figure-1.** Schematic diagram for a tunnel junction, structure of quantum dot island and equivalent circuit of a single electron transistor.

## 3. a) Design of D-Flip-flop using Logic gates

The flip-flop circuit is a basic circuit to store states information by two stable states. It is the basic storage element in the sequential logic systems. The design of D-Flip flop circuit using Logic gates is shown in

Figure-2. This circuit is a memory element with two inputs of different logical combination input values. The D-FF consists of 4 NAND gates and one NOT gate, it consists of different logic function.



**Figure-2.** (a) Diagram of the D-Flip flop using logic gates (b) Logic table.

## b) Design of D-Flip-flop using CMOS

The D-Flip flop circuit design using CMOS is shown in Figure-3. Hence the circuit comprises Eighteen

Transistors, M1 to M18, which consists of four NAND gates using CMOS technology and one CMOS Inverter. The circuit also comprises one data input and a clock just



like the normal D-flip flop design using logic gates. The two voltage sources  $V_{dd}$  are constant and its value is 5V.

The input voltage and clock are applied to D and Clock respectively.

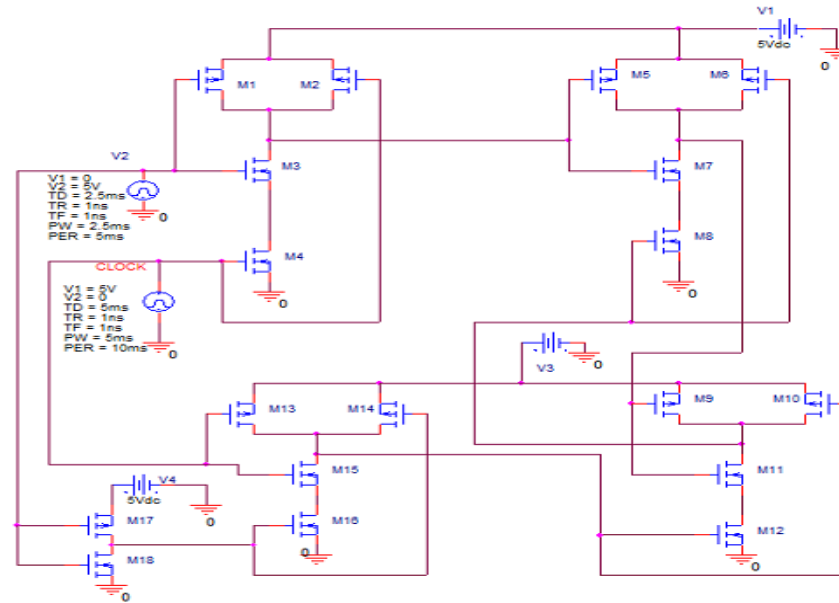


Figure-3. CMOS circuit diagram of D Flip flop.

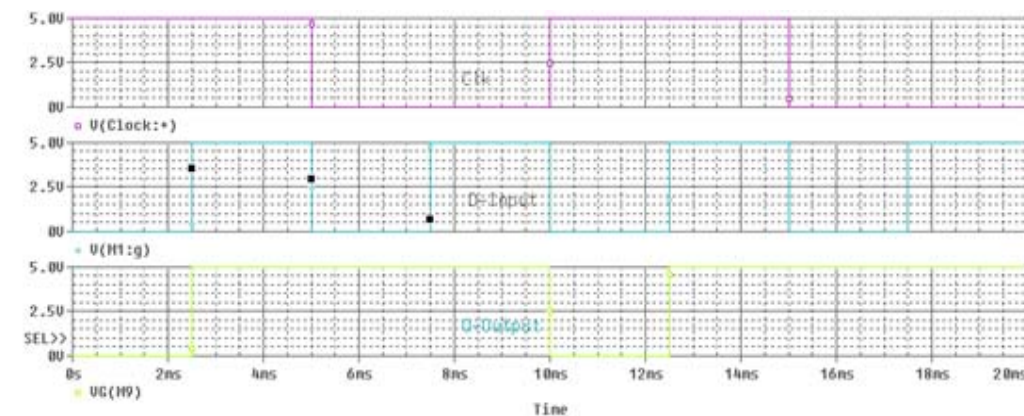


Figure-4. CMOS circuit output of D Flip flop.

The input voltage and Clock, shown in Figure-3, are the inputs of the D-Flip flop named as D and Clk, and it can take only two values 0.0V which corresponds to the logic "0", and 5V which corresponds to the logic "1". The output signals of the D-Flip flop are taken from M9 named Q and Qbar respectively.

### c) Design of D-Flip-flop using Single Electron Transistor

The D-Flip flop circuit design using single electron transistor is shown in Figure-5. Hence the circuit comprises eighteen Transistors, U1 to U18. (i.e.) nine N-type transistors and nine P-Type transistors, which consists of four NAND gates and an Inverter using Single electron technology. The circuit also comprises one data input and a clock just like the normal D-flip flop design using logic gates. The two voltage sources  $V_{dd}$  are constant and its value is 25mV. The input voltage and clock is applied to D and Clock, respectively.

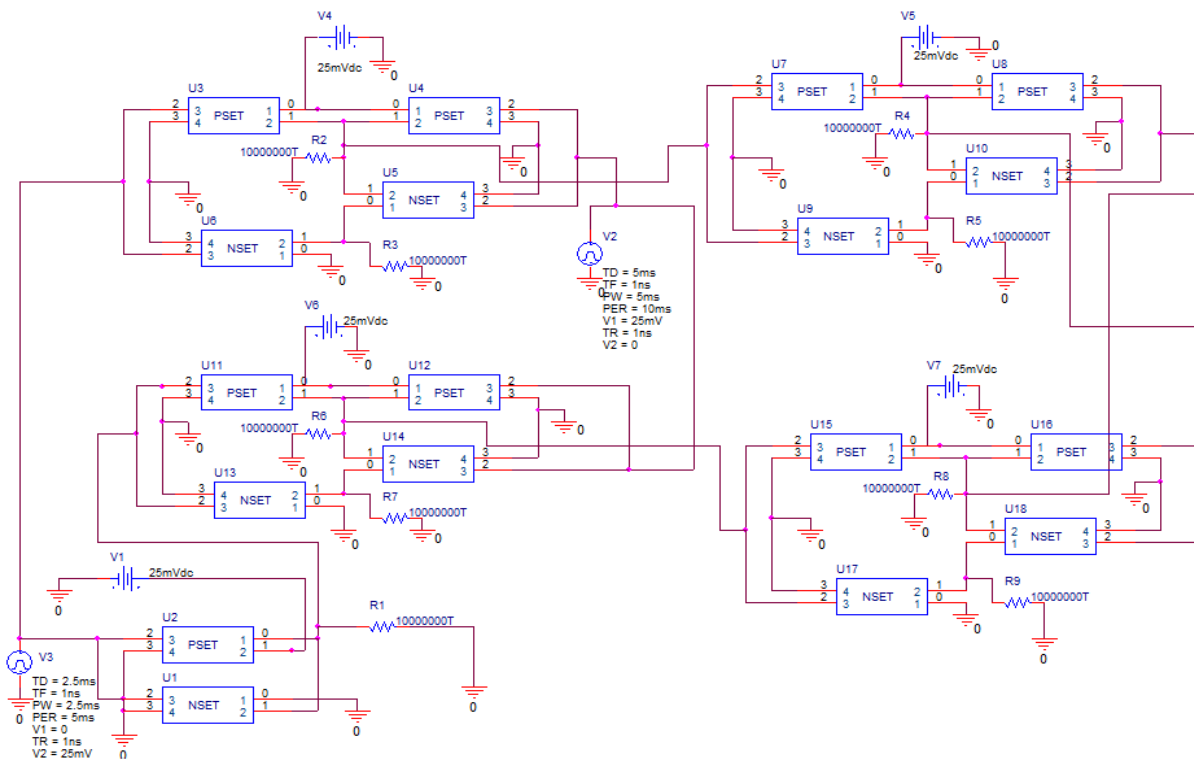


Figure-5. Circuit diagram of single-electron D Flip flop.

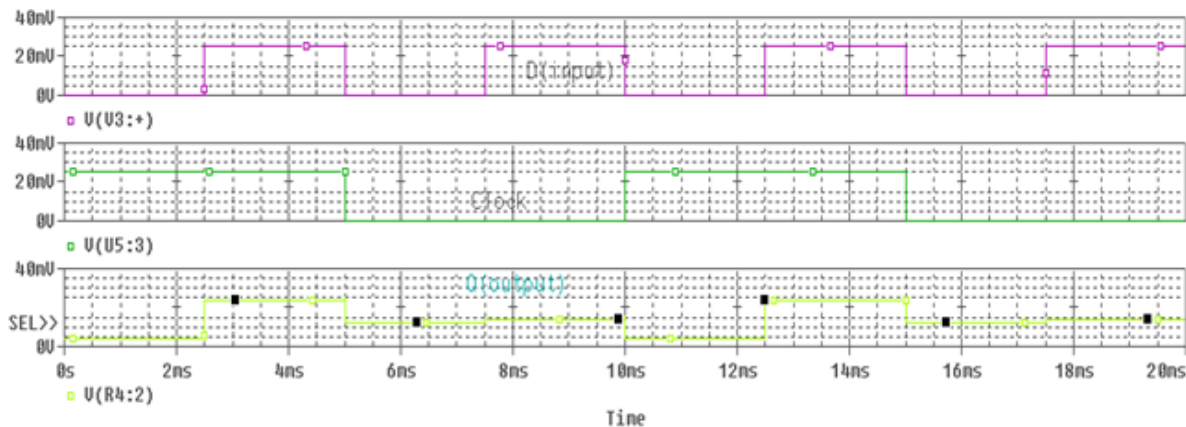


Figure-6. Single Electron Transistor circuit output of D Flip flop.

The input voltage and Clock, shown in Figure-6, are the inputs of the D-Flip flop named as D and Clk, and it can take only two values 25mV which corresponds to the logic “1”, and -0.1V which corresponds to the logic “0”. The output signals of the D-Flip flop are taken from Transistor U18- node 1 named Q and Qbar respectively.

#### 4. PERFORMANCE ANALYSIS OF CMOS D-FLIP FLOP AND SINGLE-ELECTRON D-FLIP FLOP AND RESULT

The single-electron D-Flip flop needs to be analysed the operational characteristics. From the

corresponding output nodes we take the outputs Q and Qbar respectively. The presence of zero voltage in the output islands corresponds to logic 1, whereas -0.1V voltage corresponds to logic 0. Hence, the input-output signals, of this D-Flip flop are shown in Figure 4.6. The two inputs are D and clock and the two outputs Q and Qbar respectively. When the input vector [00] is applied an excess electron is transported via tunnelling to nodes and the output voltage at Q and Qbar becomes 0.1V. When the input vector and the clock signal are high, the electrons tunnelled out of nodes are charged.

**Table-1.** Comparison between the CMOS and Single Electron Transistor.

	CMOS circuit	SET circuit
Switching Speed	$10^{-10}$ s	$10^{-15}$ s
Operating Temperature	>300 degree	<300degree
Current range	nA	Electrons
Voltage range	100mV	100 $\mu$ V
Average power	14.78 $\mu$ W	6.72 $\mu$ W
Delay	3.29ps	0.27ps
Power Delay Product	48.62aJ	1.81aJ

All the simulation results show from the various method the overall performance between the CMOS and Single electron transistor is to motivate the development of single electron nano-device, which is to confirm from the Table-1. The performance analysis between the CMOS and SET technology were tabulated from the Spice Simulator tool, which mostly used for Nano-scale device like SIMON.

## 5. CONCLUSIONS

A single-electron D flip flop and CMOS based D flip flop were presented in this paper. This single electron flip flop circuit produces their Q and Q-bar. The leakage power is very less on Nano-scale single electron transistor. In CMOS circuit the power supply is dissipated in form of heat in pMOS transistor during the charging process. In future the combined like hybrid Nano-scale devices are motivate to reduce the power and delay. Already some hybrid Nano-devices are in the development like SETMOS. From this simulation procedure we realized less delay time, and reduced in power consumption.

## REFERENCES

- [1] HoekstraJaap, *et al.* 2000. Considerations about NanoelectronicGSI processors. Analog Integrated Circuits and Signal Processing. 24(1): 59-71.
- [2] C. J. Gorter. 1951. A possible explanation of the increase of the electrical resistance of thin metal films at low temperatures and small field strengths. 17: 777-780.
- [3] Grabert Hermann and Michel H. 1992.Devoret, eds. Single charge tunneling: Coulomb blockade phenomena in nanostructures. Vol. 294. Plenum Publishing Corporation.
- [4] Karafyllidis I. 2000. Single-electron OR gate. Electronics Letters. 36(5): 407-408.
- [5] Dasigenis M. M., I. Karafyllidis and A. Thanailakis. 2001. A single-electron XOR gate. Microelectronics Journal. 32(2): 117-119.
- [6] I.Tsimperidis, I., I. Karafyllidis, and A. Thanailakis. 2002. A single-electron three-input and gate. Microelectronics Journal. 33(3): 191-195.
- [7] IoannisKarafyllidis. 2002. Design and simulation of a Single-Electron Random-Access Memory Array. Circuits and systems, IEEE Transactions on. 49(9): 1370-1375.
- [8] IoannisTsimperidis, IoannisKarafyllidis, AntoniosThanailakis. 2004. Design and simulation of a Nanoelectronic single-electron universal Control-Control-Not gate. Microelectronics Journal. 35: 471-478.
- [9] Michail E. Kiziroglou, IoannisKarafyllidis. 2003. Design and simulation of a Nanoelectronic single-electron analog to digital converter. Microelectronics Journal. 34: 785-789.
- [10] WasshuberChristoph, Hans Kosina and Siegfried Selberherr. 1998. A comparative study of single-electron memories. Electron Devices, IEEE Transactions on. 45(11): 2365-2371.
- [11] Anbarasu.Paulthurai, Balamurugan.Dharmaraj. 2012. Low-Power and High-Performance 1-Bit Set Full-Adder. Microelectronics and Solid State Electronics. 4: 94-97.
- [12] WasshuberChristoph. 2001. Computational single-electronics. Springer Science and Business Media.
- [13] Rashid Muhammad H. 1990. Spice for Electronics Using PSpice. Prentice Hall PTR.
- [14] Jain Amit, *et al.* 2015. A new SPICE macro model of single electron transistor for efficient simulation of single-electronics circuits. Analog Integrated Circuits and Signal Processing. 82(3): 653-662.