



EVALUATION OF AN T FLIP FLOP USING NEMFET BASED LOGIC

S. Kayalvizhi and C. Karthick

Department of Electronics and Communication Engineering, Sathyabama University, Chennai, India

E-Mail: kayalvzh61@gmail.com

ABSTRACT

In this paper, we introduce a Nano-Electro-Mechanical Field Effect Transistor (NEMFET) based logic flip flops tailored to the implementation of high speed and low energy functional units. Basic flip flops are implemented with NEMFET Logic are analysed and compared against equivalent CMOS realizations. The feasibility of integration of NEM switches into a CMOS process is illustrated by a practical process flow. The application of NEMS logic in T flip flop has advantage in low power consumption, low-energy functional unit. Higher switching activity by reducing number of transistor in the device. This paper proposed an aggressive design technique of NEMFET based flip flops. Which reduce the leakage power comparing with the CMOS device? The implementation result shows that, the NEMFET based logic device are achieving the reduced power dissipation with low power and reduced leakage current which is small and negligible.

Keywords: NEMS, MEMS, delay, power consumption.

INTRODUCTION

The integration of several functional circuits on a chip has been increasing tremendously, which greatly demands the low power operation and reduced short circuit current. Our proposed design will gives the integration of NEMS into the CMOS process. This gives the gives the low power consumption, low energy functional unit, higher switching activity and higher stability over a wide range of temperature, which makes the digital design has efficient, this process and gate NEMS switch design. This provides the reduced short circuit current with minimum delay. In this paper describes the NEMS technology with CMOS device. NEMS technology with CMOS device. NEMS all the switches, which has low- I off point sub-threshold swing, capacitor less memory. The switch operation of controlling NEMS logic, reduces the number of transistor required compared with typical CMOS design. The basic building block of the computer memories possible and it's also used in many sequential logic circuits is the flip flop or bistable circuit. Flip flop are categorized into four types they are SR, JK, T and D flip flops. In this paper we explain about the NEMS technology using T flip flops. This is a complex circuit which can allocate extra memory to adopt the method of tolerating an introduced flip flop design. They may gradually decrease the area of the design. They major barrier of the CMOS technology is an high leakage power and often switching activity. By using NEMS in flip flop is mainly reduced the power dissipation and number of transistor in the device. Our implementation result shows that flip flop design provides the efficient characteristics in case of short circuit current reduction with minimum delay and power consumption.

NEMS TECHNOLOGY

Nano-electro-mechanical switches (NEMS) offer new possibilities for the design of ultra-energy-efficient systems; however, thus far, all the fabricated NEMS devices require high supply voltages that limit their applicability for logic designs. Therefore, research is being

conducted to lower the operating voltages by scaling down the physical dimensions of these devices. However, the impact of device scaling on the electrical and mechanical properties of metal contacts in NEMS devices has not been thoroughly investigated. Such a study is essential because metal contacts play a critical role in determining the overall performance and reliability of NEMS [2].

NEMS transistors have generated a great amount of interest due to their superior sub-threshold behaviour. This is primarily because NEMS offer steep switching characteristics between ON and OFF states and hence, they can effectively eliminate the sub-threshold leakage issue that has troubled CMOS technology for many years. For instance, it has been shown through experiments that micro-scale electromechanical switches can exhibit an incredibly low sub-threshold swing. However, widespread usage of NEMS transistors in logic applications is hindered by the need for high supply voltages because pull-in voltage (equivalent of the threshold voltage for CMOS devices) for current NEMS devices. To overcome this shortcoming, researchers are attempting to reduce the physical dimensions of NEMS in order to reduce the pull-in voltages and consequently, the required supply voltages. However, the scalability of NEMS is predicted to be challenging since the processing techniques for fabricating extremely small NEMS have not been developed yet. More importantly, the impact of scaling on other properties of NEMS devices has not been thoroughly investigated [3].

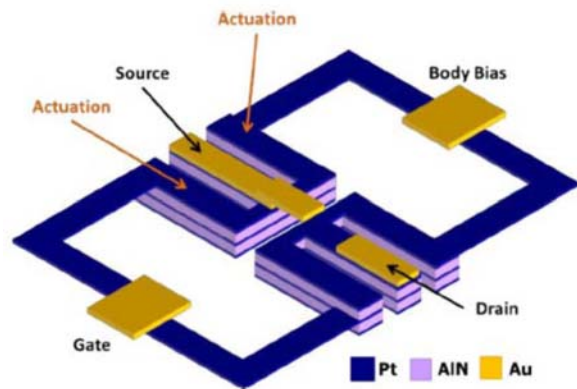


Figure-1. NEMS structure [3].

NEMS DEVICES MODELING

The design of NEMS depends on a thorough understanding of the mechanics of the devices themselves and the interactions between the devices and the external forces/fields. With the critical dimension shrinking from micron to nanometre scale, new physics emerges so that the theory typically applied to MEMS does not immediately translated to NEMS. For example, Vander Waals forces from atomic interactions play an important role in NEMS, while they can be generally neglected in MEMS. The behaviour of materials at nanometre scale begins to be atomistic rather than continuous, giving rise to anomalous and often nonlinear effects, for example [1],

- The roles of surfaces and defects become more dominant.
- The devices become more compliant than continuum models predict.
- Molecular interactions and quantum effects become key issues to the point that thermal

Fluctuation could make a major difference in the operation of NEMS.

Devices of this size and smaller are so minuscule that material defects and surface effects

Have a large impact on their performance. In principle, atomic-scale simulations should well predict the behaviour of NEMS devices. However, atomic simulations of the entire NEMS involve prohibitively expensive computational resources or exceed the current computational power. Alternatively, multi-scale modelling, this simulates the key region of a device with an atomistic model and other regions with a continuum model, can well serve the purpose under the circumstance of limited computational resources. Besides, it has been demonstrated that the behaviour of some nanostructures, like carbon nanotubes, can be approximated by continuum mechanics models, based on the same potentials governing molecular dynamics (MD) simulation, if the surface non-idealities of the nanostructures is neglected. Thus,

continuum mechanics models are still adequate to the design of NEMS, in particular, in the initial stages [1].

NANO-ELECTRO-MECHANICAL SWITCH ACTIVITY

The switch consists of two bridges, a top bridge and a bottom bridge. The input gate G1 and the source of the switch S are on the top bridge. The input gate G2 and the drain of the switch D are on the bottom bridge. A silicon nitride layer with the thickness of 1nm is coated on the surface of G2. The Source and Drain are not connected when potential difference applied between G1 and G2 is less than pull-in voltage $V_{pull-in}$. In this state, the switch is considered to be OFF, as there is no conducting path between Source (S) and Drain (D). The switch conducts when the potential difference between G1 and G2 is greater than the $V_{pull-in}$ voltage. There is a low resistance connection path between Source and Drain terminals. This switch is ON, or conducting, when the voltage on (G1, G2) = {(low, high), (high, low)}. The switch is OFF or non-conducting when the voltage on (G1, G2) = {(low, low), (high, high)}. This switch conducts when the input voltages on G1 and G2 are exclusively different, which example is an XOR function. To prevent the drain-source electrodes from the attraction between the two bridges, their overlapping area is smaller than the gate electrodes. Figure-2 shows the dimensions of the manufactured "XOR" NEMS switch [3]. Maximum all the logic gate function will be changes in the switching activity.

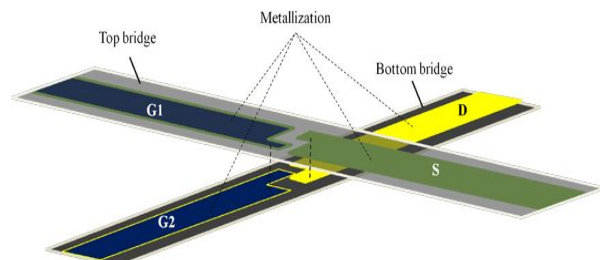


Figure-2. Structure of NEM switch [3].

BASICS OF T FLIP FLOP USING NEMS LOGIC

The T FF is like a JKFF with J and K tied together (K input inverted). Then if $T = 1$, and clock = 1, the ff "toggles" to the opposite state. If $T = 0$, the ff does not change state on the clock "tick." The T FF is a master-slave ff; output changes on the back edge of the clock. Set $T = 1$ permanently, and the T FF toggles on every clock pulse.

In basic T-FLIP FLOP, due to less number of input and output some delay can accrue, whereas NEMFET based T-Flip Flop using double gate with more number of inputs does not increase the delay over a period of time. Maximum logic '0' (switch OFF) and logic '1' (switch ON) function will be defined as logic gate contact (as switching activity) with source and drain in order to activate and deactivate the contact.

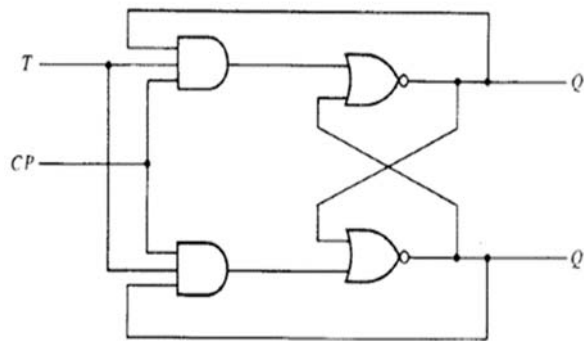


Figure-3. Basic T flip flop [11].

WAVEFORM ANALYSIS OF T FLIP FLOP

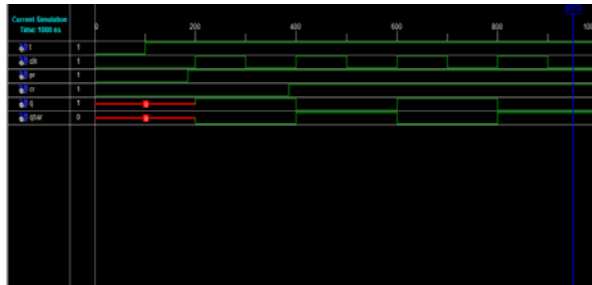


Figure-4. Existing work of basic T- Flip Flop.

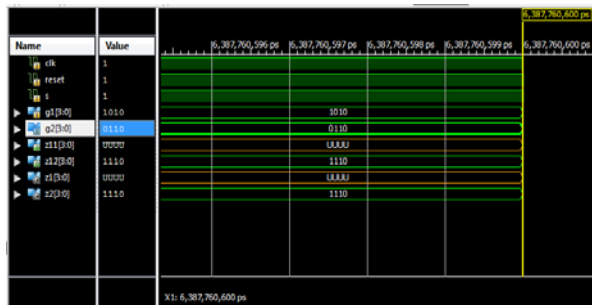


Figure-5. Proposed work of NEMS based T-Flip Flop.

COMPARISON OF NEMS BASE T-FF AND BASIC T- FLIP FLOP

Table-1. Comparison between proposed and Existing work.

Parameters	Proposed	Existing
Power dissipation	1.2mW	3.182mW
Delay	2.076ns	3.182ns

CONCLUSION

The NEMS-CMOS technology is proposed as an alternative to the current CMOS technology, which is troubled by every-increasing leakage power consumption.

The NEMS-CMOS technology integrates NEMS with CMOS devices to combine near-zero leakage characteristics of NEMS switches with high ON current of CMOS transistors and simultaneously offers low-power and high-performance operation. This technology can have interesting implications for mobile applications where low-leakage power consumption and energy efficiency are extremely critical. This can be obtained by CMOS logic of NEMS.

REFERENCES

- [1] Changhong Ke, Horacio D. Espinosa. 2005. Nanoelectromechanical Systems and Modeling. ISBN: 1-58883-042-X/\$35.00, Copyright c 2005 by American Scientific Publishers.
- [2] Hamed F. Dadgour , Muhammad M. Hussain , Alan Cassell, Navab Singh and Kaustav Banerjee. Impact of Scaling on the Performance and Reliability Degradation of Metal-Contacts in NEMS Devices. 978-1-4244-9111-7/11/\$26.00 ©2011 IEEE.
- [3] SIJING HAN. 2013. Design and Modelling Environment for Nano-Electro-Mechanical Switch (Nems) Digital Systems.
- [4] ji hum, kim. 2013. Near Zero Sub-threshold Swing Nano-Electro-Mechanical Field Effect Transistor with Suspended Ge/Si Core/Shell Nanowire Chanel.
- [5] Sijing Han. 2013. Design and Modeling Environment for Nano-Electro-Mechanical Switch (Nems) Digital Systems.
- [6] Marius Enachescu, George R. Voicu, Sorin D. Cotofana. Is the Road towards "Zero-Energy" Paved with NEMFET-based Power Management? 978-1-4673-0219-7/12/\$3\00 ©2012 IEEE.
- [7] AntoniosBazigos, Christopher L. Ayala, Sunil Rana, Daniel Grogg, Montserrat Fernandez-Bolaños, ChristophHagleitner, Tian Qin, Dinesh Pamunuwa, Adrian M. Ionescu. 2014. Electromechanical design space exploration for electrostatically actuated ohmic switches using extended parallel plate compact model. A. Bazigoset *al.* / Solid-State Electronics. 99, 93-100.
- [8] Ankitjain, A.E.islam and M.A.Alam. On The Electro-Mechanical reliability of NEMFET as an Analog/Digital Switch. alam@purdue.edu.
- [9] A.M.Ionescu, D.Tsamados. 2008. Nano-Electro-Mechanical Switches. June 9th.



- [10] VaishaviRanganathan. 2013. Silicon Carbide Nems Logic and Memory for Computation at Extreme: Device Design and Analysis.
- [11] <http://www.wikipedia.org>.
- [12] Hamed F.Dadgour and Kaustav Banerjee. 2007. Design and Analysis of Hybrid NEMS-CMOS Circuits for Ultra Low-Power Applications.
- [13] Marius Enachescu, Mihai Lefter, Antonios Bazigos, Adrian M. Ionescu and Sorin Dan Cotofana. Ultra Low Power NEMFET Based Logic. 978-1-4673-5762-3/13/\$31.00 ©2013 IEEE.
- [14] Hamed F.Dagour and kaustav Banerjee. 2007. Design and analysis of the hybrid NEMS –CMOS circuits for ultra low-power application.
- [15] Mariouseenachescu,george R. viocu and sorin D.cotofana. Leakga-enhancement 3D-stacked NEMFET-based power management architecture for autonomous sensors system.