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DESIGN AND ANALYSIS OF COMPETENT ARITHMETIC AND LOGIC UNIT FOR RISC PROCESSOR

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ABSTRACT

The Arithmetic and Logic Unit is one of the key module in digital signal processors. All the digital domain based technology depends on the operations performed by ALU. Therefore there is a need to design an efficient ALU. ALU consists of arithmetic unit and Logical unit. Arithmetic unit is designed using multiplier adder etc. The multiplier in the proposed work is designed using a unique tree structure which has lesser delay. The adder unit used is Knowles adder which is a parallel prefix adder and has lesser delay compared to other known prefix adders. The proposed work is better in terms of delay. A trade off has been made between area and delay in the proposed design. The savings of power for most power effective architectures range from 19.38% to 33.87%. The proposed design is described using Verilog hardware description language. For Synthesis of the design Cadence RTL compiler has been used.

Keywords: RISC processor, cadence, arithmetic and logic unit (ALU), knowles adder, vedic multiplier.

1. INTRODUCTION

One of the key components of any processing unit is the computation unit. The computations performed in any processor are Addition, Multiplication, Division, Subtraction and also performs logical operations like And, Or, Xor, Nand, Nor etc. ALU is called as heart of a Microprocessor. The block diagram of ALU is shown below in Fig1. Here the ALU is designed using arithmetic unit, logical unit, multiplexer and D-Flipflop.

The logic depth of Brent Kung adder is 2 log2n-1 with a maximum fan out of 2 and it uses only one wire track. Whereas the logic Depth of Knowles adder is much lower than the Brent Kung adder. The comparision of the logic levels and their maximum fan outs of various parallel prefix adders are shown in Table-1.

Vedic Multiplier is known to have lesser complexity and lower power consumption [5, 15]. The Vedic multiplier in this work is based on a vedic sutra (Urdhava Tiryabhyam) which is a vertically crosswise multiplication.

In this paper, the implementation of ALU is done using a Vedic multiplier implemented using Ladner Fisher adder and the adder used for addition is Knowles adder. A delay of 9.006ns is obtained for the proposed work which has lesser delay compared to other Arithmetic and logic units [3]. The Power consumption obtained was 2.1mW which is lesser than the existing work.

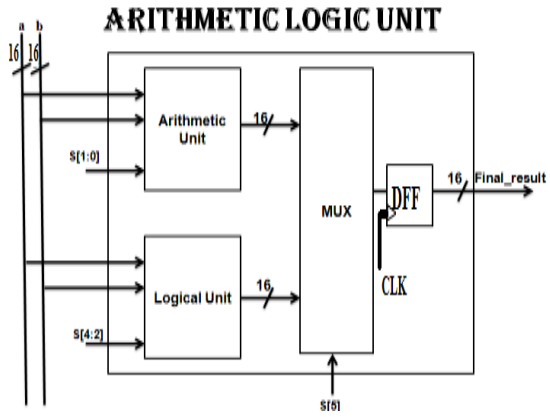

Figure-1. ALU block diagram.

The rest of the paper is as follows: Section (II) consists of existing work, Section (III) comprises of proposed work, Section (IV) has results and comparision, Section (V) has conclusion and future work.

2. ADDERS AND MULTIPLIERS

Parallel-prefix structures are found to be common in high performance adders because of the delay is logarithmically proportional to the adder width [3, 14]. Such structures can usually be divided into three stages, pre-computation, prefix tree and post-computation.

A. Ladner-Fisher adder

Fisher and Richard Ladner introduced a parallel algorithm for efficient computation of prefix sums. Ladner Fisher is one the Parallel prefix adders [5, 11]. A trade off between logic depth and number of nodes has been made with their construction. Its Logic depth is calculated using $O(\log^2_n)$, where n is the number of bits. The Ladner Fisher adder is as shown in Figure-2.

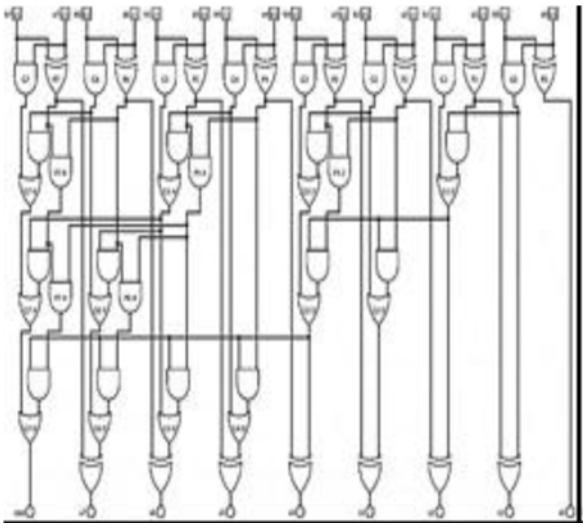

Figure-2. Ladner Fisher adder.

B. Knowles adder

Knowles adder makes a trade off between logic depth and interconnect area. Knowles adder. This adder is similar to Kogge Stone adder [13]. The only difference is that the last stage wiring complexity is reduced to half. The drawback of Kogge Stone adder implementation is routing complexity and larger area consumption.

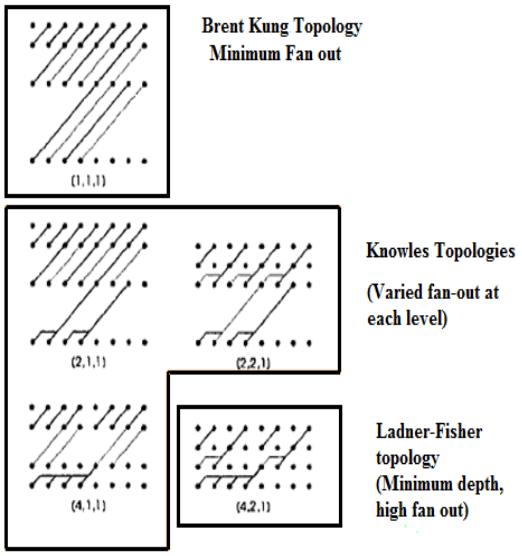

Figure-3. Knowles adder.

C. Vedic algorithm

This algorithm is based on Urdhava Tiryakbhyam sutra which means vertically and crosswise multiplication. The efficiency of any digital circuit depends on the multiplier used, as the multiplication takes more computation time. If the computation time of the multiplier is reduced the overall efficiency in terms of delay as well as power can be improved. The algorithm is computed as shown in below Figure-4.

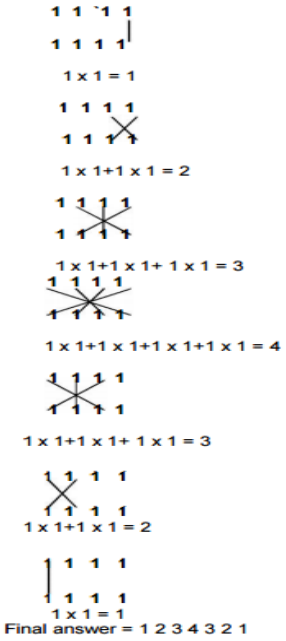

Figure-4. Vedic algorithm.

The multiplier in this paper was designed by using vedic mathematics and Ladner Fisher technique. This multiplier is more efficient when compared with conventional vedic multiplier [12]. Vedic multiplier implemented with Ladner Fisher adder has lesser complexity and is more efficient in terms of delay and power consumption.

The Brent Kung adder is the extreme boundary case of:

1) Maximum logic depth in PP adders (implies longer calculation time).

2) Minimum number of nodes (implies minimum area).

D. Brent Kung adder

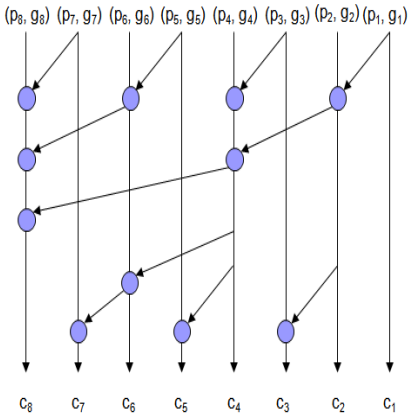

Figure-5. Brent Kung adder.

E. Comparison of Parallel prefix adders

Table-1. Comparison of Parralel prefix adders.

Type	Logic levels	Max fan-out	Wire tracks
Brent-Kung	2log2n -1	2	1
Sklansky	log2n	n=2 + 1	1
Han-Carlson	log2n + 1	2	n/4
Modifed Han-Carlson	log2n + 0.5	2	n/4
Ladner-Fischer	log2n + 1	n/4 + 1	1
Modified Ladner-Fischer	log2n + 0.5	n/4 + 1	1

3. PROPOSED ARITHMETIC AND LOGIC UNIT

The structure of designed Vedic Multiplier is based on a unique technique of multiplication which is different from the conventional way of multiplication such as add and shift. Here modular (smaller) blocks are used to design the complex one. Verilog Hardware Description Language is used for the design of vedic multiplier. The functionality of each block is verified using simulation software i.e. ModelSim. The design of 16x16 bit multiplier using four 8x8 bit multiplier blocks and two 16 bit Ladner Fisher adder blocks is shown in Figure-7. In the last stage two adders are necessary two add the outputs of 8x8 multipliers to get 32 bit product. High speed architecture for multiplication is obtained by combining the features of Vedic multiplier and Ladner Fisher adder which is considered to be the fastest multiplier and adder of the time. The speed has been improved by 2ns compared with the conventional Vedic Multiplier.

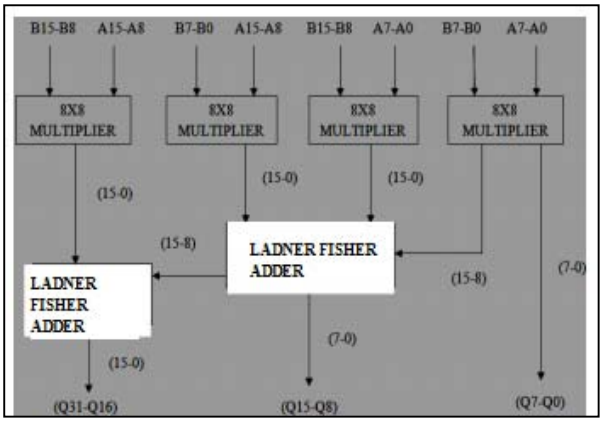

Figure-6. Vedic multiplier with Ladner Fisher adder.

The Arithmetic and Logic unit in this paper is designed using Knowles adder. The Multiplier is designed using a Vedic multiplier which in turn implemented by Ladner fisher adder. The delay is reduced by more than 2ns compared to the existing work. The logic delay is 3.6ns and the route delay is 4.286ns. The power dissiption of the proposed work is obtained as 2.1 mW. The block diagram of the proposed ALU is as shown below.

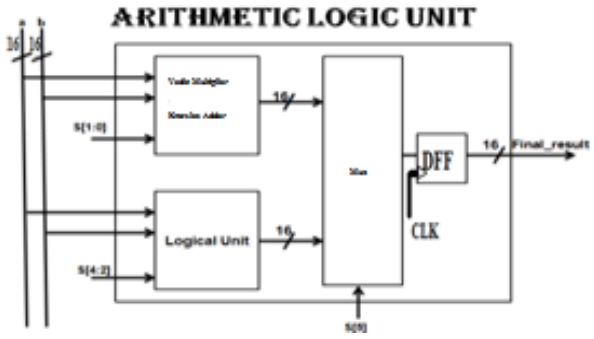

Figure-7. Block diagram of proposed ALU.

4. PERFORMANCE ANALYSIS

Table-2 discusses about the delay and power analysis of the adders. It is clear from the table that the power and delay was lesser for modified Knowles adder.

Table-2. Delay and power analysis of adders.

Parallel Prefix adders	**Power** (nW)	**Delay** (ns)
Brent Kung Adder	10000.342	15.687
Knowles Adder	9993.106	14.452
Modified Knowles adder	8886.989	13.369

Table-3. Delay analysis of proposed ALU.

Parameters	Existing ALU	Proposed ALU
Logic Delay	4.079ns	3.600ns
Route Delay	5.387ns	4.286ns
Total Delay	9.466ns	7.886ns

Table-4. Power analysis of proposed ALU.

Parameter	Existing ALU	Proposed ALU
Power	2.4mW	2.1mW

Table-5 discusses about the Delay parameter od modified and the existing vedic multplier. The Vedic multiplier designed with Ladner fisher adder is lesser when compared with existing vedic multiplier.

Table-5. Delay analysis of Vedic multiplier using Ladner Fisher adder.

Parameter	Vedic multiplier using Carry Select adder (8X8)	Vedic multiplier using Ladner Fisher adder (8X8)
Delay(ns)	28.97	26.54

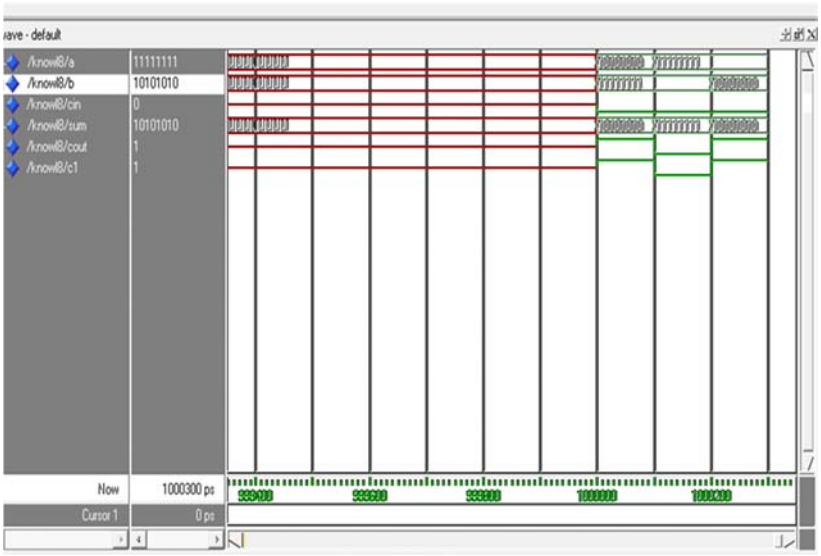

Figure-8. Simulation result for Knowles adder.

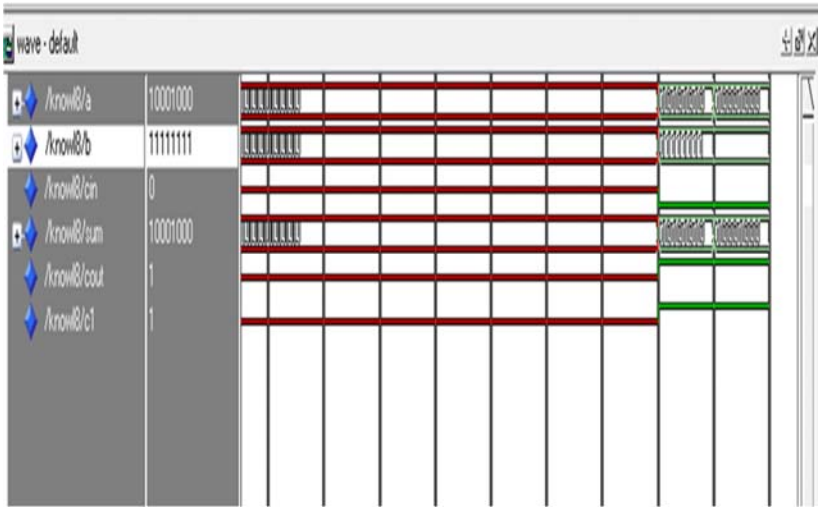

Figure-9. Simulation results for Vedic multiplier using Ladner Fisher Adder.

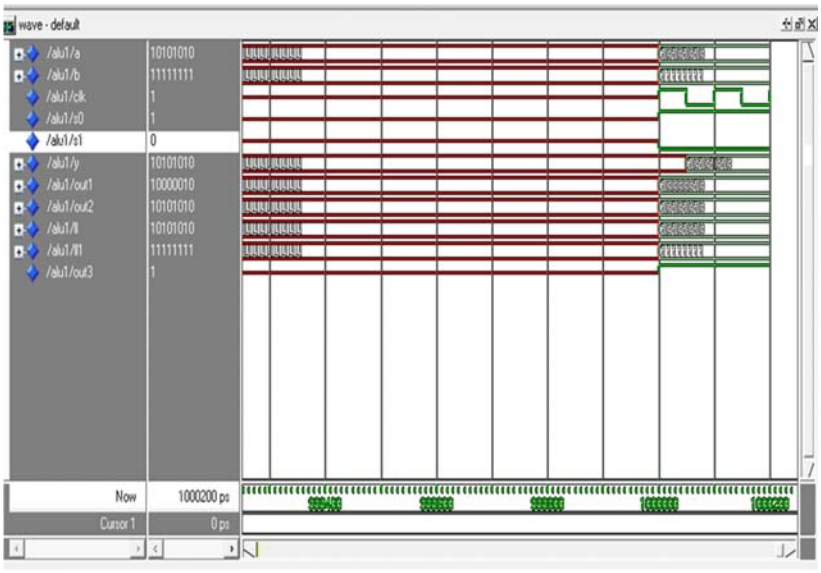

Figure-10. Simulation result for proposed ALU.

From the table3 it is clear that the proposed ALU has lesser logical and route delay compared to the existing work. The logic delay is 3.6ns and the route delay is accounted for 4.286ns. The total delay which is the sum of logic and route delay is 7.886ns which is approximately 3ns lesser than the existing work. The power dissipation has been reduced from 2.4mW to 2.1mW. So, from the results it is clear that the proposed work is more efficient in terms of delay and power.

The Layout diagram of ALU is as shown in Figure-8 obtained from Cadence Virtuso editor.

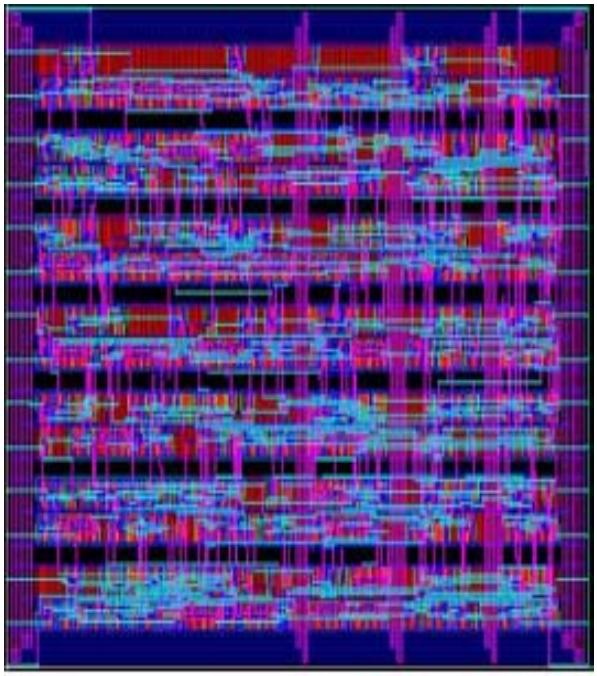

Figure-8. Layout diagram of ALU.

5. CONCLUSIONS

Arithmetic and logic unit is the key module of any processor. So, improving its performance can improve the overall efficiency of the system. Future work can be concentrated on area efficiency of the adder and multiplier and can obtain better efficiency in terms of area. This Arithmetic and Logic unit can be implemented in a processor and can obtain better efficiency for a processor.

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