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COMPREHENSIVE PERFORMANCE ANALYSIS OF LEAKAGE GATE MTCMOS SEQENTIAL CIRCUITS USING SLEEP TRANSISTORS

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ABSTRACT

There exist numerous techniques to reduce power consumption in sequential circuits. Major contributing factor for power consumption in these circuits is the clock and its effective management. To overcome this challenge methods such as clock gating, power gating and multi threshold are adopted in the design of these circuits. Effective implementation of sleep transistor logic also ensures the optimum utilization of the power in a design. This paper emphasizes and analyzes this implementation comprehensively in leakage gate MTCMOS sequential circuits. This work has been carried out on Virtuos platform and the simulation results give the better comparison of performance in various designs. This analysis fixes the challenge of reducing power consumption in sequential circuits in a most comprehensive manner.

Keywords: power consumption, ultra-low power, leakage, sub threshold, MTCMOS.

1. INTRODUCTION

The prime factor for performance in digital circuits is the energy consumed since last two decades with the level of integration touching new scales. Supply voltage reduction also plays a significant role in this attempt and it is more straightforward, when it comes to the CMOS circuits. Scaling is one of the major step towards reduction in power consumption but it in turn increases the static power consumption in most of the cases [1]. ITR study for semiconductors listed power consumption as the key factor in the performance of integrated circuits.

There is another scenario of battery operated portable design and here also lesser energy consumption is the need of the hour. In digital CMOS circuit designs the reduction in supply voltage is a good measure, which is proportional to the energy consumption. This energy factor can be addressed at distinct levels of physical design, namely, architectural, logic, layout and process technology. Especially, in circuit design this is more pertinent to logic style and its optimization [2], [3].

The typical expression for power dissipation is given by $P = C_L V^2 f$. Here, C_L is the load capacitance, V is the supply voltage and f is the operating frequency of the circuit. The cost of the end product increases by improper low power design techniques chosen for the design and also the applications will be hampered in performance. From the past few decades, VLSI design engineers have taken speed as the major performance parameter. Device scaling has offered the needed speed although there is a tremendous increase in functional density in the design. This demanded a trade off in the form of area as well as power consumption. At present, researchers across the globe are having the energy consumption as the major parameter to look while designing a circuit.

Any logic in CMOS design should be brought down to the level of analysis, where the influence of this power consumption in the overall performance of end product is properly addressed. The significant reason is to contain the amount of heat dissipated, while supporting the cause of increasing functional density in the design. Power consumption is not a worrying factor as long as it is not becoming a limiting factor for performance of the logic [4].

2. MULTI THRESHOLD CMOS TECHNOLOGY USING SLEEP TRANSISTORS

Employing distinct threshold voltages for transistors in a design is often referred as the Multi Threshold CMOS technique (MTCMOS). This leads to the optimization of power and delay in the circuit design. V_{th} refers to threshold voltage of the device and it is the key factor in analyzing the performance of a transistor. Transistors with lesser threshold voltage possess higher switching activity are very crucial in assessing the clock periods of the sequential circuit design. The trade off in this way is the static leakage power. The solution is in the form of higher threshold voltage transistors, which are to be used in the non critical paths to compensate the effect caused by the static leakage power. This is well understood know that static leakage reduced by near ten times in the case of high V_{th} transistor designs than in the case of the lower V_{th} designs [1].

MTCMOS technology becomes very impactful with this sleep transistor logic. Here the transistors with low V_{th} and also the lower leakage can be used in the design of core logic and the sleep transistors consists of the higher V_{th}. Sleep transistors isolates the logic cells from the supply power, ground to reduce the leakage in the sleep mode of operation. Here the wake up latency and power plane integrity are the major concerns. Another concerning factor is the duration of the wake up time as it would affect the performance of the VLSI design from the power management perspective. In a power management circuit, the amount of current passing to the ground will be the source of noise, particularly when the sleep transistors are turned ON. There exist a tradeoff between the

transition time from the sleep to active mode and the amount of current going to the ground.

This proposed effective utilization of the sleep transistor in the MTCMOS logic meets the conditions of reducing the threshold voltage of the transistor and also reduces the stand by current. These two are essential to assess the overall performance of a design. MTCMOS has both N channel and P channel transistors with distinct V_{th} values in a chip. Effective power management is feasible with the sleep transistor mode of operation. In the physical design of this technology, it is important to take the large current flowing through these transistors (active mode) into consideration. Channel width is another factor to be looked for in this case. Here exists a tradeoff between the local and global sleep transistors. The challenge with the local sleep transistors is in the form of larger area overhead [10]. MTCMOS implementation with the effective usage of sleep transistor mode becomes more crucial in sequential circuit designing, whereas it is less challenging in the combinational circuit design. This challenge can be dealt by using the complex timing method or additional circuitry should be added, this in turn may result in the performance degradation.

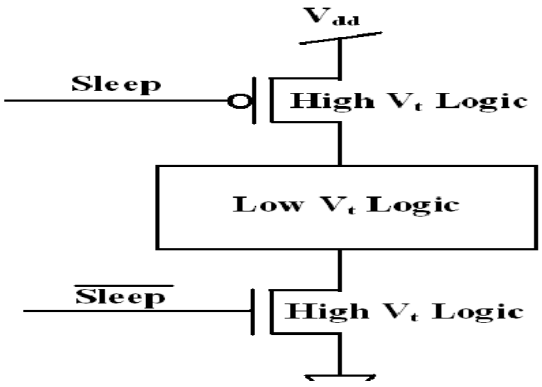

Figure-1. Multi-Threshold CMOS technique.

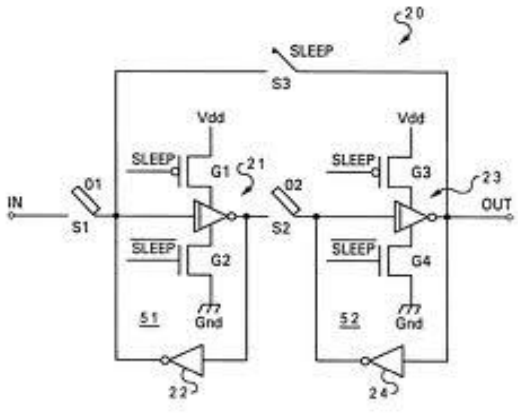

Figure-2. MTCMOS with sleep transistor mode.

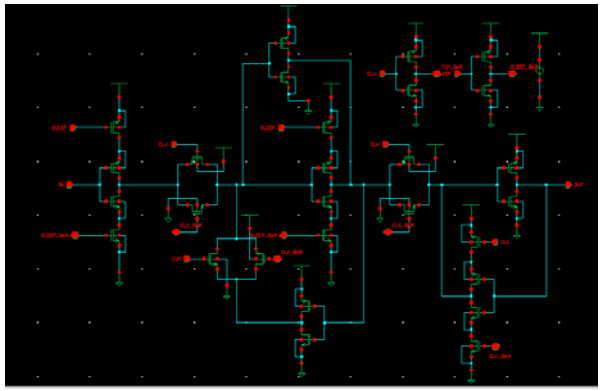

Figure-3. MTCMOS circuit structure.

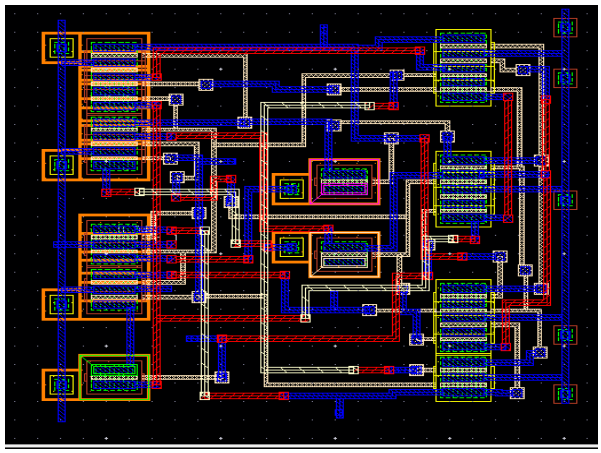

Figure-4. MTCMOS Layout.

The only issue in this method of using sleep transistors in this technique is the transistor sizing to be done carefully. Otherwise, it results in the performance degradation of MTCMOS design when compared with the CMOS circuits.

3. DESIGN OF LEAKAGE FEEDBACK D FLIPFLOP USING THE PROPOSED METHODOLGY

In general, a flip flop is used to store the information with two stable states of operation. These are the rudimentary elements of any digital system of a larger scale of integration. When these are used for infinite storage, the response of the system not only depends on the present inputs but also on the present state. A typical flip flop has two inputs, a clock and two responses. One of the response is normal and the other is the complement of it [7] [8].

Power consumption in memory circuits is crucial as the functional density of the transistors is higher and there are many methods to contain this have been addressed by various researchers [5] [6]. The dynamic power consumption increases with the switching activity and is the major contributing factor in the sequential circuits. The impact of scaling should be well analyzed in this context as the sub threshold leakage current becomes

crucial. Methods are needed to control this leakage current as it is very much evident from the following relation:

$P = P_{dynamic} + P_{short\ circuit} + P_{leakage}$.

Here, $P_{dynamic} = \alpha CV^2f$ and $P_{short\ circuit} = I_{short\ circuit} V_{dd}$. Whereas, $P_{leakage} = I_{leakage} V_{dd}$. Taken all these factors into consideration several methods are proposed to reduce the power consumption in sequential circuits.

Multi-Threshold CMOS using sleep transistors technique lessens the leakage power. To reduce leakage power in MTCMOS circuits, sleep and sleep bar transistors are operated with high threshold voltages. The high threshold mode in MTCMOS technique controls the leakage power and low threshold mode increases the speed performance. When sleep input is OFF and sleep bar input is ON, there is no current flowing in the low threshold voltage circuit. When sleep is ON and sleep bar is OFF then the circuit works in normal mode. MTCMOS technique employing leakage feedback gate and sleep transistor mode of operation is represented in the Figure-5.

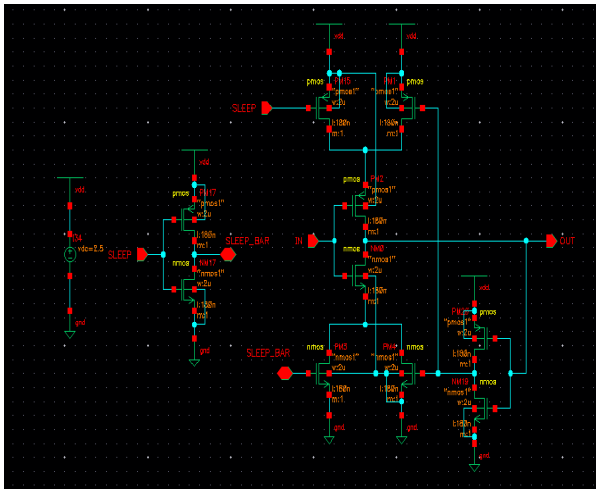

Figure-5. Leakage feedback gate.

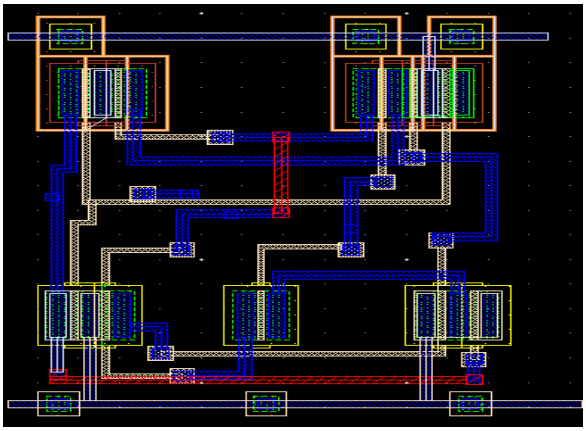

Figure-6. Layout of the leakage feedback gate.

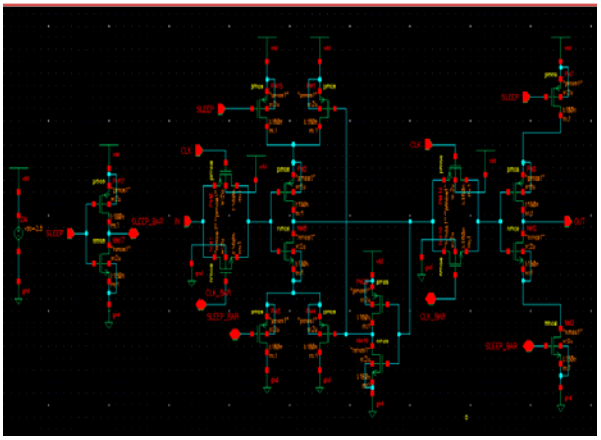

Figure-7. Leakage feedback MTCMOS flip flop.

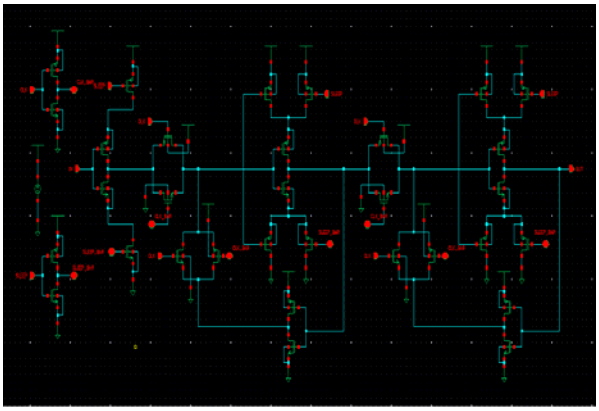

Figure-8. Leakage feedback based MTCMOS dynamic flip flop.

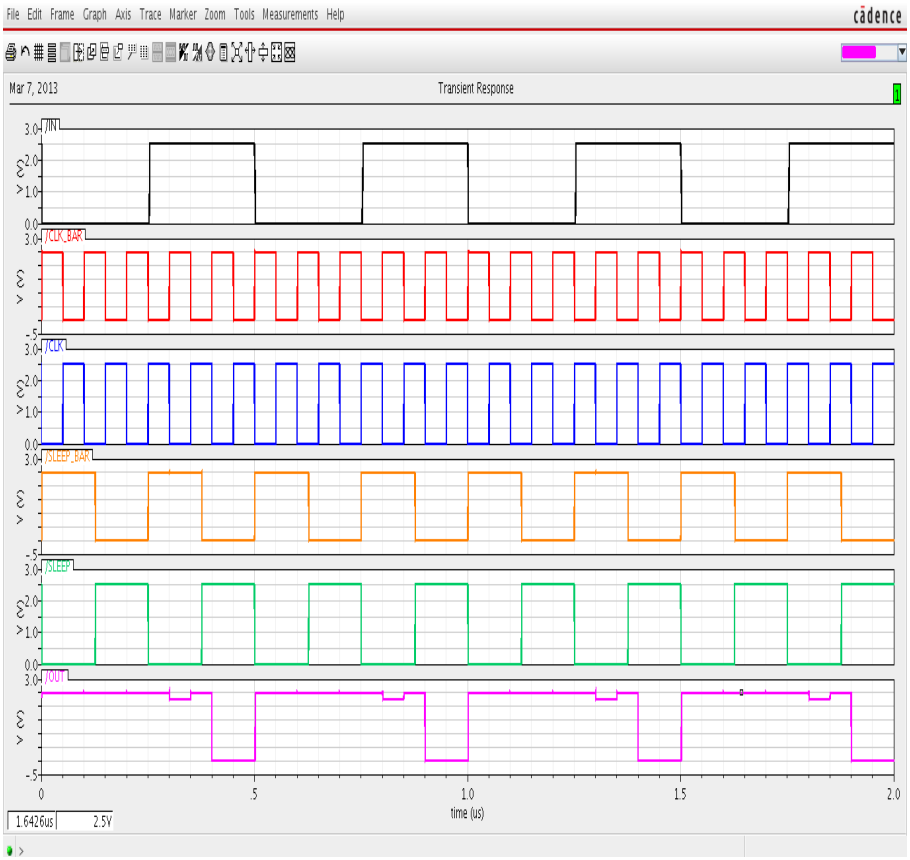

Figure-9. Output waveforms of MTCMOS.

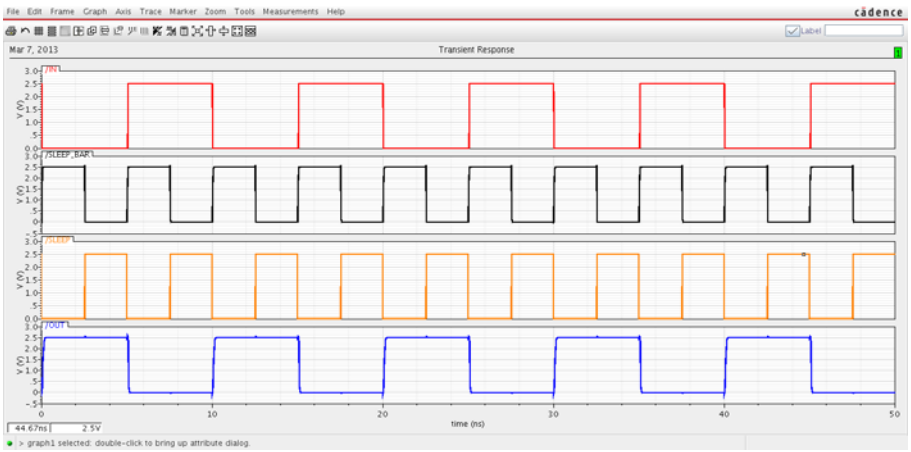

Figure-10. Output waveforms of leakage feedback gate.

4. RESULTS AND CONCLUSIONS

Because leakage currents will be large, when using low V_{th} devices, the clock period must be made fast enough such that the node voltages can be stable over the clock periods of interest.

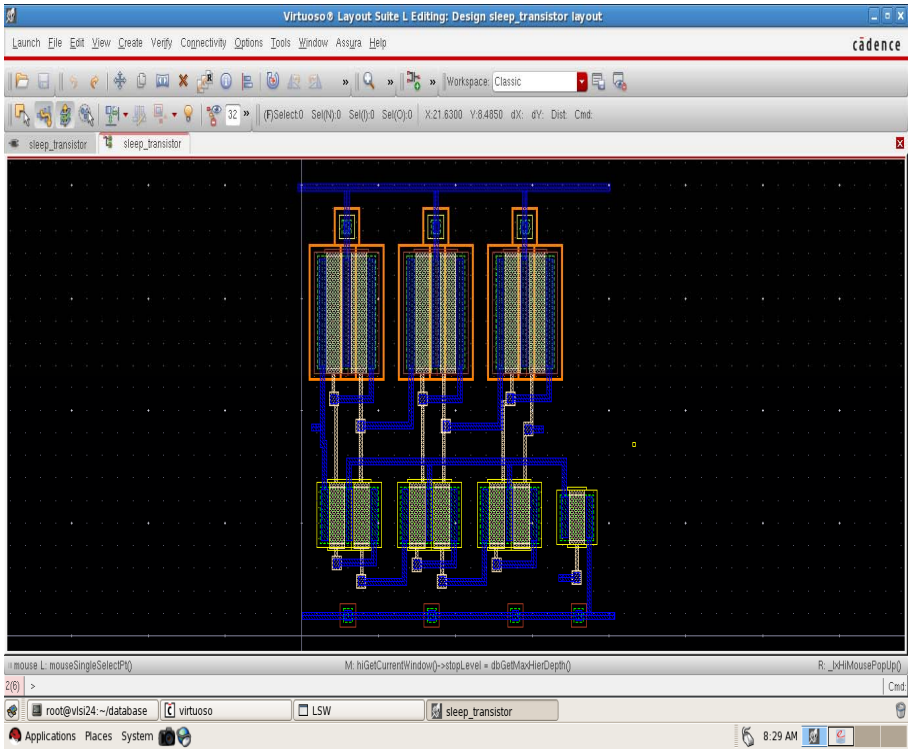

Figure-11. Layout of the sleep transistor mode of operation in MTCMOS technique.

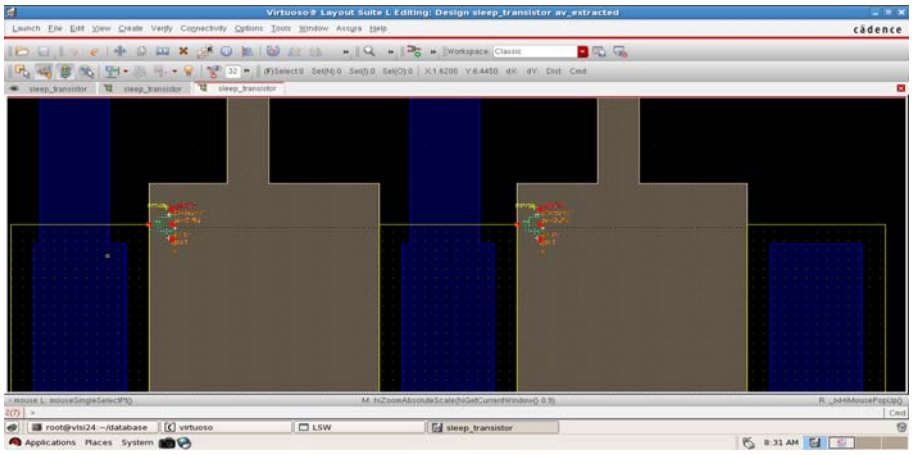

Figure-12. Internal transistor parasitic.

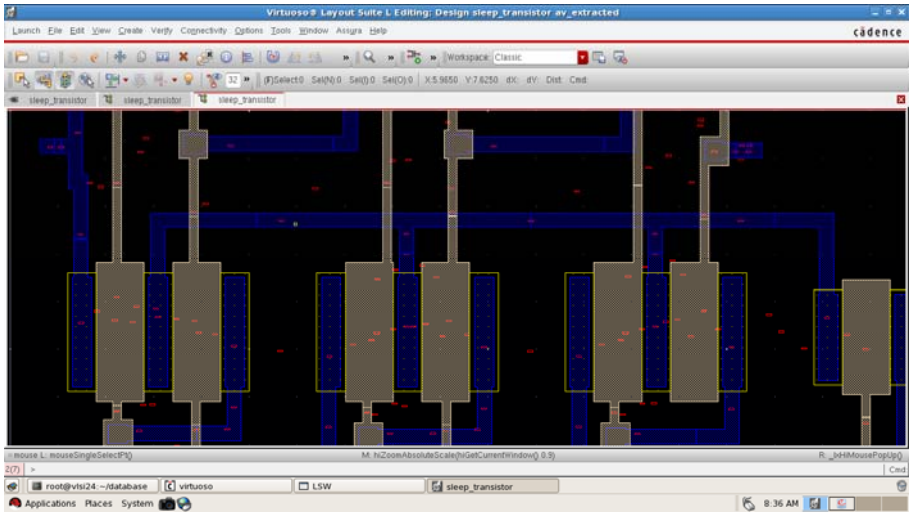

Figure-13. Internal parasitic of resistance and capacitance in transistors.

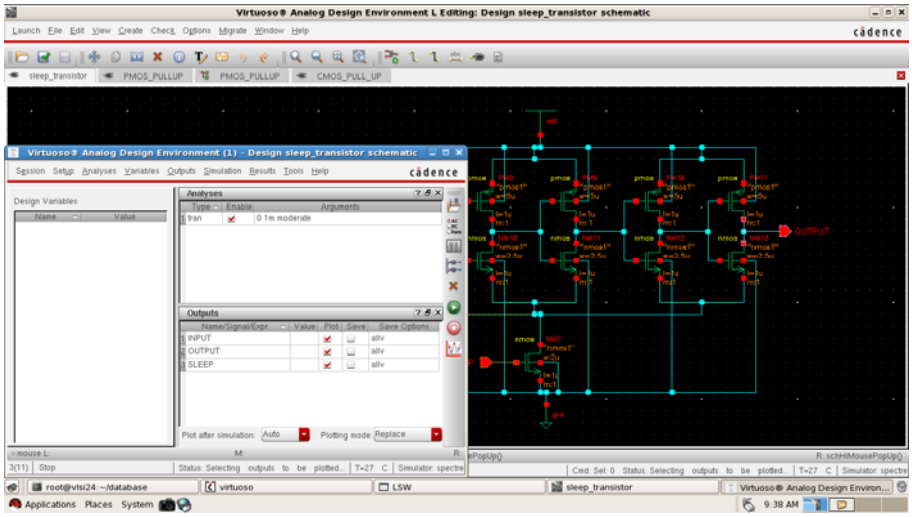

Figure-14. Simulation of the sleep transistor.

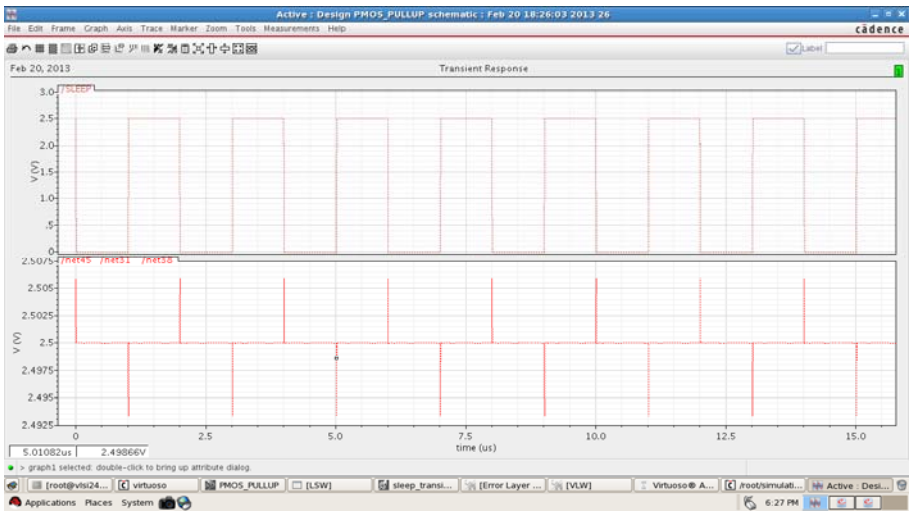

Figure-15. Output waveform sleep transistor.

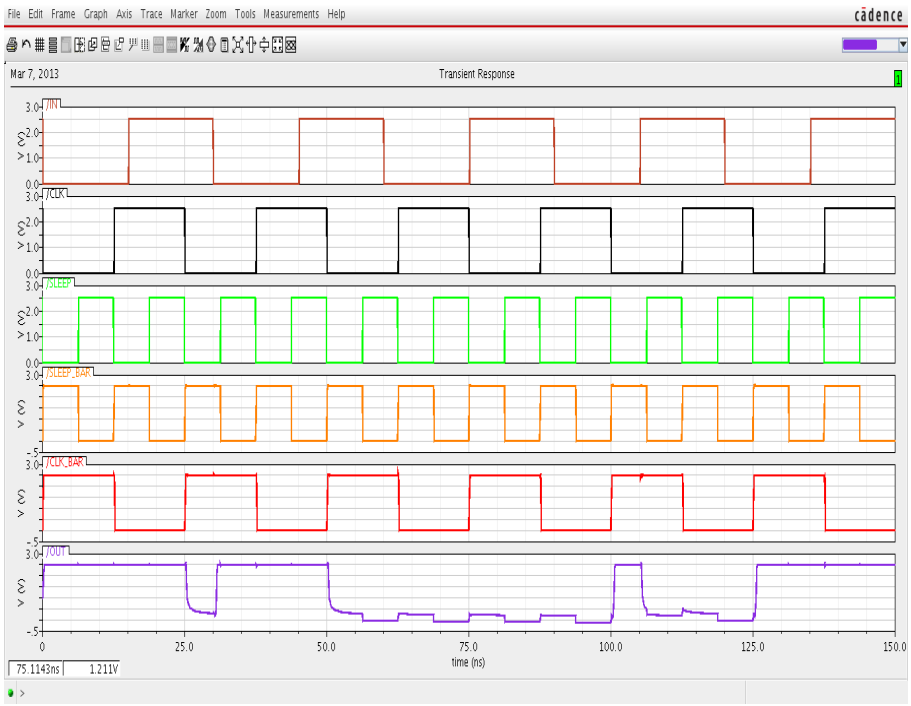

Figure-16. Leakage feedback MTCMOS flip flop using proposed methodology.

5. CONCLUSIONS

A detailed analysis of the MTCMOS implementation with the sleep transistor mode and its impact has been carried out. MTCMOS is very effective in static logic and made reasonably well in performance with the sleep transistors in sequential circuit design also. The layout of the sleep transistor mode of operation is also obtained. RC extraction has been carried out and the internal parasitic elements were obtained. An analysis of leakage feedback in a D flip flop is carried out and the transistor sizing importance is discussed. By using local sleep devices of both polarities, all sneak leakage paths, can be eliminated in the sequential circuits. This detailed analysis would pave the way for the exploration of further methodologies towards reducing the power consumption with all the challenges of the digital circuit design that comes in terms of clock management and leakage current.

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