VOL. 11, NO. 13, JULY 2016 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

ANALYSIS AND SIMULATION OF LOW POWER ALU DESIGN BY USING MODIFIED GDI TECHNIQUE IN MICROCHIP APPLICATION

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ABSTRACT

Power dissipation incorporates a major impact whereas we have a tendency to area unit coming up with any circuit. Since this issue plays a serious role when deciding the potency of the designed circuits i.e. while during this paper we have a tendency to area unit proposing an inspiration for sequent circuits in order that we will scale back the facility dissipation. Power dissipation that successively reduces the complete power dissipation of electronic equipment. During this paper, we have a tendency to plan a reduced power 1-bit full adder (FA) with 10-transistors and this can be employed in the look ALU. The planned style consists of GDI adder based mostly on mux circuits. By exploitation low power 1-bit full adder within the implementation of ALU, the facility and space area unit greatly reduced to quite five hundredth compared to traditional style and half-hour compared to transmission gates. So, the look is attributed as a neighbourhood economical and low power ALU .In this, ALU consists of 4x1 electronic device, 2x1 electronic device and full adder calculated to implement logic controls, like AND, OR, etc. and arithmetic operations, as ADD and cypher. GDI cells area unit employed in the look of multiplexers and full adder that area unit then associated to understand ALU. The simulation results are finished T-Spice tool with TSMC018 technologies.

Keywords: static power, dynamic power, power dissipation, GDI, modified GDI.

1. INTRODUCTION

ALU is one amongst the most elements of microchip. They use quick dynamic logic circuits and have rigorously optimized structures. Its power consumption accounts for a big portion of total power consumption of information path [1]. ALU additionally contribute to at least one of the Very best power-density locations on the processor, because it is clocked at the very best speed and is unbroken busy most of the time leading to thermal hotspots and sharp temperature gradients at intervals the execution core. Power dissipation is essentially the facility that is regenerate to heat then conducted or radiated removed from the device. Electronic associated electrical devices will have a limit on the present they'll safely handle that's not an electronic limit, however a physical one. For example, a electronic transistor could preferably be ready to handle an exact quantity of current, however it's given a lower current rating as a result of the die gets too hot. Dissipation is typically measured in watts, and uses the same old law calculations for power. Most of the terribly giant Scale IC (VLSI) applications, Full adder circuit is practical building block and most important element of complicated arithmetic circuits like microprocessors, digital signal processors or any ALUs. Nearly each complicated machine circuit needs full adder electronic equipment. The complete machine block power consumption is reduced by implementing low power techniques on full adder electronic equipment. During this paper, from completely different completely different} existed base papers many full adder circuits supported different low power techniques are planned targeting. We've designed ALU in several methods by exploitation GDI cells to implement multiplexers and full adder circuit. The input and output sections include 4x1 and 2x1 multiplexers and ALU is enforced by exploitation full adder.

2. NEW MODOFIED GDI TECHNIQUE

Gate Diffusion Input (GDI) methodology relies on the employment of a straightforward cell. One is also reminded of the quality CMOS electrical converter at the primary look of this circuit, however there are some necessary differences: (1) The GDI cell contains 3 inputs-G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). (2) Bulks of each NMOS and PMOS are connected to N or P (respectively); therefore it may be every which way biased in distinction to CMOS electrical converter. The fundamental GDI cell is shown in Figure-1.

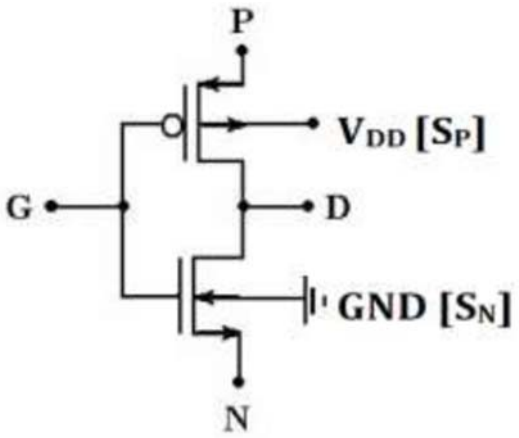

Figure-1. Basic modified gate diffusion input.

2.1 Multiplexer

Multiplexer can acts as a digital switch. Choice line plays a significant role to pick explicit input. If the amount of input lines is „2n" and choice lines are „n"

choice lines. With the „n" choice line the actual „2n" input line are chosen. Figure shows the implementation of 2x1 electronic device and Figure-5 shows the layout of 2x1 electronic devices. The amount of choice lines for 2x1 electronic devices is one choice line. With relation to the choose line the inputs are chosen. Within the same approach 4x1 electronic devices conjointly designed to execute arithmetic and logic unit. The amount of choice lines needed for 4x1 electronic devices is 2 and with relation to the 2 choice lines the four inputs are activated. Figure-3 shows the schematic of 4x1 electronic devices and figure shows the layout of 4x1 electronic devices.

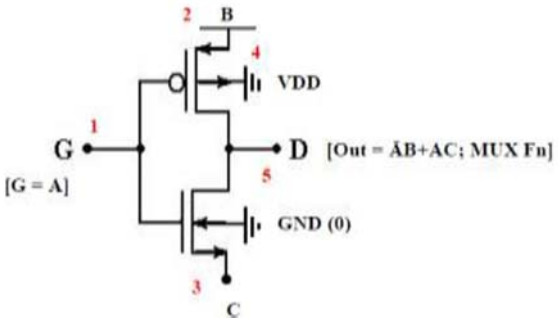

Figure-2. Modified GDI based 2x1 multiplexer.

2.2 XOR Gate

XOR gate is that the main building block of the complete adder and additionally which supplies the total output of the complete adder. The amount of transistors taken to style the XOR circuit is four. That the adder circuit will be improved by reducing the world of XOR circuit. Figure-8 shows the implementation of XOR circuit and Figure-4 shows the layout style of the XOR circuit.

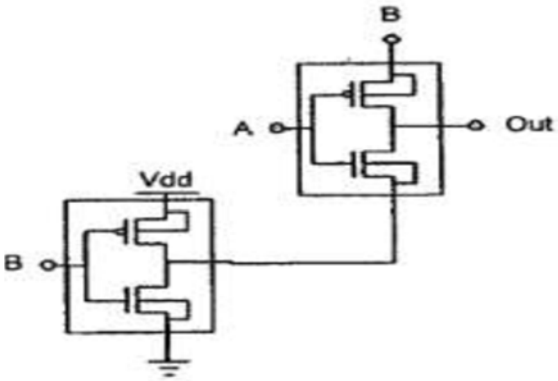

Figure-3. Modified GDI based XOR gate.

2.3 Full adder

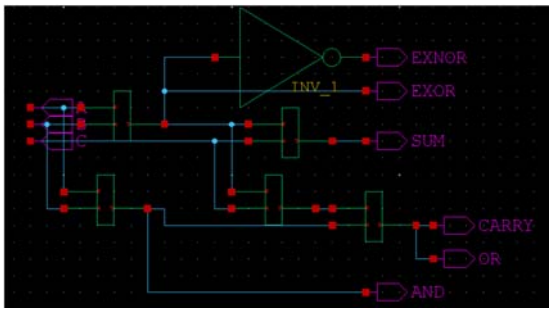

Figure-4. Modified GDI based One bit full adder.

One bit full adder circuit is additionally a crucial block to style Arithmetic and logic unit. Full adder circuit contains 3 inputs and 2 outputs named total and carry. The operation adds just for one bit numbers. the quantity of transistors needed style to style one bit full adder square measure less therefore the space are optimized for the higher performance of arithmetic and logic unit circuit design. Figure shows the implementation of the one bit full adder and Figure-5 shows the layout style of 1 bit full adder.

3. ALU DESIGN

The Arithmetic and Logic Unit (ALU) is that the essential part within the silicon chip it performs all arithmetic like addition, multiplication, subtraction, etc. and logical controls like OR, XOR, AND, NAND. In pc Central process Unit (CPU) is that the brain of the pc and ALU is prime block of CPU. The processor found within Graphical Processor Unit is additionally contains powerful ALU. We have a tendency to style ALU mistreatment full adder and also the electronic device circuits. The complete adder circuits used here is single bit full adder .the electronic device circuit is of 4X1 mux and 2X1MUX. The complete adder circuit's area unit designed PTLGDI logic vogue. The electronic device employed in the ALU is for input choice and to see what kind operation to perform. The electronic device is enforced mistreatment six and 2 transistors .the electronic transistor electronic transistor semiconductor device semiconductor unit semiconductor} count is reduced and power consumption is additionally low compared to pass transistor electronic device. This style is easy in terms of your time and space overwhelming.

The full adder performs the computing functions of ALU. The pass electronic transistor logic reduces the parasitic capacitance and Modified GDI logic increase the speed of the operation.

In existing methodology ALU is intended mistreatment 4X1 mux, 2X1 mux and full adder. The multiplexers were designed mistreatment pass electronic transistor logic. And also the full adder is enforced mistreatment eight transistors. The electronic transistor count is reduced.

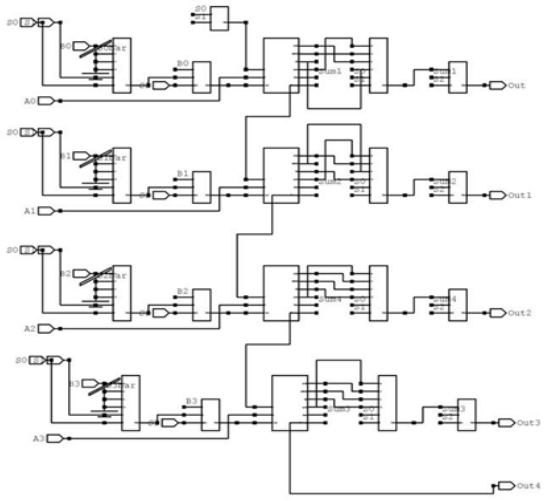

Figure-5. ALU Design.

4. SIMULATION RESULTS

Theses circuits are designed and simulated using Tanner EDA Tool.

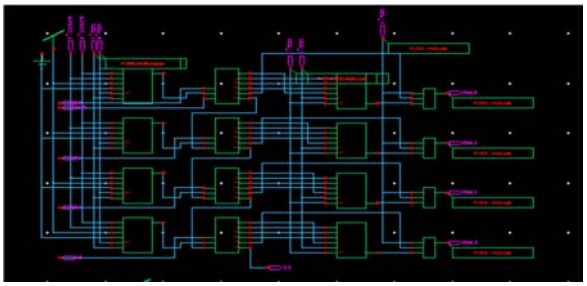

Figure-6. Design of convolution ALU.

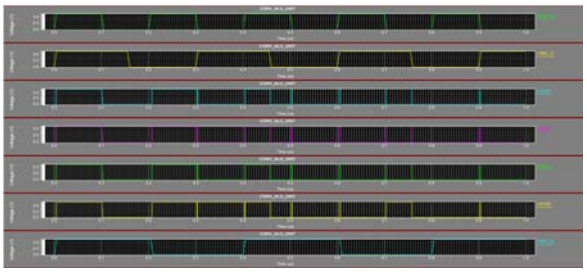

Figure-7. Simulation of convolution ALU.

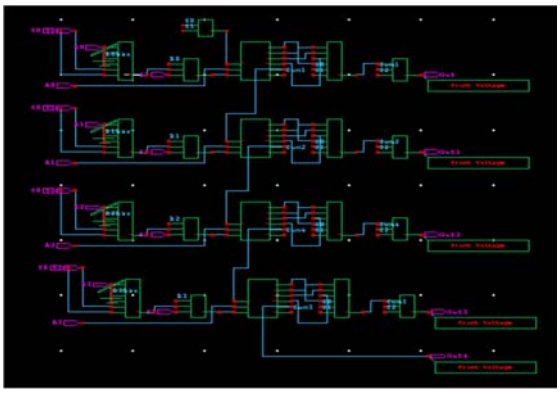

Figure-8. ALU Design of GDI technique.

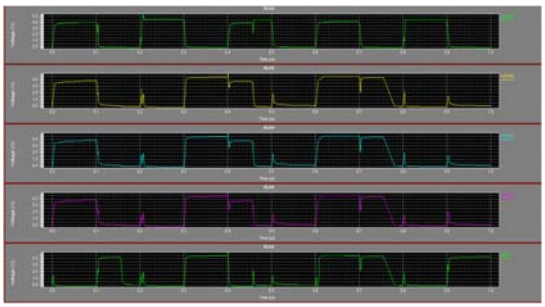

Figure-9. Simulation of GDI technique ALU.

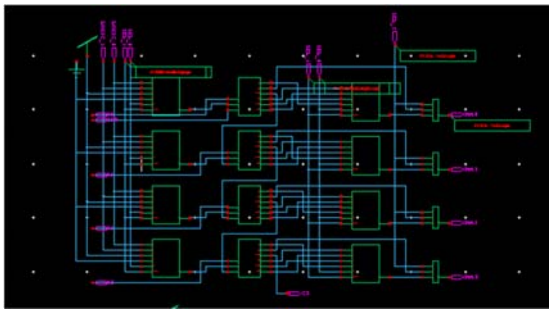

Figure-10. Modified GDI based ALU design.

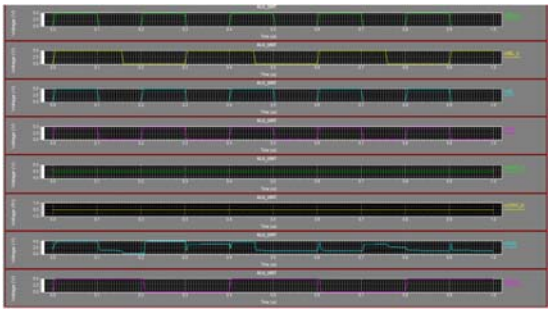

Figure-11. Simulation of modified GDI ALU.

5. PERFORMANCE COMPARISON OF EXISTING AND PROPOSED DESIGN

Type of circuit	Power consumption
Convolution ALU	Average power consumed -> 4.216707e-010 watts Max power 9.220208e-001 at time 3.2046e-009 Min power 5.981470e-008 at time 0
GDI technique ALU	Average power consumed -> 2.951406e-011 watts Max power 1.092607e-001 at time 9.02622e-007 Min power 2.915294e-006 at time 2.00488e-007
Modified GDI ALU	Average power consumed -> 2.415730e-010 watts Max power 1.155156e-001 at time 9.03131e-007 Min power 2.435673e-009 at time 4e-008

6. CONCLUSIONS

Power consumption in CMOS circuit is classed in 2 categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuit's static power dissipation is negligible so not thought of as compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by $P = C_L f V_{dd}^2$. The facility provide is directly associated with dynamic power. The numbers of power provide to ground connections area unit reduced in Modified GDI implementation that reduces the dynamic power consumption. With mistreatment GDI technology coming up with a ALU shopper less space, less power consumption.

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