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RTL LEVEL POWER OPTIMIZATION OF ETHERNET MEDIA ACCESS CONTROLLER

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ABSTRACT

Ethernet is the most popular layer-2 protocol and widely used in Local Area Networks (LAN's) and Metropolitan Area Networks (MAN's). Ethernet connectivity due to its broad existence had become a part of Internet-of-Things (IoT) for gateway solutions. With broader market opportunity there is a need for Ethernet connectivity devices with low power consumption. In this paper, the experimental analysis and results of power consumed by Ethernet MAC design, with and without low power techniques, at Register Transfer Logic (RTL) level are presented.

Keywords: VLSI, ethernet, lowpower, CMOS, IoT, clock gating, gray encoding, binary encoding.

1. INTRODUCTION

The rapidly emerging Internet of Things (IoT) market provides a huge business potential, hence organizations are making huge investment to develop IoT based applications and products. IoT edge devices that perform sensing, monitoring and controlling may need to send this information to remotely located processing elements, through gateway devices that are interconnected using Ethernet technology [1].

These gateway devices that are interconnected to Ethernet, demands not only high performance and smaller foot-print, but also should consume low power.

As more IoT applications are interacting with gateway devices, power consumption has become a key limitation factor. This paper explains about the design of Ethernet Media Access Controller (MAC) and the strategy followed to estimate and optimize the power consumption at RTL level. This paper is organized to have multiple sections. Section II explains about the Ethernet MAC as gateway solution and section III explains about dynamic power dissipation in CMOS integrated circuits. Section IV explains about power estimation and power optimization methodology. Section V shows experimental results obtained and Section VI shows the analysis and comparison of obtained experimental results followed by conclusion in section VII.

2. ETHERNET MEDIA ACCESS CONTROLLER (MAC) AS GATEWAY SOLUTION IN LAN ENVIRONMENTS [1]

Connectivity adds a great value to many embedded applications. For many applications, having ability to attach edge devices to communicate with remote servers and cloud networks through gateway systems like LAN and MAN provides additional benefits, as these systems can be operated and controlled outside the IoT Cloud. Ethernet[1] due to its broader existence has become a most feasible solution for IoT application developers, service providers and OEM manufacturers to transfer the information sensed by edge devices to remote servers or cloud networks through a robust LAN and WAN networks. Due to this, Ethernet is becoming more popular, hence industries and professional bodies have collaborated to improve power consumed by systems that are connected to Ethernet network.

3. DYNAMIC POWER CONSUMPTION IN CMOS

A. Dynamic power dissipation in CMOS integrated circuits

In CMOS integrated circuits, dynamic power dissipation is caused mainly due to Switching Power.

- **Switching power**

Switching power, as shown in Figure-1, is defined as the power dissipated, when the node changes its state, which causes charging or discharging of internal node capacitance and net capacitance.

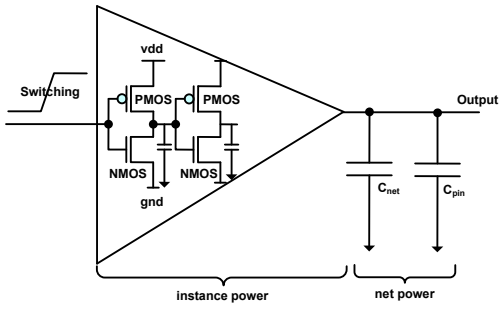

Figure-1. Switching power in CMOS circuit.

Since switching power is a major contributor for dynamic power dissipation, one should aim for reducing switching activity, which leads to reduction in dynamic power, thereby overall reduction in power dissipation that occur in CMOS based designs.

4. POWER ESTIMATION AND OPTIMIZATION METHODOLOGY

Power estimation [4] refers to, estimation of the average power dissipation for the given digital circuit. The commonly used method to estimate average power is to simulate the digital circuit for the desired behavior by driving set of input patterns know as input stimulus. Based upon these input stimulus, the internal nets and gates in the circuit switches its state from one logic level to another logic level. This switching information for all gates and internal nets are captured in a file named switching activity information file (SAIF). The power estimation tool reads in this SAIF file and calculates the dynamic power dissipated for the given digital circuit.

Power optimization refers to the implementation of low power techniques that suits well for the given design, that is expected to reduce the overall power dissipation occur in the circuit.

A. Environment setup to generate SAIF file

The below Figure-2, shows the environment setup [4] used to generate the Switching Activity Information file (SAIF), for the Ethernet MAC design.

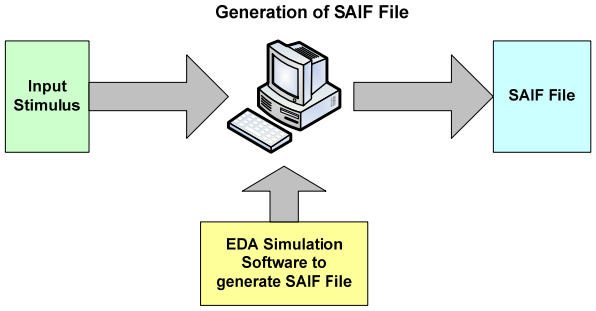

Figure-2. Environment setup to generate SAIF File [4] [5].

The EDA simulation software that generates switching activity information file is installed into the Host computer as shown in Figure-2. The input ports of design-under-test (DUT), whose dynamic power dissipation is to be estimated, are driven by set of inputs for a period of time. ie. A simulation is performed on the given DUT using the given input stimulus for the period of time.

Once the simulation is complete, the EDA simulator generates an output file called Switching Activity Information File (SAIF), which consists of switching activity information captured for all gates and internal nets present in the DUT. This SAIF file once generated will be used by power analysis tool to perform power estimation.

B. Environment setup for power analysis and estimation

The below Figure-3, shows the environment setup [5] used to estimate the power dissipation for Ethernet MAC design. The SAIF file generated using EDA simulator is given as input to the power analysis tool, along with other inputs such as technology library information, power library database and constraints. Based upon these inputs, the power analysis tool, analysis the switching activity of all the gates and nets and calculates the power dissipated due to switching of the gates and internal nets.

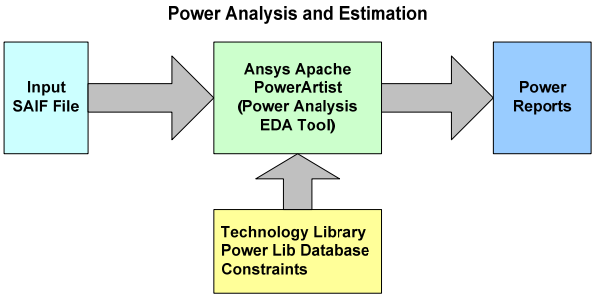

Figure-3. Environment setup to estimate power using Ansys Apache Power Artist EDA tool [3].

Once all analysis and estimates are done, the tool generates an output report with details of power consumed by each gate and net captured in SAIF file.

5. EXPERIMENTAL RESULTS

The Power Estimation for Ethernet MAC design was performed as follows:

A. Power estimation on actual design

Initially the power estimation was done on the actual design, which does not have any low power techniques implemented in it and the obtained results are tabulated.

B. Power estimation on modified design

Once the power estimation was obtained for actual design, then a suitable low power technique for this design namely Clock Gating [6] and Gray encoding of states [7] in a finite state machine were implemented, and again power estimation was done, using the same set of parameters that were used to estimate power in actual design. The power estimation done on actual design and modified design had resulted into *4 different scenarios* and the results obtained in each scenario is tabulated as shown below:

- **Scenario-1: Without clock gating and binary encoding of states in an FSM**

The Power Estimated for scenario-1, for various frame lengths were shown in below Table-1.

Table-1. Without clock gating and binary encoding of states in an fsm [3].

Without clock gating and binary encoding of states in an FSM			
Frame size (in Bytes)	**Power consumption**		
	Static (uW)	**Dynamic** (mW)	**Total** (mW)
64	46.463	2.0043	2.0508
128	46.588	2.1177	2.1643
256	46.564	2.3396	2.3862
512	46.508	2.7899	2.8364
1024	46.586	3.6558	3.7024
1280	46.542	4.093	4.1395
1518	46.676	4.4707	4.5173
1*640	46.494	3.0852	3.1317
10*64	46.487	3.5346	3.5811

- **Scenario-2: Without clock gating and gray encoding of states in an FSM**

The Power Estimated for scenario-2, for various frame lengths were shown in below Table-2.

Table-2. Without clock gating and gray encoding of states in an fsm [3] [7].

Without clock gating and gray encoding of states in an FSM			
Frame size (in Bytes)	**Power consumption**		
	Static (uW)	**Dynamic** (mW)	**Total** (mW)
64	46.463	2.0043	2.0508
128	46.588	2.1177	2.1643
256	46.564	2.3396	2.3862
512	46.512	2.7874	2.8340
1024	46.522	3.6557	3.7022
1280	46.541	4.0863	4.1328
1518	46.675	4.4707	4.5174
1*640	46.514	3.0093	3.0558
10*64	46.522	3.5189	3.5654

- **Scenario-3: With clock gating and binary encoding of states in an FSM**

The Power Estimated for scenario-3, for various frame lengths were shown in below Table-3.

Table-3. With clock gating and binary encoding of states in an fsm [3] [6].

With clock gating and binary encoding of states in an FSM			
Frame size (in Bytes)	**Power consumption**		
	Static (uW)	**Dynamic** (mW)	**Total** (mW)
64	46.465	2.0027	2.0492
128	46.592	2.1153	2.1619
256	46.567	2.338	2.3846
512	46.510	2.7883	2.8348
1024	46.522	3.6559	3.7024
1280	46.520	4.0909	4.1374
1518	46.678	4.4690	4.5157
1*640	46.517	3.0077	3.0542
10*64	46.523	3.5173	3.5638

- **Scenario-4: With clock gating and gray encoding of states in an FSM**

The Power Estimated for scenario-4, for various frame lengths were shown in below Table-4.

Table-4. With clock gating and gray encoding of states in an fsm [3] [6] [7].

With clock gating and gray encoding of states in an FSM			
Frame size (in Bytes)	**Power consumption**		
	Static (uW)	**Dynamic** (mW)	**Total** (mW)
64	46.516	2.0044	2.0509
128	46.592	2.1153	2.1619
256	46.566	2.3381	2.3846
512	46.515	2.7859	2.8324
1024	46.526	3.6532	3.6998
1280	46.544	4.083	4.1296
1518	46.677	4.4691	4.5157
1*640	46.517	3.0077	3.0542
10*64	46.523	3.5173	3.5638

6. ANALYSIS AND COMPARISON OF RESULTS

In this section, the power estimation results for four different scenarios specified in section V are analyzed and a graph is plotted to make a comparative analysis of power dissipated under each of the scenarios as shown below:

A. Without clock gating vs with clock gating

The below Figure-4, shows a graph plotted for *dynamic power* dissipated for various sizes of frame length.

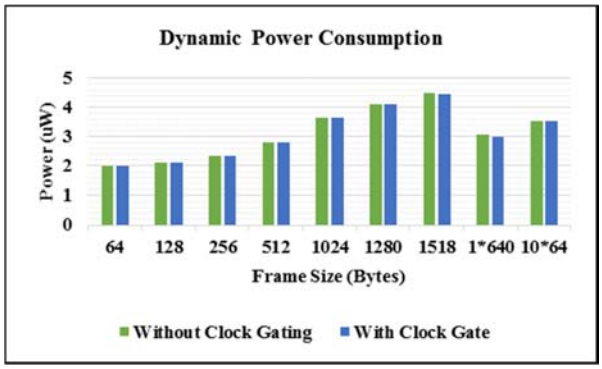

Figure-4. Dynamic power dissipation [3] [6].

From the above Figure-4, we observe that dynamic power has reduced by 0.379% for the design that

has clock gating when compared against the actual design that does not have clock gating.

The below Figure-5, shows a graph plotted for *total power* dissipated for various sizes of frame length.

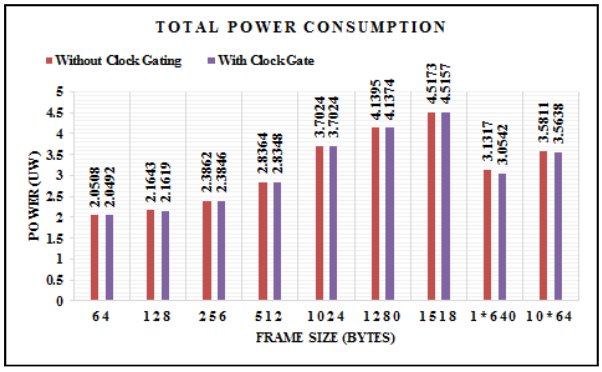

Figure-5. Total power dissipation [3].

From above Figure-5, we can observe that, the total power dissipation has improved by 0.372% for the design with clock gating. i.e.). The total power dissipation occurred for a design with clock gating is comparatively less than the design without clock gating. From the graph, we can also observe that there is a significant improvement in power dissipation for short size frames; say for example, frames of length 64Bytes. The power dissipation may further improve, when the application layer demands to send more number of such small size frames back to back.

B. Binary encoding vs gray encoding

The below Figure-6, shows a graph plotted for *dynamic power* dissipated for various sizes of frame length.

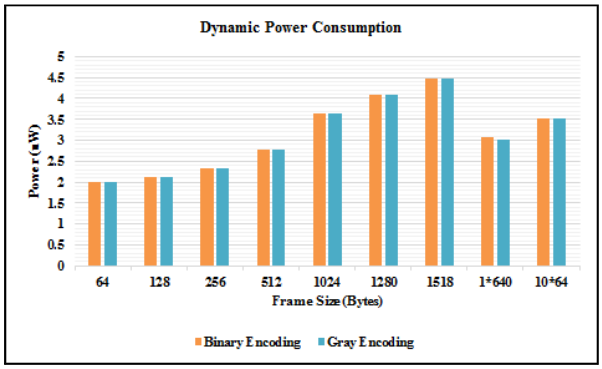

Figure-6. Dynamic power dissipation [3][7].

From the above Figure-6, we observe that there is no change in dynamic power dissipation for frames having size less than 512Bytes, for both designs that have implemented binary and gray encoding techniques. But for frame size of length greater than 512Bytes, the dynamic power dissipation has reduced by 0.52% for the design that has implemented gray encoding technique.

The below Figure-7, shows a graph plotted for *total power* dissipated for various sizes of frame length.

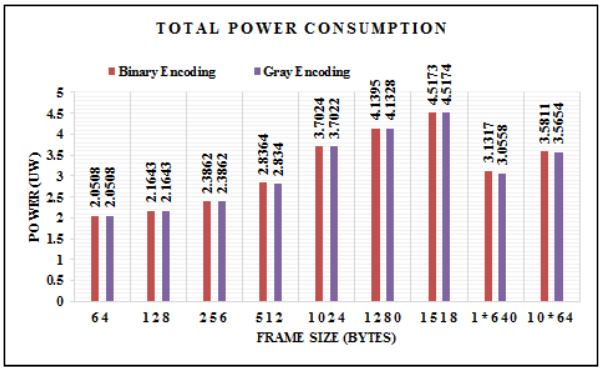

Figure-7. Total power dissipation [3].

From above Figure-7, we can observe that, the total power dissipation has improved by 0.34% for frames of size above 512Bytes for the design that implements gray encoding technique. For frames of smaller sizes, there is no change in power dissipation for both the designs that implements binary encoding and gray encoding. This power reduction may further improve when the application layer demands to send a mixed sized frames.

C. Without clock gating and binary encoding vs with clock gating and gray encoding

The below Figure-8, shows a graph plotted for *dynamic power* dissipated for various sizes of frame length.

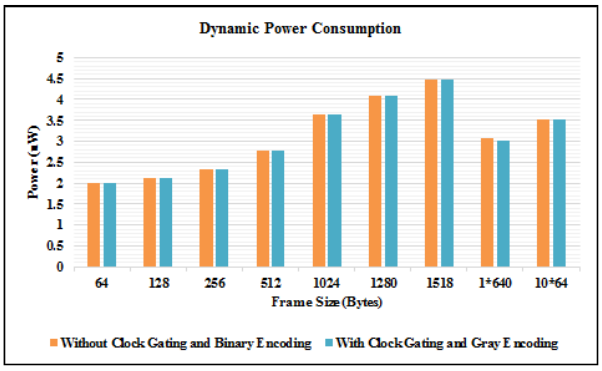

Figure-8. Dynamic power dissipation [3] [6] [7].

From the above Figure-8, we observe that the dynamic power dissipation has improved by 0.40% for all size frames for the design that implements both clock gating and gray encoding techniques.

The below Figure-9, shows a graph plotted for *total power* dissipated for various sizes of frame length.

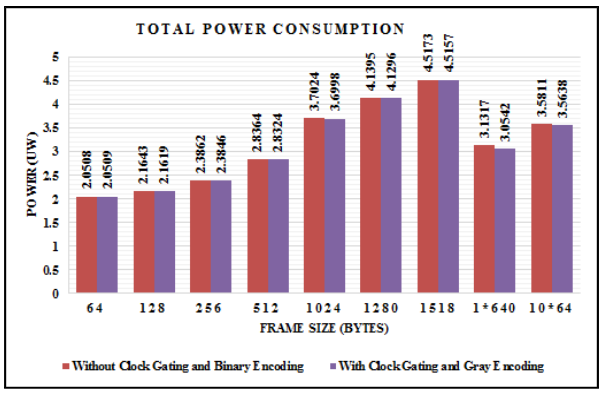

Figure-9. Total power dissipation [3] [6] [7].

From above Figure-9, we can observe that, when both the low power techniques namely clock gating and gray encoding of states are combined, the total power dissipation has improved by 0.40% for the modified design (*A design implemented with above mentioned low power techniques*) when compared against an actual design (*A design without any low power techniques*). From above graph, we can see that for frames having larger length (for example, a frame size of 640Bytes) there is a significant improvement in total power dissipation. For applications that demands huge bandwidth such as video calling, video chat and video conference, the application layer may choose to have frames with large size, which may further improve the overall power dissipation.

CONCLUSIONS

From the above experimental results and the graph plotted using those results, it is seen that, a suitable low power technique that was identified and implemented in the modified design, has reduced the switching activity significantly, that led to potential reduction in dynamic and total power dissipation, for various Ethernet frame length sizes. ie). A significant improvement in power dissipation was achieved from the modified design with suitable low power techniques implemented in it.

The above experiments were conducted on Register Transfer Logic (RTL) level of design, which provides the designer a great flexibility to implement various low power techniques and evaluate its impact on power dissipation occurred for various frame lengths. As a future scope of work, this experiment can be carried out on gate level designs. In gate level designs we may choose gate level netlist, synthesized using a particular technology.

In order to achieve significant improvement to reduce power dissipation in CMOS based designs, all feasible and suitable power reduction techniques should be deployed at all stages of the VLSI design for ASIC applications. The System designers should do a careful analysis before choosing a power reduction techniques that suits well for their design, keeping its implementation impact, its verification challenges [2], performance trade-offs, impact in project schedule and time to market the product.

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