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A LOW POWER MULTIBIT FLIP FLOP MERGING TECHNIQUE USING WSN NODES

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ABSTRACT

In a wireless sensor network nodes, the highest energy consumption exhibits by wireless communication. The low power VLSI designs plays a vital role in today's wireless devices because of limited energy supply from the batteries. The consumption of power reduction not only enhancing the battery life but also reduce the overheat problem. In a modern IC, the power consumption done by the clock which plays the major part in the VLSI designs. Here, the low power is attained by Multi Bit Flipflop Merging technique in WSN using Parallel Prefix Operations (PPO). Along with the power, the minimization of area and Delay is also considered.

Keywords: parallel prefix operation (PPO), WSN nodes.

1. INTRODUCTION

WSN are sometimes called Wireless Sensor and Actuator Network [1]. They are distributed spatially from autonomous sensor network to monitor the physical or environmental conditions such as temperature and pressure [2]. Some of the Characteristics of WSN are as: Using batteries and energy harvester's power consumption constraints for nodes, heterogeneity, scalability, easy of use. These nodes essentially consists of microcontroller, sensors, a radio all combined with limited power supply [3]. For example, battery. In terms of energy, radio transmissions are very expensive; they must be keeping from minimum to extend the node lifetime [4]. The communication to computation energy cost varies from 100 to 3000 [5]. So the data communication should be traded for the node processing which can convert the many sensors measuring reading to the few useful data values [6].

WSN applications need a specific data processing approach since WSN nodes are data driven in nature [7]. Also it requires low energy components of limited energy supply from the scavenging or from batteries. For low power microcontrollers, currently they are designed around off the shelf for on the node processing [8]. Anyhow, when employing more appropriate hardware, also the consumption of energy can be significantly reduced. Hence it identifies many WSN applications algorithm is solved by using the parallel prefix operation sums [6]. It consists of several number of Processing Elements (PEs) designed as a folded tree. Unlike the most recent researches which focus on a single energy constituent of Wireless Sensor Networks independent from other constituents, this novel method of paper presents the Energy Driven Architecture (EDA) as a new technique of architecture and indicates a novel approach for minimizing the energy consumption in total of a WSN [7].

An ultra-low-power nodes [9] which capable of sensing, computation and the wireless communication which has the applications in medicine, security, industrial automation, science [10]. Over the past few years, the implementation of wireless sensor networks utilized nodes are based on off-the-shelf general purpose microcontrollers [11]. The reducing power consumption requires the System on Chip (SOC) implementations which should provide both adequate performance and energy efficiency to meet the demands of the long deployment lifetimes that characterize the applications of WSN [12]. By selectively shutting down idle components the power get consume which can be done in DPM scheme. The S-MAC reduces the wastage of energy caused by idle listening, packet collisions, overhead and overhearing [13]. Duty Cycle Control reduces the energy requirements for the instructed minimum latency within a network or part of a network [14].

2. EXISTING SYSTEM

An existing system which consists of Eight 16-bit Parallel Elements, each consisting of data path with programmable controller and 16 * 36 bit instruction memory [15]. Each mux and data path selects an external data, stored data or the previous result as the next input for the data path [16].

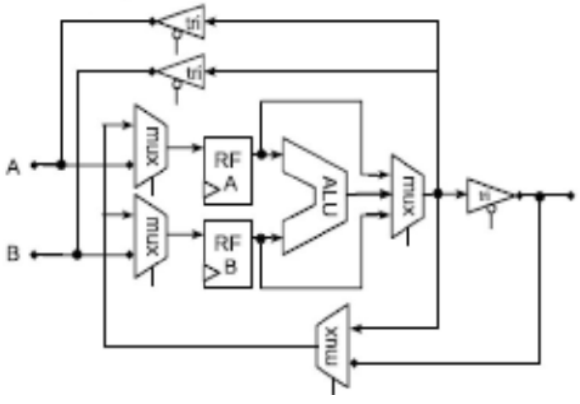

Figure-1. Functional blcok of an existing system.

The data path consists of Register files (RF - A and RF – B) and Arithmetic Logic Unit (ALU) at the inputs A and B shown in (Figure-1) for the operand

isolation. These Register Files are comprises the distributed memory data for the whole system [17]. They are only the clocked elements within the data path [18]. By adopting such a holistic approach assures that energy awareness is incorporated into the groups of communicating nodes and the entire sensor networks and also to an individual sensor node. By following the methodology of the energy-aware design based on the techniques such as designers can enhance the lifetime of network by the orders of magnitude. It consists of several Parallel Processing Elements structured as a Folded clock Tree [19]. In terms of energy, the fabricated chip confirm an]' improvement of 10-20%.

3. PROPOSED SYSTEM

In modern VLSI designs, power consumed by clocking takes the major role in the whole design especially for the designs using deeply scaled CMOS technologies. Here we propose a Multi-bit Flip flop technique for the reduction of power consuming by the replacement of some flip flop without disturbing the performance of the original circuit. Hence the total power reduction is done by replacing the 2 bit flip flop with two 1 bit flip flops consuming the same clock. The Clock skew can be calculated by the delay different points of maximum and minimum delays.

Clock skew = DelayMax -DelayMin

Parallel Prefix Operation (PPO)

The parallel Prefix is the cumulative sum of sequence of numbers a0,a1,a2 and the second sequence of numbers b0,b1,b2 [20]. The sum of the prefixes of the input sequence numbers are:b0 = a0

b1 = a0 + a1
b2 = a0 + a1 +a2

input numbers	1	2	3	4	5	6	...
prefix sums	1	3	6	10	15	21	...

High order parallel algorithm

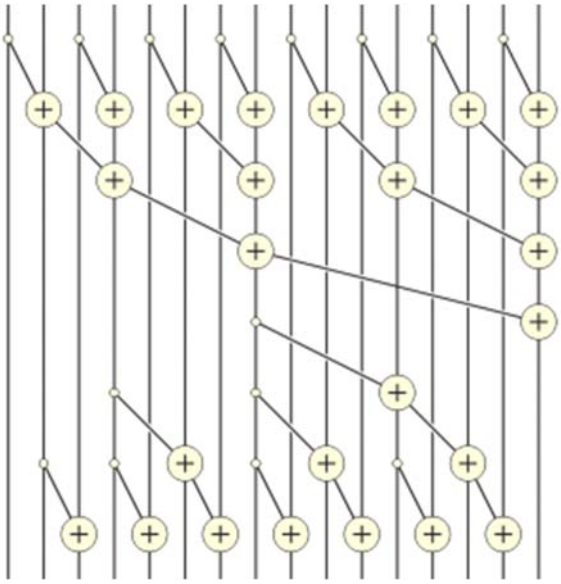

Figure-2. Circuit representation of 16 bit parallel prefix sum.

Multi bit flip flop merging

Many number of Flip Flop in the circuit consumes the most of the power from the power source. Instead of placing separate clock signal for the each and every Flip flops, we can give single clock signal to the flip flop based on the clock skew, its value generated from the combination table.

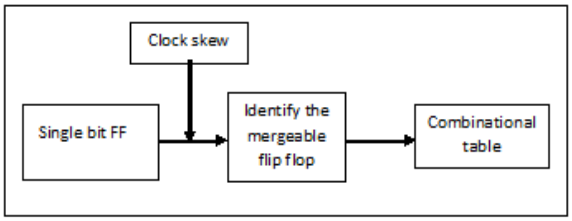

Figure-3. An overview of merging technique diagram.

Hardware details of multi bit flip flop

a) Totally Spartan 3 FPGA contains 100 pins but user can interface 44 pins others for internal uses.

b) This FPGA needs 1.2v DC supply

c) 24 MHz frequency required to execute the program.

Block diagram for the proposed system

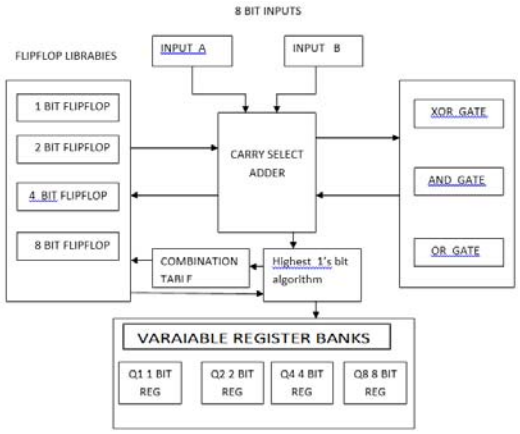

Figure-4. A schematic diagram of the proposed system.

There are five different blocks are present in the proposed system of the multi bit flip flop merging technique as shown in the Figure-4. They are as follows:

a) Input Block

b) Flip flop Library Block

c) Combinational Table

d) Component Block

e) Variable Register Block

Let us see the functionality of each block.

a) Input block

This block is used to define the 8 bit input to the blocks a and b.

b) Flip flop library block

It is the Pre-defined Library which consists of single bit flip flop, two bit flip flop, four bit flip flop, eight bit flip flop.

c) Combinational table

It is used to define the Flip flop Library to built the Adder by the selection of the user.

For example- Selecting the two bit Flip flop, by using the two bit flip flop to build the eight bit adder

d) Component block

The Component block contains 3 basic gate components. They are

a) XOR Gate

b) AND Gate

c) OR Gate

For Adder, we are using the carry select adder method. It is required the add the bit by the help of XOR gate, AND gate or OR gate.

e) Variable register block

This is the output register bank is selected of flip flop in the combinational table. Then the register bank is selected for storing the output data temporarily.

Flow graph of the proposed technique

Here few steps to explain about the flow chart of the proposed system Figure-5.

Step 1: Enter the inputs a and b are in 8 bit format and carryin is single bit format.

Step 2: Selecting the XOR gate, AND gate or OR gate and build the output of sum and carry.

Step 3: Selecting the libraries based on the selection of flip flops. Then the output data storage cycle will also be decided.

Step 4: Combinational table will chose the flip flop libraries.

For example - For 8 bit Sequential Addition

If choosing the 2 bit Flip flop for MSB 4 Bit and 4 bit Flip flop for LSB 4 Bit, the combinational table check the possibilities of flip flop in that particular addition. If possible means then it will select the flip flop libraries and do the adder process to that particular clock cycles.

If it is not possible means, it will show the non-possible flip flop co-ordinates/libraries.

Flowchart

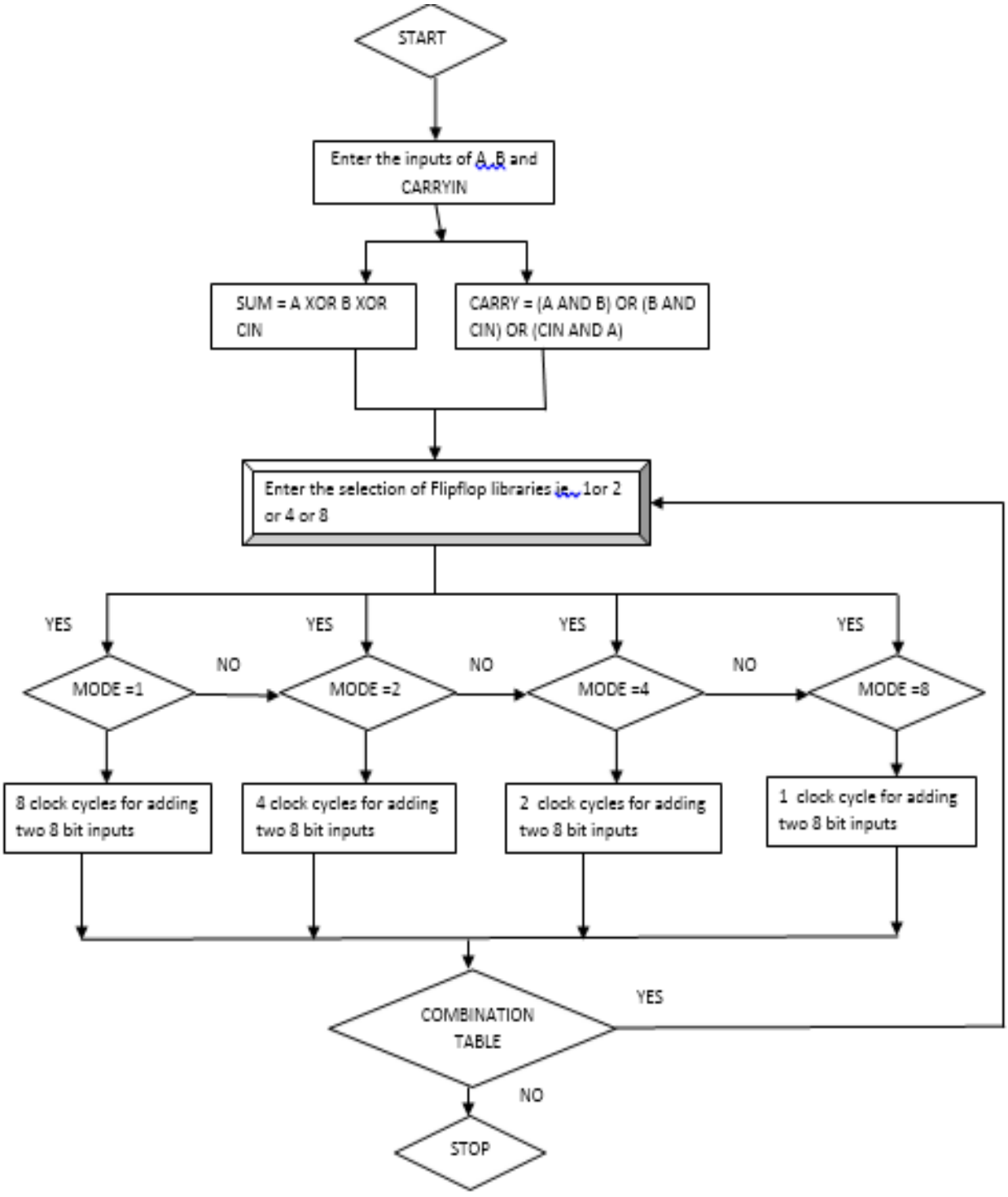

Figure-5. Flowchart for the proposed system.

4. SIMULATION RESULTS

As the previous block diagram and a flowchart which gives the simulation result of multi bit flip flop as shown in the Figure-6. For a Single bit flip flop the simulation output of 8 clock cycle, for two bit flip flop the output will be 4 clock cycle,

For a four bit flip flop the output will be 2 clocks cycle, for an eight bit flip flop the output will be a single clock cycle.

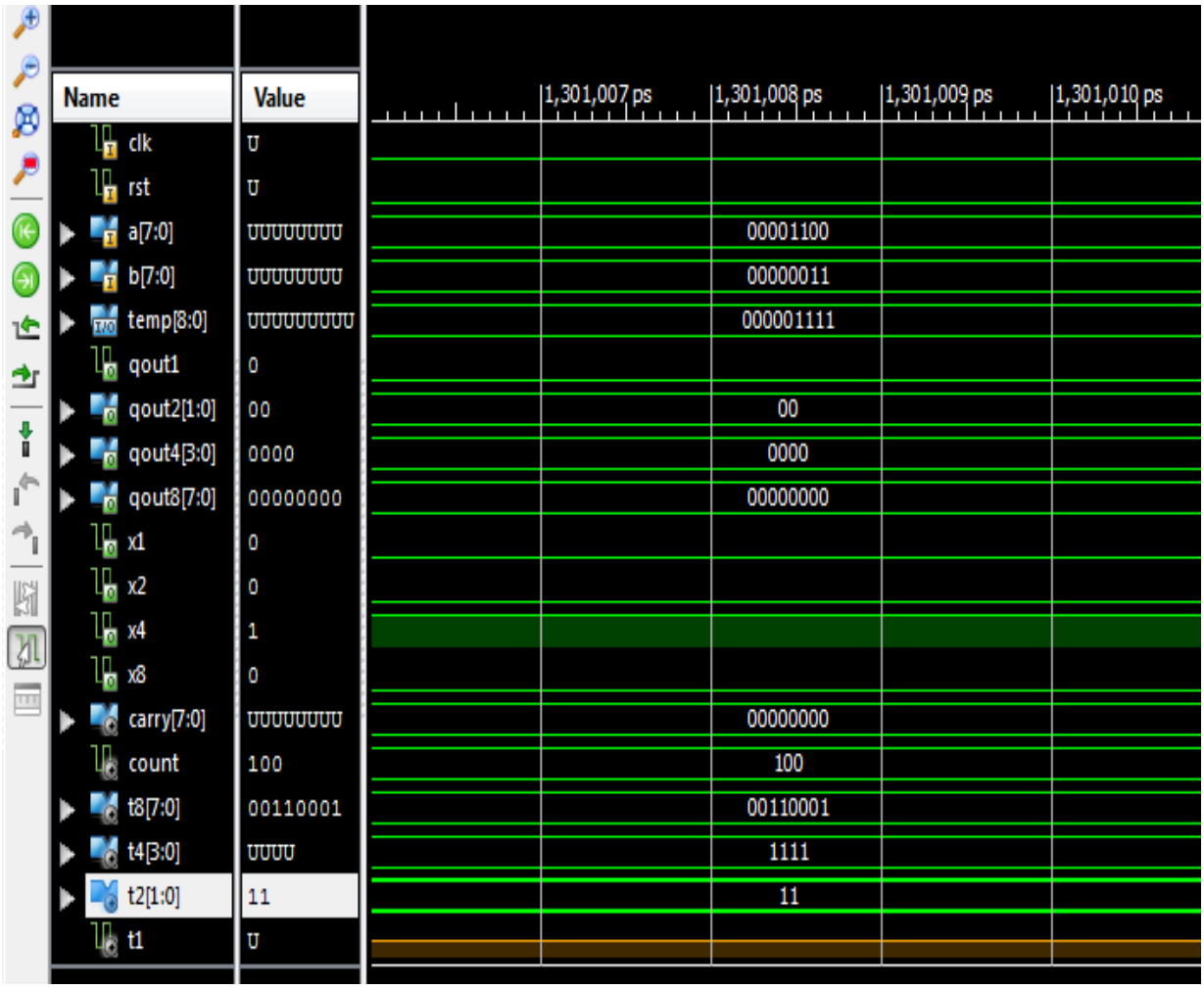

Figure-6. Simulation result of multibit flip flop.

Table-1. Power comparison in multi bit flip flops.

FLIP FLOPS	POWER IN WATTS
Existing System	257.2 mWatts
For Single Bit Flip Flop	150.7 mWatts
For Two Bit Flip Flop	130 mWatts
For Four Bit Flip Flop	110.3 mWatts
For Eight Bit Flip Flop	92.4 mWatts

CONCLUSIONS

Here introduced a new placement flow with clock-tree aware flip-flop merging and MBFF generation. And also proposed the corresponding algorithms to simultaneously minimize power and clock latency when applying MBFFs during placement and also designed multiple bit Flip-Flop up to eight bit and used that Flip-Flop for storing the output of eight bit adder.

And showed the power comparison for single bit, two bit, four bit and eight bit Flip-Flop with eight bit adder using Xilinx 12.4i software. Finally implemented this adder in Spartan - 3E FPGA board.

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