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DESIGN OF LOW POWER LOW VOLTAGE CMOS AMPLIFIERS IN SUBTHRESHOLD REGION

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ABSTRACT

The growing demand of portable electronics equipment makes the circuit designer think about low power low voltage integrated circuit design. The major drawback on implementing strong inversion low-voltage CMOS circuits is the threshold voltage which does not scale down as the same rate as compared to the power supply. Hence the design of electronic circuits operated in subthreshold region has become an absolutely necessary feature in order to provide efficient benefits by technology scaling. This Project focuses on the weak inversion design of low power low voltage Inverter, Nand gate, common source amplifier, Differential amplifier and Operational Transconductance Amplifier (OTA). The CMOS OTA is designed in 350 nm CMOS TSMC process technology and BSIM 3v3 SPICE model and obtained 66db gain, 61 degree phase margin with 163nW power consumption by applying 0.9V supply voltage. In design of CMOS OTA TANNER EDA TOOL is used.

Keywords: amplifiers, digital logic gates, frequency compensation, medium performance, sub-threshold region, ultra low power.

INTRODUCTION

Many researches in balancing the trade-off between power and performance have been done in the average performance, average power region of the design spectrum. Still, not more studies have been done at the two extreme ends of the design spectrum, at one end namely the ultra-low power with acceptable performance and at the other end high performance with power within limit [12]. To achieve the ultra-low power requirement one solution is to operate Transistors in sub-threshold region (supply voltage less than the threshold voltage (Vth)) of the transistor) [11]. In this paper, we investigate sub-threshold region for ultra-low-power applications. The performance characteristics of inverter and Operational Transconductance Amplifier operating in the sub-threshold region have been discussed using 350nm TSMC CMOS technology in Tanner circuit simulation tool.

More recently, design of digital and analog circuits was investigated with transistors operated in the weak inversion region, in such a technique the sub threshold undesired leakage current of the device is used for computation.

Significant power savings can be obtained for low to medium with ten to hundreds of megahertz frequency of operation applications [12]. Hearing aid devices are clearly one of the most appropriate application areas for subthreshold logic since ultra-low-power consumption requirement takes first priority, while the clock rate is nearly in the kHz range [17].

SUBTHRESHOLD REGION

Generally when a MOS transistor in saturation region within any analog or digital circuit, we anticipated that the transistor is turned off (drain to source current is zero) when the transistors gate source voltage is below threshold voltage of that transistor. This region is known as Subthreshold region also known as weak inversion region.

Subthreshold current

In ideal case current flows from drain to source is zero in subthreshold region. But, exactly below the threshold the drain current is exponentially proportional to the gate to source potential [11].

This current is known as subthreshold current and is given as below equation [17].

$$I_D = I_{spec}\ ex\ p\left(\frac{V_{GS}-V_{THO}}{nV_T}\right)\left[1-ex\ p\ \left(-\frac{V_{DS}}{V_T}\right)\right] \quad (1)$$

Where $$I_{spec} = 2nuC_{OX}\frac{W}{L}V_T^2 \quad (2)$$

Where V_{THO} is the threshold voltage of the transistor, V_{GS} is the gate voltage, V_{DS} is the drain voltage,

n is subthreshold factor and is given by

$$\left(n = 1 + \frac{C_d}{C_{OX}}\right) \quad (3)$$

C_{OX} is the oxide capacitance and C_d is depletion capacitance
V_T is the thermal potential

$$\left[V_T = \frac{kT}{q}\right] \quad (4)$$

k is Boltzmann constant, T is room temperature in Kelvin [300K], q is charge of electron[17].

If V_{DS}>4V_T then $\exp\frac{-V_{DS}}{V_T} \ll 1$, since $e-4 \cong 0.018$. The last term in equation (1) is approaches equal to one, which can be ignored. So, the expression for drain current then,

$$I_D = I_{spec}\ exp\left(\frac{V_{GS}-V_{THO}}{nV_T}\right) \quad (5)$$

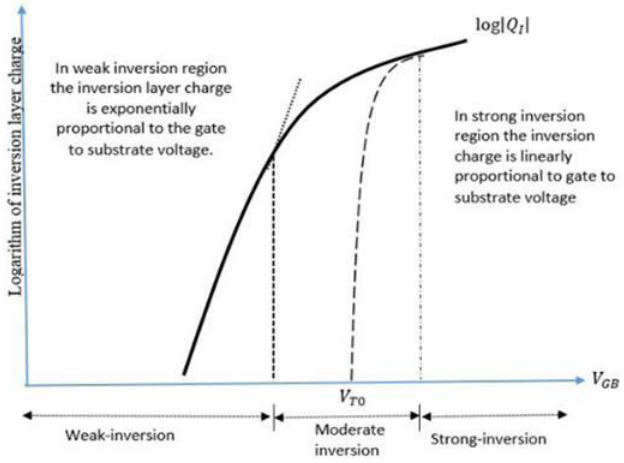

Figure-1. Logarithm of inversion layer charge per unit area Vs gate to substrate voltage.

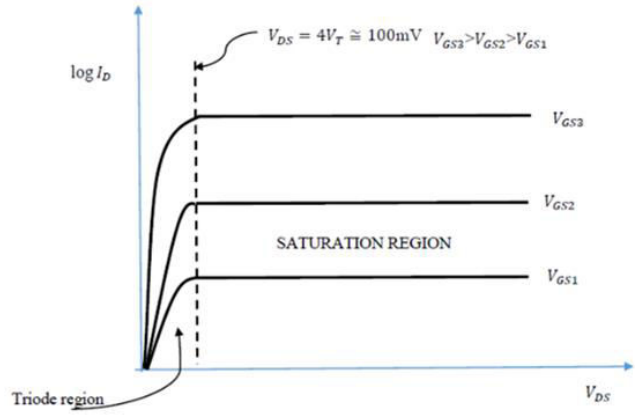

Figure-2. Output characteristics of an n-channel MOSFET operation in the weak inversion region in a log-linear plot.

The drain current equation (5) is independent on the value of V_{DS}, hence V_{DS}>4V_T when in the sub-threshold region, this region can be treated as saturation of MOSFET in sub-threshold. As V_{DS}required to do so and it does not depend on Vgs as in the case above threshold. It is easy to keep the MOSFET in saturation for subthreshold operation. This is very beneficial for low-voltage designs.

Subthreshold logic design of inverter

Subthreshold CMOS logic operates with the less supply voltage Vdd less than the transistors' threshold voltage Vth. This is done to make sure that all the transistors are indeed operating in the subthreshold region.

Inverter designed in subthreshold CMOS logic with vdd 0.2v, input voltage 1v, loading capacitance 100pF, W/L of pmos 50u/.25u and for nmos 2.5u/.25u. This inverter functions as strong inversion operation but consumes only 1.6pW.

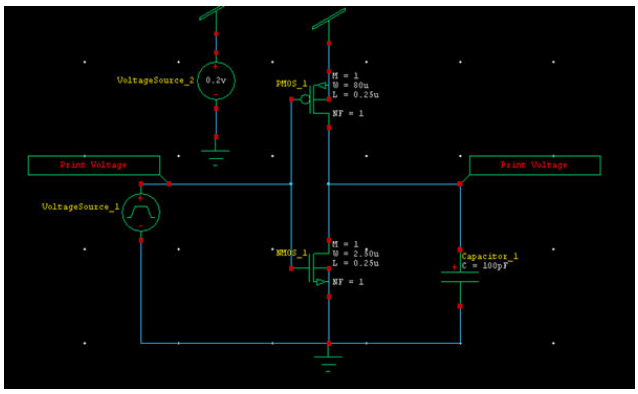

Figure-3. Subthreshold inverter schematic.

Input bit voltage given as 0101011 and corresponding output is obtained from the W-edit wave form viewer.

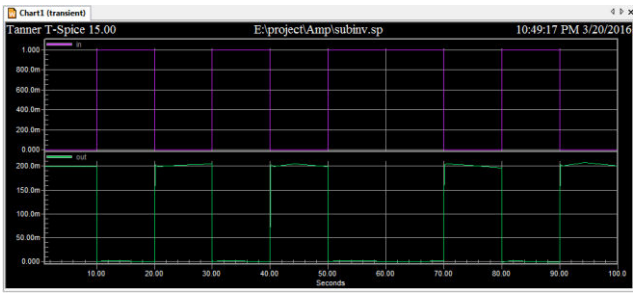

Figure-4. Output transient response of subthreshold invertor.

Subthreshold logic design of Nand gate

The NAND gate is designed in the subthreshold CMOS logic is as shown in Figure-3.3. Transistor's aspect ratios are for both pmos 50u/.25u,for both pmos 2.50u/0.25.Power supply 0.2V,loading capacitor 100pF. Power consumption is only 6.18fW.

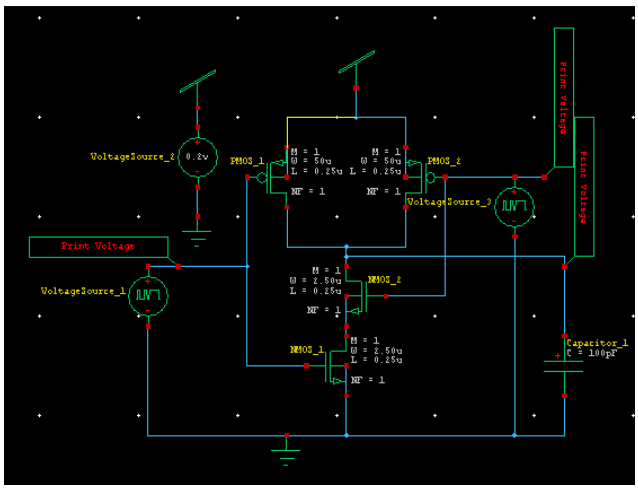

Figure-5. Subthreshold Nand gate schematic.

The Figure shows the output transient response of basic Nand gate with supply voltage of 0.2V.It is seen that

the operation is almost similar with strong inversion Nand gate with very low power consumption.

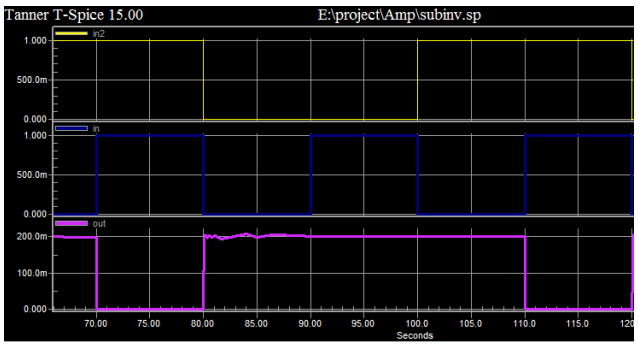

Figure-6. Output transient response of subthreshold Nand gate.

Subthreshold logic design of common source amplifier

Common source amplifier is a simple basic CMOS amplifier with only one MOSFET whose source is common to both vdd and vss supply.

Below is the N-MOSFET common source amplifier with 0.5uA bias current and 0.1v vdd supply voltage.

Common source amplifier is also known as transconductance amplifier as the current at the output is proportional to input voltage applied at gate terminal of n channel MOSFET.

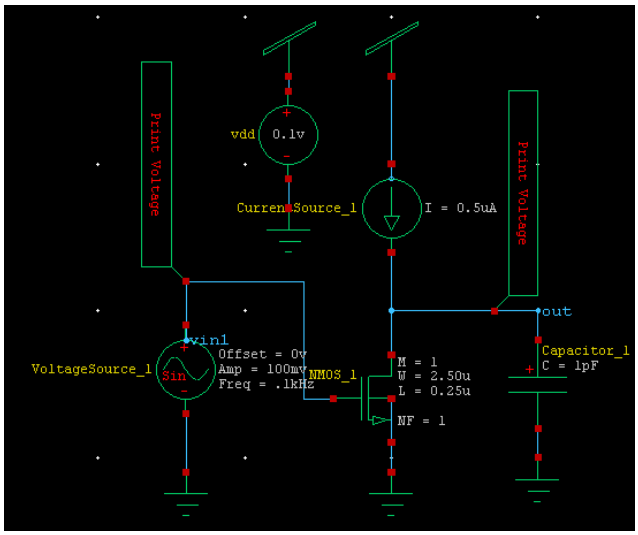

Figure-7. Subthreshold common source amplifier schematic.

N-mosfet common source amplifier designed with 0.5uA bias current and 0.1v Vdd supply voltage.

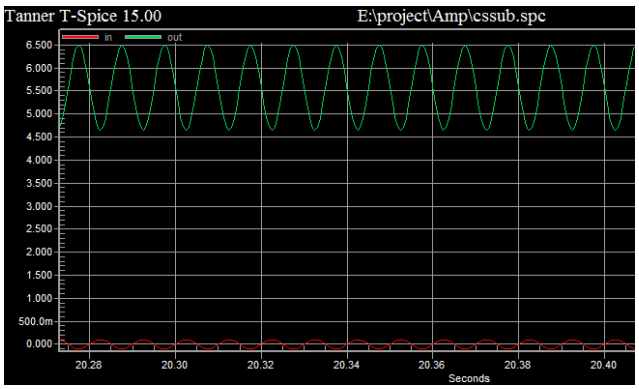

Figure-8. Output transient response of subthreshold CS amplifier.

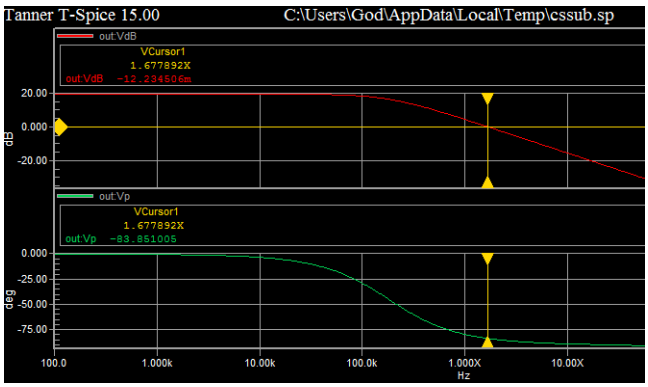

Figure-9. AC analysis of subthreshold common source amplifier.

From the above analysis gain plot crosses 0db at 1.6MHz and corresponding phase margin is 96 degree Measurement results:

Gain	= 19.3367 db
PhaseMargin	= 96.1577 degree
UnityGainBandwidth	= 1.6755 MHz
GainBandwidthProduct	= 32.3987 MHz

Average power consumption = 2.7uW

Subthreshold logic design of differential amplifier

A differential amplifier is one of the type of amplifier in electronics that amplifies the difference between two input voltages but eliminates any voltage common to the two inputs. It is an analog circuit with two inputs vin- and vin+ and one output Vout in which the output is ideally proportional to the difference between the two voltages

Vout=A (vin+ - vin-)

Where A is the gain of the amplifier

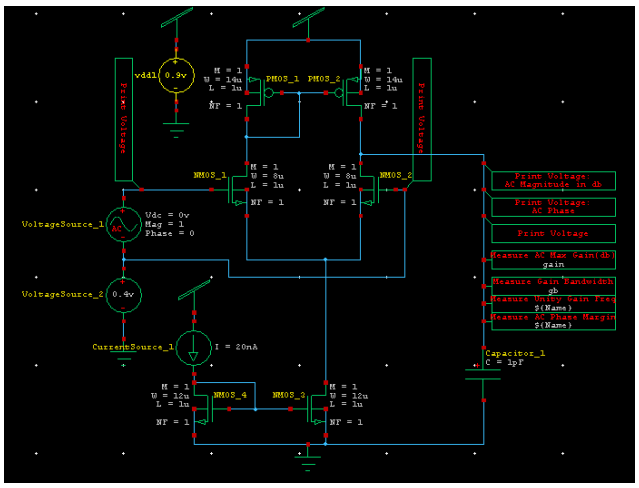

Figure-10. Subthreshold differential amplifier schematic.

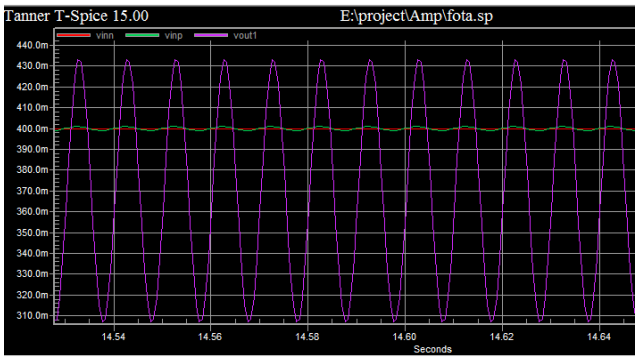

Figure-11. Output transient response of subthreshold differential amplifier.

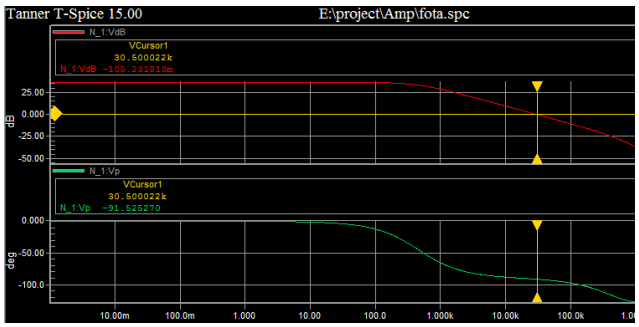

Figure-12. AC response of subthreshold differential amplifier.

Below results are obtained from AC analysis of subthreshold differential amplifier

gain = 35.9044
PhaseMargin = 88.2075
UnityGainBandwidth = 30.2333k
Gain bandwidth product = 1.08550M
Average power consumption = 22nW

Subthreshold logic design of two stage OTA

OTA Operational Transconductance amplifier is one of the main building block of many analog integrated circuits [4]. OTA differs from regular OPAMP by the output stage. OTA has ideally infinite output impedance and output is current also it is proportional to the voltage difference between two inputs, whereas in OPAmp output is voltage with ideally zero output impedance, which is achieved by having buffer stage as output stage.

OPAmp is voltage controlled voltage source whereas OTA is voltage controlled current source.

Two stage amplifiers generally have 2 amplifier stages one is differential amplifier and second gain stage.

Two stage OTA is designed by combine transconductance amplifiers differential amplifier and common source amplifier to achieve the higher gain. But stability is one of the main criteria to manage.

As there are 2 poles in 2 stage OTA that produce 20 db degrade in gain for each pole that leads to stability issues. To make sure the stable system second pole should be greater that unity gain frequency. To do this Miller compensation capacitor is used between input and output node.

Below circuit is to analyze small signal behavior in two stage circuit with miller compensation capacitor Cc to ensure the stability of two stage OTA.

Frequency compensation technique

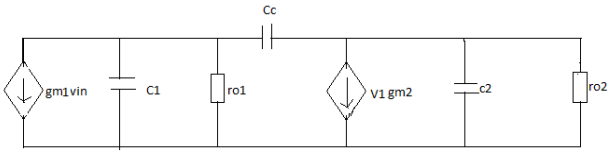

Figure-13. Small signal analysis of two stage amplifier.

Above figures shows the small signal circuit for 2 stage amplifier with miller compensation capacitor Cc.
Poles of the 2 stage amplifiers are
P1=1/ro1c1
P2=1/ro2c2

Applying KCL in input side we can get below equation.
Considering ro1 as R1, ro2 as R2,
V1/(1/Sc1) + V1/ R1+ gm1Vin + (V1-V0)/(1/ SCc) =0
V1= ((V0 SCc R1- gm1 R1Vin)/(1+ SR1(C1+Cc)
Similarly in output side,
V0/(1/SC2) + V0/ R2+ gm2V1+ (V0-V1)/(1/ SCc) =0
V0 (S(C2 + Cc)+ (1/ R2) = V1(SCc- gm2)
V0(S(C2 + Cc)+ (1/ R2) = ((V0 SCc R1- gm1 R1Vin)(SCc- gm2))/(1+S(C1 + Cc) R1)
V0 [S(C2 + Cc) R2+1][1+S(C1 + Cc) R1]=[V0 S Cc R1- gm1 R1 Vin]

General equation for the gain in 2 stage amplifier is given below:
V0/ Vin =ADC (1-(S/Z)/(1+(S/R)(1+(S/R2)
= ADC(1-(S/Z)/(1+S((1/P1)+ (1/P2))+S2(1/P1P2))
=S((1/P1)+(1/P2))

Comparing this standard equation of 2 pole system with our equation we get below values
P1P2 =1/(R2(c1 + Cc)+ R1(c2 + Cc))

= gm2 Cc/(C1 C2+ C1 C2+ C2 Cc)
Neglect C1 C2+ C1 C2
P1P2= gm2/ C2
DC gain of 2 stage amplifier is given as
ADC = gm1 R1 gm2R2 (6)
Gain bandwidth product is given by
GBW = DC gain * P1 (7)
GBW = gm1 R1 gm2R2*1/(gm2 R1R2 Cc)
GBW = gm1/ Cc1 (8)

Phase margin

Vo/Vin = - tan-1 (W/Z) - tan-1 (W/P1) tan-1 (W/P2)
= tan-1(1/10) - tan-1(ADC) - tan-1(GBW/P2)
Pm= 84.29-tan-1(GBW/P2)
(GBW/P2) = tan 24.29=0.4513
P2 =2.2 GBW
=2.2(gm1/Cc)
For 60^o phase margin, P2 =2.2 GBW, zero =10 GBW
gm2=10 gm1
gm2/CL≥2.2(gm1/10Cc)
Cc≥0.22 CL (9)

The above condition should be satisfied when we want the phase margin be around 60^0

DESIGN CONSIDERATION

Slew rate calculation and bias current estimation
Q=CV
dq/dt=I=C(dv/dt)
dv/dt=I/C
SR=I_0/CL (10)
CL=5.5PpF
I_0= SR* CL
SR=3.5mV/us
I_0 = 3.5*5.5pF
I_0 =19.3nA

Calculation for compensation capacitor

From equation (9) To get 60 degree phase margin the condition is
Cc≥0.22 CL.
CL we have 5.5PpF
So, Cc≥1.21

So compensation capacitor must be ≥1.21, lets have 2pF for this design.

Calculation for transconductance and transistors size

Let us design gm1 for Cc1=2pF and 30KHz unity gain bandwidth, we need to calculate gm from below equation.
GBW = gm1/ Cc1
gm1=300uS.
gm1=I_{D1}/nVt
I_{D1}=10nA, Vt=26mV

Subthreshold slope factor n is estimated as 1.63 for nmos

Similarly Subthreshold slope factor n is 1.56 for pmos by examining the gm value from operating point analysis.

From structure of the Figure-14 we can equate the below transistors sizes as they are current mirrors.
(W/L) nmos_1 =(W/L)nmos_2
(W/L) nmos_3 =(W/L)nmos_4
(W/L) pmos_1 =(W/L)pmos_2

According to the above specification Operational Transconductance amplifier is designed as follows.

nmos_1 and nmos_2 are the input transistors whose transconductance decides unity gain bandwidth of the amplifier.Nmos_3 and Nmos_4 are the current mirrors which forces drain current of Nmos_4 to be equal that of Nmos_3.

pmos_1 and pmos_2 are current mirror load, whereas pmos_3 and nmos_5 are the common source amplifier form the second stage to increase the gain of the Operational transconductance amplifier. Bias current IB flow through nmos_3 and nmos_4, as there are two branch IB flow through nmos_1 as well as nmos_2

In pmos_1 and pmos_2 the same current IB/2 flows as they are current mirror loads. Bias voltage is also given to pmos_5 for second stage bias current.

Table-1. Subthreshold OTA parameter values.

Devices	Value	
	W	L
nmos_1,nmos_2	6µm	1µm
pmos_1,pmos_2	14µm	1µm
nmos_3,nmos_4	10µm	1µm
pmos_3	175µm	1µm
nmos_5	75µm	1µm
Supply voltage Vdd	0.9V	
Load Capacitance (CL)	5.5pF	
Compensation Capacitor	2pF	
Bias current	20µA	

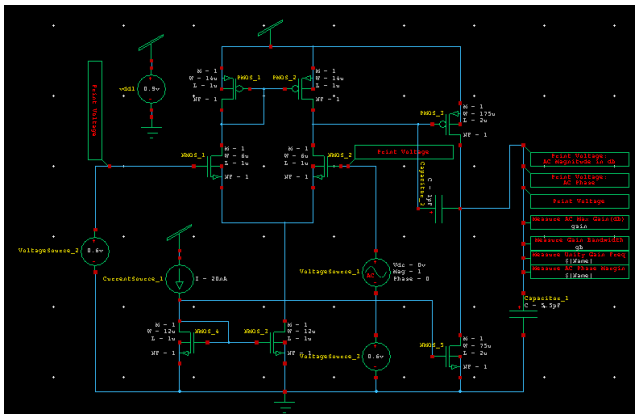

Figure-14. Subthreshold OTA schematic.

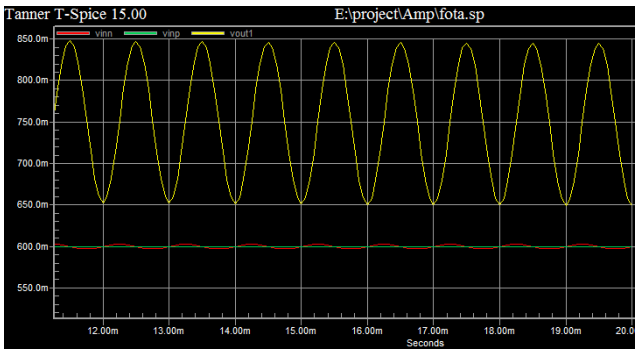

Figure-15. Output transient response of subthreshold OTA.

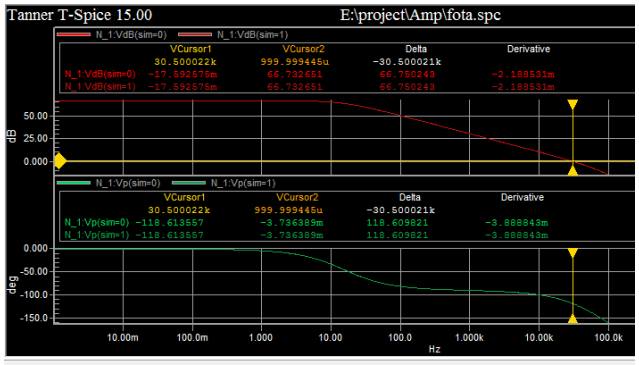

Figure-16. AC response of subthreshold OTA.

Results

Average power consumed -> 163nW
Measurement result summary

Gain	=	66.7326 db
PhaseMargin	=	61.4315 degree
UnityGainBandwidth	=	30.4468kHz
Gain bandwidth product	=	2.0318MHz

LOW PASS FILTER USING SUBTHRESHOLD LOGIC

To illustrate the application of designed OTA we have designed Low pass filter with the above subthreshold CMOS OTA.

Design of low pass filter

A Low pass filter is designed with below specifications
Cut of frequency fc=2kHz
R=10K
Equation for fc is given by

$$fc=1/2\pi RC \quad (11)$$

Value of C can be calculated from above equation as 0.0079uF

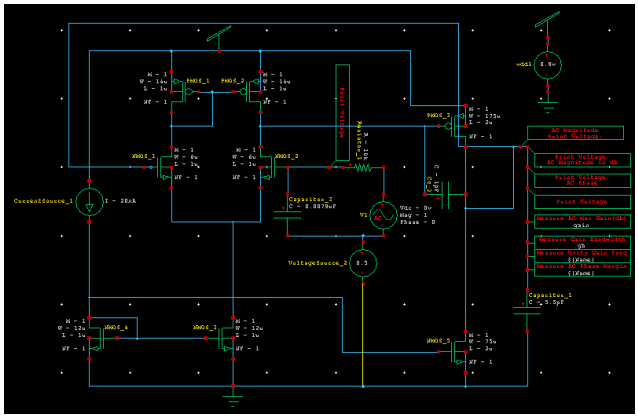

Figure-17. LPF using subthreshold OTA.

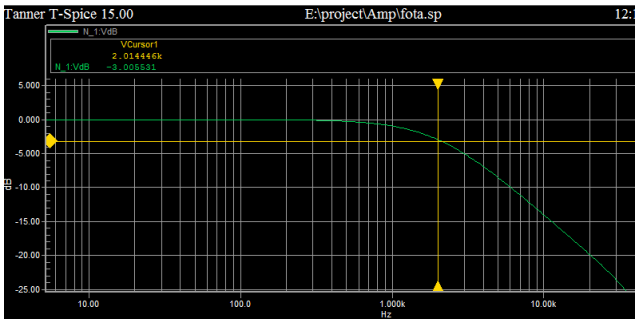

Figure-18. Output response of LPF using subthreshold OTA.

From the above output response of LPF we have obtained 3db frequency as 2kHz exactly as designed.

Table-2. Comparison of the power consumption between strong inversion and weak inversion (subthreshold) region circuits.

Devices	Parameters	Strong inversion	Weak inversion
Inverter	Supply voltage	2V	0.2V
	Power consumption	98.77uW	1.6pW
Nand gate	Supply voltage	2V	0.2V
	Power consumption	18.37uW	6.18fW
Common source amplifier	Supply voltage	2V	.1V
	Gain	19 db	19 db
	Phase margin	96 degree	96 degree
	Unity gain band width	3.2MHz	1.6MHz
	Gain bandwidth product	62MHz	32MHz
	Power consumption	5.8uW	2.7uW
Differential amplifier	Supply voltage	5V	0.9V
	Gain	35 db	36 db
	Phase margin	88 degree	88 degree
	Unity gain band width	4MHz	30kHz
	Gain bandwidth product	159MHz	1.08MHz
	Power consumption	277uW	22nW
Operational Trans conductance amplifier	Supply voltage	5V	0.9V
	Gain	62 db	66 db
	Phase margin	65 degree	61 degree
	Unity gain band width	30MHz	30kHz
	Gain bandwidth product	1.86MHz	2MHz
	Power consumption	380uW	163nW

CONCLUSIONS

Subthreshold behaviour of MOSFET has been examined. From the analysis, it is seen that MOSFETs operating in subthreshold region produces output similar to normal strong inversion operation with very low power consumption. MOS transistors operating in the subthreshold region would be a classical design methodology to satisfy the ultra-low-power demand.

Subthreshold region is particularly suitable in wireless sensor networks, biomedical applications and in those applications where speed is not a concern, e.g., for bandwidth specifications in the range of a few kilohertz. Implementing subthreshold logic design to other low frequency applications in biomedical would be the future work of my research.

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