DESIGN AND SIMULATION OF THE SOLS TECHNIQUE APPLIED FOR FM0, MANCHESTER AND MILLER ENCODING SCHEME

R. Sangeetha Vani[1] and M. R. EbenezarJebarani[2]
[1]Department of Electronics and Communication Engineering, Sathyabama University, Chennai, India
[2]Faculty of Electrical and Electronics, Sathyabama University, Chennai, India
E-Mail: sangeetha06.1990@gmail.com

ABSTRACT

Encoding techniques are fetching important role in communication. Techniques like Miller, Manchester, and FM0 encoding are used in numerous applications. Each technique has different operations depends on their needs. Each and every encoding scheme are used without losing any of its parameters. This paper adopt similarity oriented logic simplification technique (SOLS technique) which merges architecture together and synchronize the operation and also DSRC technique is used to maintain the dc-balance and signal reliability. By applying both the techniques we can reduce the number of transistors and maintains the DC balance. The present work deals with obtaining an integrated architecture of FM0, Manchester and Miller encoding to overcome several drawbacks of traditional method. A universal asynchronous receiver/transmitter (UART) is used here to translate data between parallel and serial forms for communication. In this proposed approach the number of hardware components is reduced, hence results in the reduction of the overall area consumed with the added functionality in DSRC.

Keywords: DSRC, SOLS, FM0, Manchester, Miller, UART.

1. INTRODUCTION

Encoding used for communication to convert the information into suitable form for transmission. Encoding techniques can also be used for security purposes. This type of encoding is utilised at the transistor level, so it can be used with optical communication.FM0 ,Manchester and Miller coding techniques are used in this paper to encode the data while transmit the signal through UART medium. Since, encoding plays the dynamic role in secured communication. Developing architecture for such encoding techniques using SOL's method by DSRC (Dedicated Short Range Communication) application. DSRC is designed to support the variety of applications based on vehicular environments communication. DSRC, the subset of RFID (Radio Frequency Identification) for tracking and identification. DSRC is a protocol for one- or two-way medium range communication especially for intelligent transportation systems. Enables the message sending and broadcasting among automobiles for safety issues and public information announcement and very much useful in the ETC -Electronic Toll Collection system. In case of ETC system, the toll collecting is electrically accomplished with the IC-card platforms that are contactless. Perhaps, the ETC can be extended to the payment for parking-service and gas-refuelling as well. The SOLS (Similarity oriented logic simplication) can be implemented with two methods namely balance logic sharing and area-compact retiming. The area-compact retiming used to reduce the transistor counts and balance logic-operation sharing is used on the transistor level, so it can be used with to combine the FM0, Miller and Manchester encoding schemes.

2. LITERATURE REVIEW

Yu-hsuan lee and cheng-weipan (2014) discussed about the coding-diversity among the FM0 and Manchester codes seriously limiting the design of the fully reused VLSI architecture for both the encoding schemes. In this paper, the similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation. John B. Kenney (2011) done the study on automotive industry. The industry is in the verge of developing dedicated short-range communication equipment, for use in vehicle-to-vehicle and vehicle-to-roadside communication. Dependence of the co-operative principles for interoperability decides the effectiveness of this technology.

Yu-Cherng Hung, Min-Ming Kuo, *et al.*, (2009) proposed a modified Manchester and Miller encoder that can operate in high frequency without a sophisticated circuit structure. The concept has adopted the concept of parallel operation was used to improvise the data throughput. Here in addition to that, this technique of hardware sharing is adopted in the proposed design to reduce the number of transistors.

Subsequently, P. Benabes, A. Gauthier, and J. Ohman, (2003) described a new Manchester code generator which is designed at the transistor level. The generator described uses 32 transistors and has the same complexity as a standard D flip-flop. The main advantage of this design is using a clock signal which is having the similar frequency as the data. Output variations on the rising edge and falling edge of the clock.

Ayoub Khan, Manoj Sharma, *et al,* (2008) offered a high-level architecture of tag emulator and attempted to present a high focus to use the RFID Emulator as data transport device and level design of UHF RFID tag emulator and implementation fixing tool. The synthesis result demonstrates that FSM design is of FM0 and Miller encoders tobe used in the RFID tag efficient and we have achieved operating frequency of emulator 192.641 MHz and 188.644MHz for FM0 and Miller encoders.

Daniel Jiang, Vikas Taliwal, *et al*., (2009) deals with the explicit multichannel nature of DSRC which necessitates on a simultaneous and multichannel operational system for safety and non-safety applications. This paper dealt with an overview of DSRC based safety communications between vehicles and proposes a coherent set of protocols to address these requirements.

Yu-hsuan lee and cheng-weipan, (2006) defines an intrinsic unbalance computation load etweenFM0 and Manchester sorts their VLSI planning with poor hardware consumption. In order to overcome this problem, in this paper they have proposed a reuse-oriented Boolean simplification (ROBS) technique. The ROBS technique constructs the balance-type design to progress the hardware utilization rate from 50 % to 90 %.

Juinn-horngdeng and feng-chin Hsiao *et al*., (2006) offered a joint discovery and authentication of frequency shift keying (FSK) modulation and demodulation (MODEM), Manchester coding and decoding schemes are proposed for dedicated short range communication (DSRC) systems over high mobility fading channels. They have proposed a joint coded-FSK detection scheme with a low complexity-FSK detection scheme.

Tiancheng Zhang *et al*., (2014) presented a RFID simulation system which supported effective data analysis and helped users to judge the effectiveness of the deployment. This system have implemented part of ISO 18000- 6C communication protocol and supports backscatter, the path loss tag mobility and capture models. It provides a user-friendly visual platform for users which enabling them to build virtual scenarios of their own and to deploy the RFID devices into it. Furthermore, in order to improve the efficiency of operations in the application scenarios, and combine R-Tree with TSB-Tree to support the RFID object setting and the route analysis.

Manar Mohaisen, Hee Seok Yoon, *et al*., [2008] analyze the performance of the encoding and the modulation process in the uplink and downlink of the EPC global Gen2 system through the investigation and model. Adding to that, the issue of synchronization on time and frequency domain, as well the preamble design is estimated. Over the simulation in the uplink, this paper determines the detection probability of FM0 and Miller coding

3. PROPOSED WORK

A. FM0/Manchester/Miller encoder with sols technique

The purpose of SOLS technique is to design a fully reused VLSI architecture for FM0, Manchester and Miller encodings. The SOLS technique is classified into two parts

(i) Area-compact retiming
(ii) Balance logic-operation sharing.

The area-compact retiming relocates the hardware resource to reduce transistors. The balance logic-operation sharing combines different encodings with the identical logic components to achieve the DC-balance and signal reliability.

(i) Area compact retiming

The area compact retiming is shown in Figure-1 displaces the hardware resource to reduce the transistor it mainly used in FM0 encoder. For FM0 the state code of the each state is stored into DFFA and DFFB.
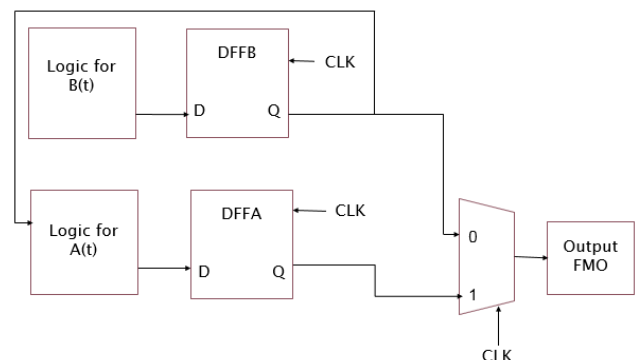

Figure-1. Without area compact retiming.

In Figure-2 the transition of the state code is only depends on the previous state and is denoted as the A(t-1) and then the B(t-1) and then the current state is denoted as the A(t) and then the B(t) instead of the both A(t-1) and B(t-1) ,here B(t) is the previous state of B(t-1) Thus, the FM0 encoding just requires a single 1-bit flip-flop to store the previous value B(t−1). If the DFFA is directly removed, non-synchronization between A(t) and B(t)causes the logic fault of FM0 code. The DFFB is relocated right after the MUX−1 to avoid this logic fault, where the DFFB assumed to have positive-edge triggered flip flop. Atevery cycle, the FM0 code, comprising A and B, is derived from the logic of A(t) and B(t) respectively. In this case FM0 code is alternatively switched between A(t) and B(t) via MUX−1 by the control signal of the CLK.
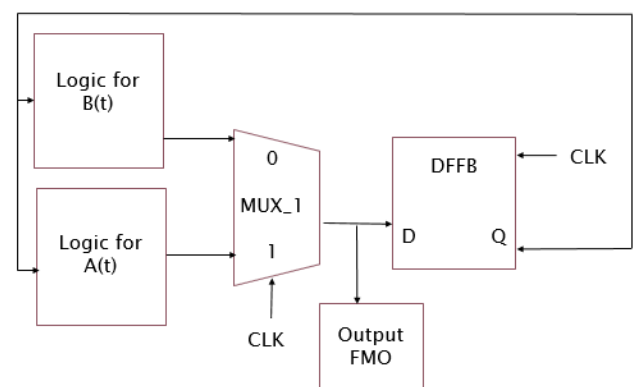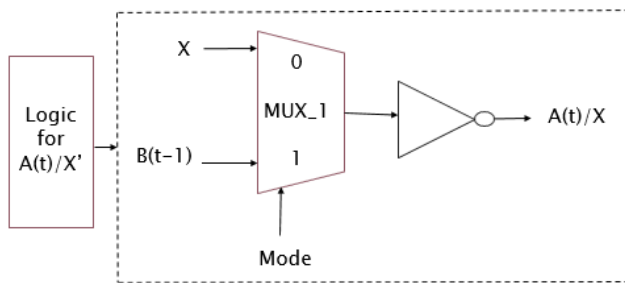

Figure-2. With area compact retiming.

In Figure-3 the Q of DFFB is directly updated from the logic of B(t)with 1-cycle latency. When the CLK is logic-0, the B(t) is passed via MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB the timing diagram of the value Q of DFFB is here consistent whether the DFFB is relocated or not the B(t) is passed through MUX−1 to the D output of DFFB. Followed by it, the forth-coming positive-edge of CLK updates it to the Q of DFFB the timing chart for the Q of DFFB is steady whether the DFFB is relocated.


Figure-3. FM0 encoding with area compact retiming.

(ii) Balance logic operation sharing

The Manchester encoding is expressed using the XOR operation. Equation of the XOR gate is

$$X \oplus CLK = X\ CLK + \sim X\ CLK \quad \longrightarrow \quad (1)$$

The concept of balance logic-operation sharing shown in the Figure-4 integrate the X into A (t) and X into B (t), here the FM0 and Manchester encoding logics have a common part of use of the multiplexer like logic with the selection of the CLK. The inverted of B (t-1) cab be used to obtain the value of A (t) and X is obtained by an inverter of X. The logic for A (t)/X can be formulated in sharing the same inverter in the circuit, and then a multiplexer is placed before the inverter to switch the operands of B (t- 1) and X. The Mode indicates which mode is adopted either FM0 or Manchester encoding. The similar concept can be also applied to the logic for B (t)/X. However, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and the Manchester encoding have not utilised it in shared mode. Therefore, the HUR of this architecture is certainly limited.
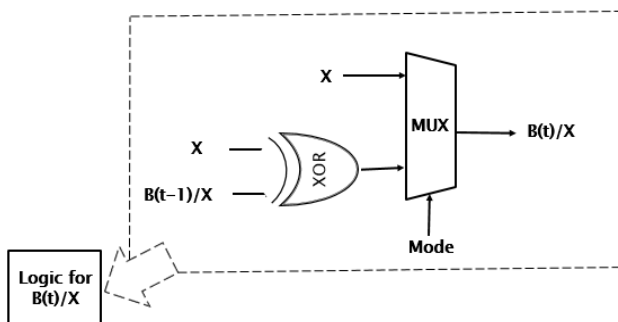

Figure-4. Balance logic operation sharing.

This architecture shares the XOR for both B (t) and X, and there by increases the HUR. When we adopt the FM0 code, initially the CLR is disabled then the B(t - 1) can be derived from DFFB .Hence, the relocated DFF can be used totally to save the multiplexer. The logic for A (t)/X includes an inverter and MUX-2. In its place, the logic for B(t)/X just incorporates a XOR gate. In the logic for A(t)/X, MUX-2's computation time is almost identical to XOR in the logic for B(t)/X.

However, the logic for A(t)/X further integrates an inverter in the series to that of MUX−2. This unbalance computation time between A(t)/X and B(t)/X results in a glitch to the MUX−1,which in-turn causing the logic fault on coding.

To improve this unbalance computation time, the architecture of A(t)/X and B(t)/Xwith the balance computation time between them is derived. The XOR in the logic for B(t)/X is translated into the XNOR using an inverter, proceeded by sharing the same with the logic for A(t)/X. This shared inverter is then relocated backward to that of the output of MUX−1. In this way, the logic computation time between A(t)/X and B(t)/X is more balance to each other.
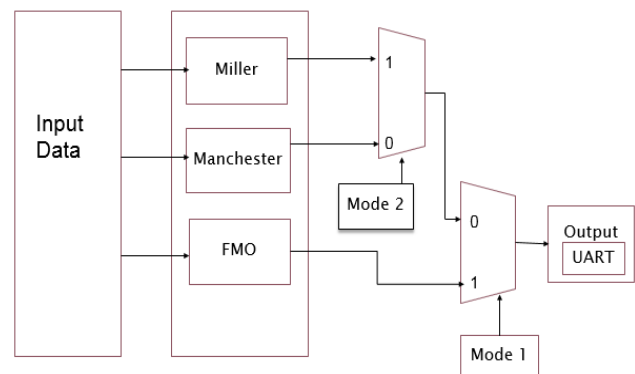
Figure-5. Proposed block diagram.
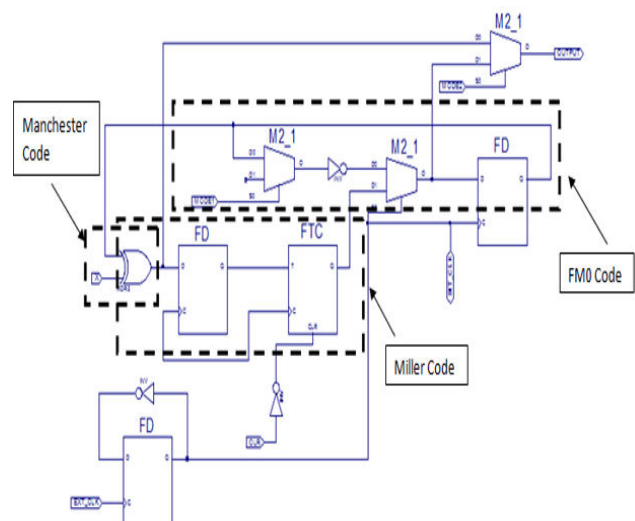
Figure-6. Architecture of proposed system.

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Table-1. Mode selection.

Mode 1	Mode 2	Output
0	X	Manchester
1	0	FM0
0	1	Miller

The Architecture in the figure Figure-6 shows the schematic of FM0/Manchester/Miller with SOLS technique. The adoption of the encoding is derived based on the Mode and CLR depicted in the Table 1. The CLR in addition has another individual function of a hardware initialization. If in case CLR is derived by inverting the Mode without allocatinganseparate CLR control signal, this leads to a conflict between the hardware initialization and coding mode selection.

To avoid this conflict, both the Mode and CLR are assumed to be allocated separately pertaining to this design from the system controller. Whether the schemes FM0 or Manchester or Miller code is adopted depends on Mode and CLR, at handno logic component of the proposed architecture been wasted. Every component is active in all the encodings. Hence, the HUR of the proposed architecture is improved greatly. The coding-diversity between FM0, Miller and Manchester encoding techniques case the limitations on the hardware utilization of the architecture design. By using this SOLS technique, the hardware utilization rate has been improved. It not only develops a fully reused VLSI architecture, but also has the capability to exhibit a reasonable performance compared with the existing works.
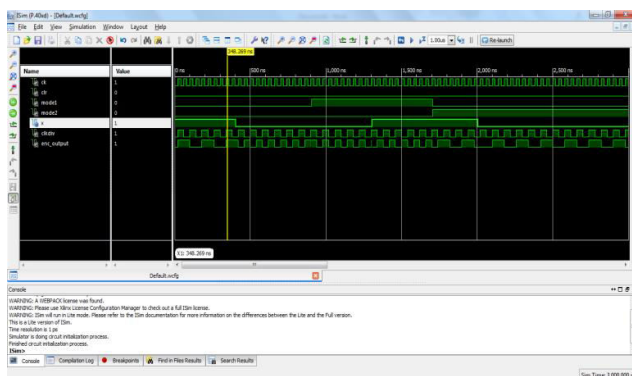
4. EXPERIMENTAL RESULTS AND DISCUSSIONS

Figure-7. SOLS technique for Manchester (mode = 00).

Figure-7 depicts the SOLS based design of the encoding schemes that operates in the Manchester mode selected by the mode values as mode0 = '0' and mode1= '0', the data is encoded in the Manchester encoding scheme and transmitted based on the UART protocol.
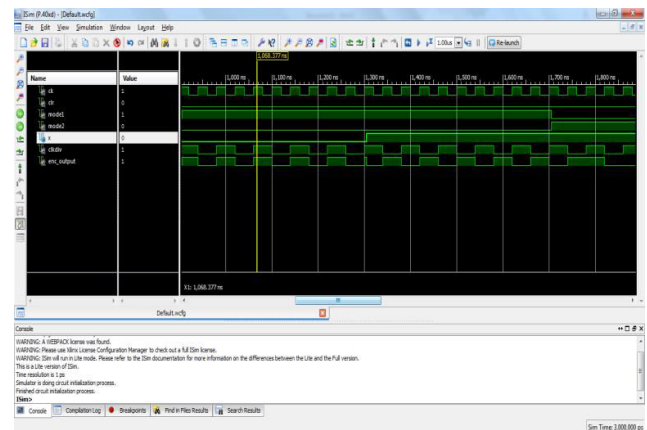

Figure-8. SOLS technique for FMO (mode = 10).

Figure-8 displays the SOLS based design of the encoding schemes that operates in the FMO mode selected by the mode values as mode0 = '1' and mode1= '0', the data is encoded in the Miller encoding scheme and transmitted based on the UART protocol
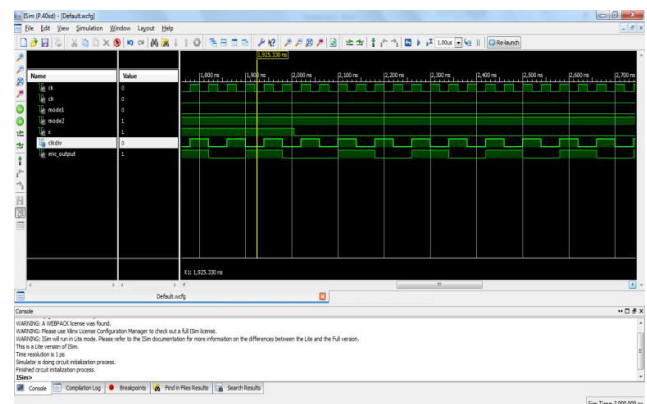

Figure-9. SOLS technique for Miller (mode = 01).

Figure-9 shows the SOLS based design of the encoding schemes that operates in the Miller mode selected by the mode values as mode0 = '0' and mode1= '1', the data is encoded in the Miller encoding scheme and transmitted based on the UART protocol.

5. CONCLUSIONS

It is suitable for bit streams in radio communications and can be transported using a standard UART. It is simple to encode, decode and has good error detection and can negate the need for 'check-summed' data. This paper not only develops an entirely reusable VLSI architecture, but also exhibits a competitive performance compared with the existing works. By using SOLS technique the hardware utilization rate will be improved. The encoding capability can fully support (Universe) the DSRC standards. The Design strategies of entirecircuits for FM0, Manchester and Miller VLSI architecture have been designed and simulation results are obtained using VHDL language. This design is very effective is short range communication especially in military transport system for secure short range

communication between missile launchers ,military trucks, within military carriages, secure communication in the border security forces. FM0/Manchester/Miller encoder combination was used in many applications like library RFID management systems having advantages like high reliability, automated materials handling, and long life. In the similar way some other applications which use this technique are Supermarkets, E-passports, Transportation and Tracking.

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