VOL. 11, NO. 17, SEPTEMBER 2016 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

DESIGN AND PERFORMANCE ANALYSIS OF ASYNCHRONOUS COUNTER USING FEYNMAN GATE BASED T FLIP FLOP

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ABSTRACT

The design of circuits using reversible logic has resulted in optimization of power dissipation. The reversible computation has found its application in low power circuit design, DNA computing and Quantum computing. Basic reversible gates can be used to realize Boolean functions in reversible logic design. A T Flip flop has been designed in this work and used to implement an Asynchronous counter. The optimized T Flip Flop design has been compared with the existing T flip flop. The design proposes reduced power dissipation and gate delay and is significantly lower than the existing system. The design is developed on Xilinx ISE 9.1i, the simulation was done on ModelSim and Xilinx Xpower was used for power analysis.

Keywords: sayem gate, fredkin gate, Feynmen gate, reversible logic, poer, delay.

1. INTRODUCTION

Reversible logic design has led to the design of logic circuits which consume less power. The data loss that happens in irreversible computation leads to dissipation of energy in the form of heat. The notion behind the reversible logic is to design systems using components that preserve information and can thus potentially run backwards. The reversible logic circuits are designed to reduce the loss of energy. It has been described that for an irreversible logic computation on a single bit, kTln2 joules of energy is lost in the computation, where k is the Boltzmann's constant, t is the absolute temperature at which computation is performed [3]. Bennet showed that there would not be KTln2 amount of energy lost if the system allows reproduction of inputs from the produced outputs [4]. Reversible systems do not lose information and a reversible operation can be performed using reversible logic gates. The reversible logic circuits are used in quantum computation, optical information processing and low power VLSI design.

Reduction of quantum cost, garbage outputs, delay and number of outputs are the major challenges in designing a reversible logic circuit. The work in this paper focuses on designing of a reversible circuit that will have reduced power than the existing works.

2. REVERSIBLE LOGIC GATES

A reversible logic gate is a circuit in which the numbers of inputs are equal to number of outputs and between the input and the output vectors there is a one to one correspondence. The Quantum cost is the measure of optimization of a reversible logic gate and this refers to the cost of circuit in terms of cost of primitive reversible. The reversible logic gates have unused outputs and they are defined as garbage outputs [4].

2.1 NOT Gate

A simplest reversible logic gate is a NOT gate and it is a 1 X 1 gate with a quantum cost of zero and the gate is depicted in the Figure-1 below.

Figure-1. NOT Gate.

2.2 Feynman Gate

Feynman Gate, depicted in the Figure-2 is a 2X2 reversible gate. The input-output relationship is given by $P=A$, $Q=A \oplus B$. It is used as a copying gate and applied for duplication of outputs. It has a quantum cost of one [5]. It can be used as a gate with one garbage output to work in XOR operation.

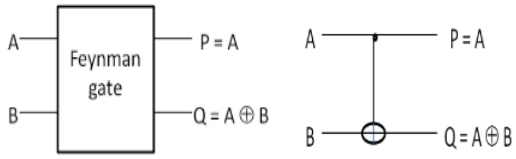

Figure-2. Feynman Gate.

2.3 FREDKIN Gate

A Fredkin gate is a one through reversible logic gate with three ouputs and driven by three inputs. The output of a Fredkin gate is defined as $P=A$, $Q=AB \oplus AC$, $R=A'C \oplus AB$, where A, B and C are the input vectors. It can generate two different outputs. The quatum cost of this gate is five [5]. The Fredkin gate is shown in Figure-3.

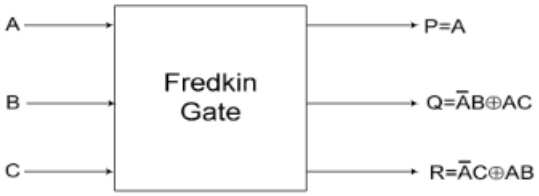

Figure-3. Fredkin Gate.

2.4 TOFOLLI Gate

The Tofolli gate, a 3X3 reversible logic gate is an universal logic gate The quantum cost of a Toffoli gate five [5] and it is shown in the Figure-4. The outputs of Toffoli gate is given by $P=A$, $Q=B$ and $R=AB \oplus C$, where A, B and C are the inputs to the gate.

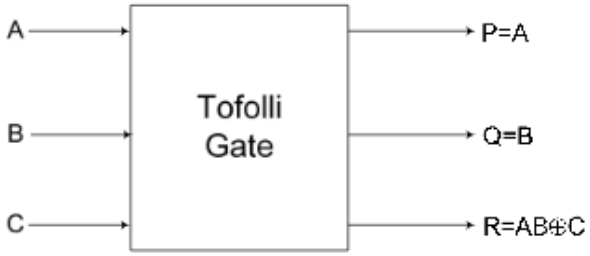

Figure-4. Tofolli Gate.

2.5 SAYEM Gate

Sayem Gate, a 4 X 4 reversible logic gate whose output of which is defined by $Q=A'B \oplus AC$, $R=A'B \oplus AC \oplus D$, $S=AB \oplus A'C \oplus D$ [5]. The Sayem gate also satisfies the universality of a logic gate. The quantum cost of a Sayem Gate is 5[6]. The Sayem Gate is shown in the Figure-5.

Figure-5. Sayem Gate.

3. ASYNCHRONOUS COUNTER DESIGN

Asynchronous circuits are used as interfaces and they act as glue logic that binds the components of a system. Implementation of an asynchronous circuit using reversible logic gates leads to a design of an optimized circuit design improved efficiency.

3.1 Existing reversible T flip flop

The logical operation of T Flip Flop is that the when the input is high, and output toggles and when the input is low, the output is maintained at the same level. The truth table of the T Flip Flop is shown in Table-1.

Table-1. Truth table of T Flip Flop.

T	Qt+1
0	Qt
1	Qt+

The Existing T Flip Flop is designed one Feynman Gate and two Sayem Gates [1]. The flip flop has four inputs and three garbage outputs. The existing design of T flip flop is shown in Figure-6. Three constant inputs, three garbage outputs and the quantum cost is thirteen for the exiting design.

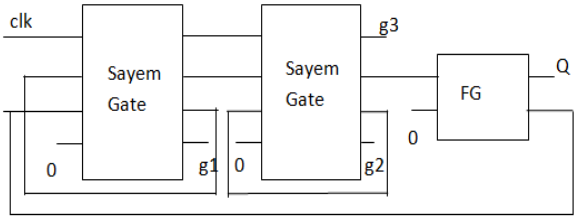

Figure-6. Existing T Flip Flop.

3.2 Power efficient reversible T flip flop

The proposed T Flip Flop is designed as an improvement over the existing design and is designed using Fredkin gates and Feynman gates; the design is as shown in the Figure-7 as below. The designed T Flip Flop has three garbage outputs and two constant input and. The design shows efficient power utilization than the existing design.

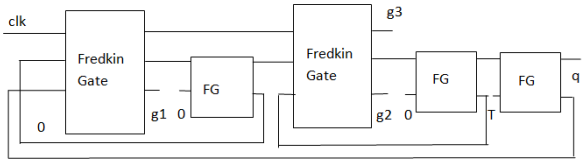

Figure-7. Proposed T Flip Flop.

The T Flip Flop has been used to design an asynchronous up and down counter, the schematic of the T flip flop is shown in the Figure-8.

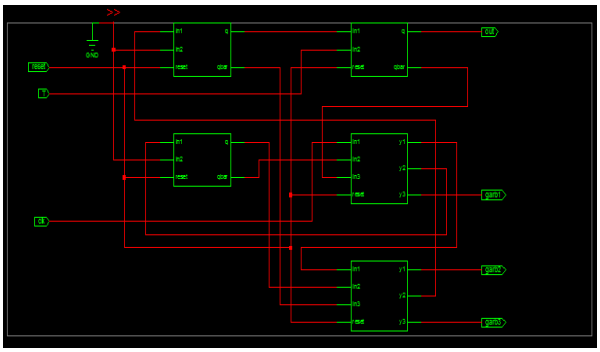

Figure-8. Schematic diagram of proposed T Flip Flop.

3.3 Asynchronous counter using proposed T flip flop

A 4 bit asynchronous up/down counter is designed using the proposed reversible T Flip Flop and it is shown in the Figure-9. The designed T Flip Flop is connected serially with enable logic to make the asynchronous counter function as both up counter and down counter. The enable logic is designed using a

reversible Feynman gate; the enable value is fed into the second input of the Feynman Gate.

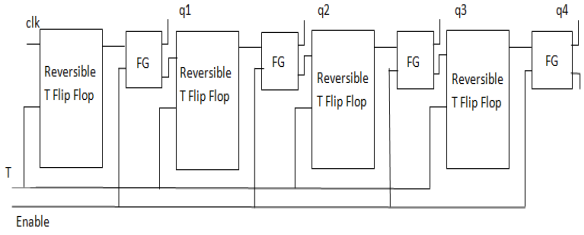

Figure-9. Asynchronous counter using proposed T Flip Flop.

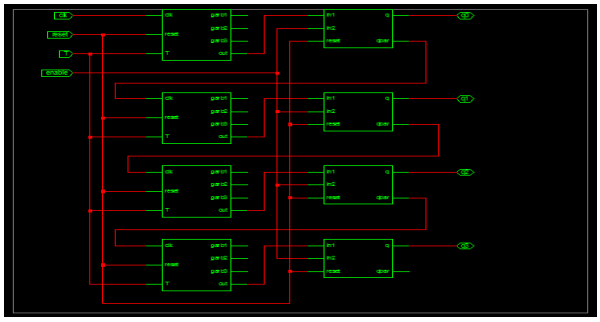

Figure-10. Schematic diagram of Asynchronous counter.

4. SIMULATION AND RESULTS

The counter is designed on Xilinx ISE, the synthesis report from the Xilinx ISE is used to calculate the gate delay which is shown in Table-2. The design is simulated on Altera Modelsim, the simulated output of both asynchronous up counter is shown in Figure-11 and down counter is shown in the Figure-12. The power estimation is done using Xilinx XPower tool with the clock frequency set at 1 GHz. The new counter design's power is compared with the counter design that already exists and the power obtained is shown in the Table-2.

Table-2. Gate delay and power outputs (power calculated at a clock frequency of 1 GHz).

Methodology	**Power** (mW)	**Gate delay**(ns)
Existing Counter	37.47	18.57
Proposed Counter	36.28	14.61

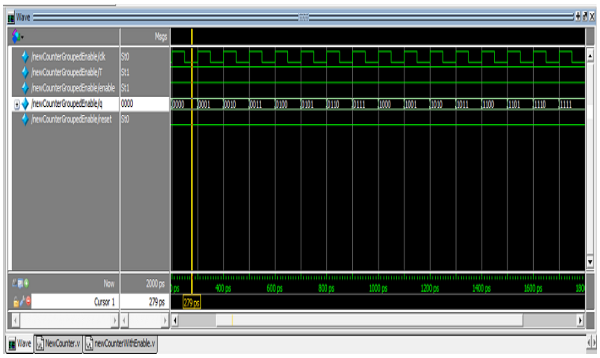

Figure-11. The simulated output of the asynchronous Up Counter using the designed T flip flop.

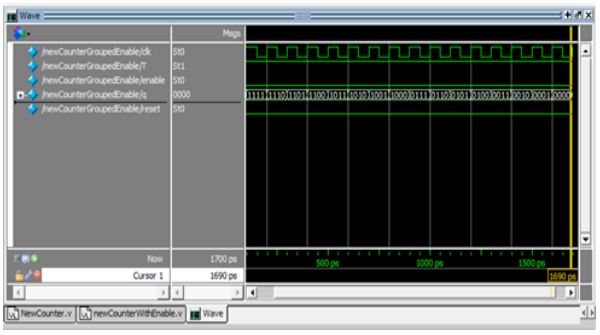

Figure-12. Shows the simulated output of asynchronous down Counter using the designed T Flip Flop.

5. CONCLUSIONS

This work has analyzed the performance of the newly designed T flip flop and its utilized in an asynchronous counter design. The power consumption is reduced when compared with the already existing model and the reduction is also observed in gate delay. The asynchronous up and down counter was summarized in this paper with respect to power and gate delay based on reversible Feynman Gate. The scope of this work can be further extended by designing sequential reversible circuits that will have reduced power consumption, reduced quantum cost and reduced gate delay.

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