



DESIGN AND IMPLEMENTATION OF LASER MISSILE JAMMING SYSTEM USING SPATIAL PARALLELISM ON FPGA FOR BETTER PERFORMANCE AND THROUGHPUT

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ABSTRACT

The current trend in the system development and the competition among manufacturers motivate both the designers and developers to improve the performance of systems and decrease the power consumption but not at the cost expense of those systems. Today, the Field Programmable Gate Array-based embedded systems is considered as the preferred computational platforms due to multi key features of these platforms including the reconfigurability, flexibility, short-time to marketing, and etc. The advanced technologies and the facilities presented via these technologies pushed towards real-time and multi-functional systems, which encourages the designers and developers to replace the single processing unit by those units with the ability to process multiple data per time. Many mechanisms can be applied over the field programmable gate array platforms to provide the ability for multi-processing and the spatial parallelism. Therefore, in this paper, the advantages of applying the spatial parallelism over the Altera Nios II Embedded Evaluation Kit (NEEK) board are presented. The spatial parallelism was used to design and implement a laser missile frequency jamming system. The spatial parallelism is combined with the FPGA features, which improves designed system in many aspects such as increasing the system throughput, decreasing the system cost, the power consumption of the system, and the system complexity. This paper provides a presentation of the system modules, the functionality of each of these modules, and the results obtained from the touch screen of the (NEEK) board.

Keywords: field programmable gate array, spatial parallelism, frequency jamming, embedded system.

1. INTRODUCTION

There has been a hard competition between the giant companies and the need to meet the customers' requirements. Therefore, it is necessary for those companies to consider some key features when designing and implementing their systems. The most important features that should be taken in considerations are the reconfigurability, cost, power consumption, and time to marketing. The field programmable gate array (FPGA) has all of these features and more characteristics including the ability to process data in parallel manner, and reliability [1], [2].

When the functionality of the system is critical and closely related to human life, the ability of these systems to process data in real-time respond and taking an accurate decision-making with lower complexity as much as possible must be considered. The frequency jamming system can be included within this category, where the computational platform for such a system should be accurate, efficient, and robust. In addition, such systems with functionality like the jamming system should be portable and scalable [3]. Nowadays, the processing platforms of the frequency jamming systems have core problems represented in their complexity and the time required for the process signals. The delay of processing can be considered as a natural result for the system design, the power consumed to perform the system functionality and other reasons. For these key reasons and more, these platforms used to implement the frequency jamming functionality is incapable of providing the requirements for effective and fast processing systems. This paper focuses on presenting the aspects which should be

improved in order to increase proposed system performance and throughput. For increasing the system throughput, the spatial parallelism approach was applied to enable proposed system from processing multiple signals per time instead of the processing single signal. Other aspects such as the power consumption, reconfigurability, cost, and portability have been improved via using the FPGA platform as the implementation environment for proposed system. It is proposed that less than four aircraft fighters should use the laser missiles to attack a single target because there is a laser beam interference situation if more than four laser missile have been launched to destroy a single target. Because of that, a laser missile frequency jamming system with the ability was proposed to process four frequency signals per time as well as the ability to control four defused plates to direct the captured frequencies towards the attacking aircraft fighters.

Furthermore, in order to cover all related sub functions of proposed system; we proposed modules which have a close relation to proposed system such as the input signal unit manager being responsible for synchronizing the four input signals, signal emulator module which will generate test signals to check the system functionality when no signals are available, output data buffer module to store the captured and processed signals for later researches sake, and address generation unit which takes a responsibility for generating addresses for the processed data to be stored in the output data buffer.

The paper is organized as follows. Section 2 highlights the related work. Section 3 provides an overview for key design modules in proposed system



which performs the main functionality of the system. Section 4 presents the final results obtained from the system which have been shown on the LCD touch screen of the (NEEK) board. Section 5 presents a brief conclusion and analysis of the results and the system performance.

2. RELATED WORK

The continuous motivation to increase the embedded systems performance enforced the designers as well as the developers to pass over the old fashion mechanisms such as stretching the system clock frequency and harnessing more useful approaches including the parallelism [4]. The spatial parallelism is considered as a core factor to handle the need for increasing the systems performance. Scarce information is available for the design and implementation of frequency jamming since it is known as military confidential documents but the related systems to the frequency jamming as well as the spatial parallelism is reviewed in this section.

The system model proposed by [5] presents a jamming system based on chaotic nonlinear system where the (2-FSK) signals and the third-order Duffing oscillator model were used to be the enemy communication signals. The 2- frequency-shift keying (2-FSK) which is a method used to transmit digital signals was proposed by the researcher to be the enemy signal. This signal after processing by the jamming guide unit will be amplifying its power to be re-transmitted. The proposed system can be implemented using the TMS digital signal processing starter kit (DSK).

The infrared guided missile can be considered as a core weapon in the military field since it can use the reflected energy from the intended targets. [6] proposed a scheme to jamming this kind of missiles. Where the IR missiles have tracking and missile guidance modules, the jamming module presented in this paper includes the signal processing unit and phase detector as well as tracking loop and was designed using MATLAB SIMULINK. The signal processing module detects the frequency using a Band Pass Filter (BPF), whereas the functionality of the phase detector is to capture the signal modulation phase and at the same, generates a signal indicator for the error. Finally, the tracking unit is in simple words to represent a DC motor.

The exploration of the spatial parallelism feature has been used in many levels of the system construction ranging from interconnects used within the system to the entire functional units. The Ethernet-based interconnects was selected by [7] as a potential solution for improving the cost-effectiveness of the systems. The spatial parallelism at interconnects and communication level is exploited. End-to-End or (Multiple Physical links) was used in this proposed scheme which can result in systems that have a scalable feature and lower-cost components. Using the spatial parallelism principle in interconnects and communication levels represented in using multiple (1Gbit/s) links has achieved good results with respect to improving the throughput over low-cost.

The spatial parallelism has been harnessed by [8] to perform a fully stochastic simulation using the FPGA

architecture. The presented architecture is faster than the existing simulator designed and implemented on FPGA with over than 12-30 times.

The spatial parallelism in the hardware part can be used side by side with the algorithm levels like the proposed one by [9], where a fast motion and detection (ME/DE) algorithm has been used jointly at the spatial parallelism hardware architecture. Parallel ME/DE modules and four levels of the Multi-View Coding (MVC) have been harnessed in order to improve the throughput.

3. SYSTEM SPECIFICATIONS

To simplify understanding the system mechanism in order to perform the frequency jamming functionality, it is better to have a look first at proposed top-level design of the system. Figure-1 provides a conceptual illustration of the proposed system:

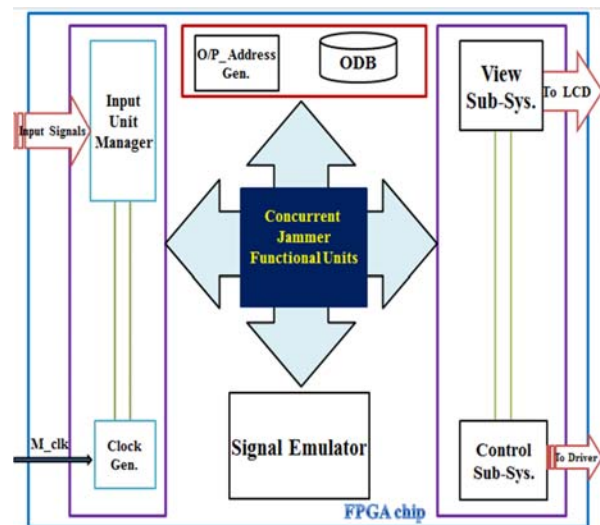


Figure-1. Top level design of laser missile frequency jamming system [10].

As it can be seen, the first step is to receive the input frequency signals to be synchronized first and then to be sent to other modules to perform the frequency jamming functionality. The clock generator module will be responsible for manipulating the (PLL) to provide the system with base frequency up to (200 MHz). The signal emulator module and as its name implies, can generate testing signals to check the system performance. The concurrent jammer functional units is considered as the core of the system because they are responsible for performing the frequency jamming functionality and sent the obtained frequencies to the control sub-system which is capable of controlling multiple jamming platforms. At the same time, the processed data was sent to the LCD touch screen of the (NEEK) board for showing them. Finally, the processed data was stored in the output data buffer for the research purposes. The next sub-sections illustrate the system modules as well as the temporal results obtained from each of these modules.



3.1 Input unit manager

In order to process multiple data per time and to ensure the smooth distribution of the emitted signals from the aircraft fighters, the need to design a module responsible for synchronizing the input signals appeared. Simply, this module is capable of receiving multiple frequency signals and then distributes these signals (specifically 4 signals) over the concurrent jamming units to be processed. The approach used within this module was the multiplexing mechanism.

3.2 Clock generation module

It is known as an issue that the base frequency of the FPGA boards is restricted to (50 MHz). In order to increase this base frequency, a clock generation module which is responsible for providing proposed system with base frequency up to (200 MHz) is designed. The ideal approach to obtain this result is via manipulating the Phase-Locked Loop (PLL) which is a control embedded circuit within the Nios II Embedded Evaluation Kit (NEEK) that its generated output signal phase is related to the phase of an input signal [11]. This logic circuit which has been harnessed by proposed project and this circuit has the ability to perform multiple functions such as the phase shifting, programmable duty cycle, and spread spectrum the input clocking.

3.3 Signal emulator module

In case, when no signals are available, it is necessary to check the system response as well as its throughput. The main function of this module is to provide multiple signals per time to act as the input laser missile frequencies and then check the system throughput depending on these frequencies since that the generated frequencies are known to the operator, so it is so easy to compare the obtained results from the system with those signals generated from the signal emulator module. The performance of this module depends on the behavior of the time and a periodic signal which will be used to test the system. The internal design of this module is shown in the Figure-2.

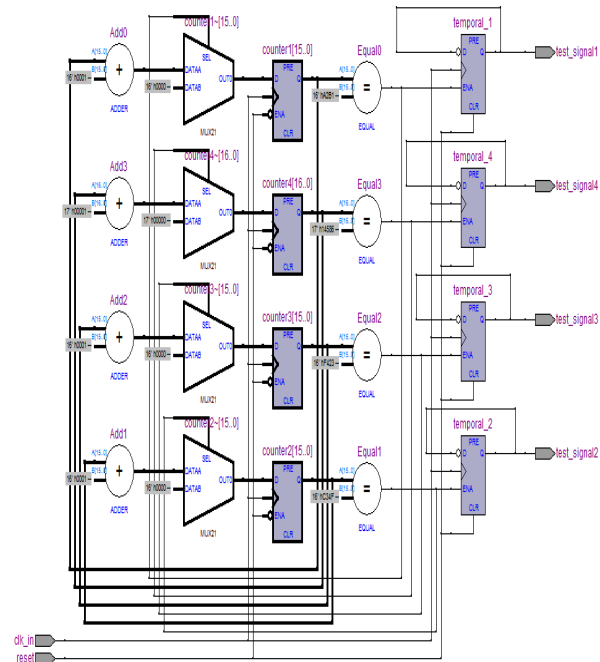


Figure-2. RTL view for the signal emulator.

3.4 Concurrent jamming functional units

The core functionality of proposed system is illustrated in this section. The jamming process was divided into sub-tasks which is done via module in order to decrease the system complexity. The initial step detects the frequencies and then processes these data gradually via other modules until the processed data was sent to the sub-view system and the control sub-system. The core units within proposed system are presented as follows:

a) Frequency capture module

This module in turn has two phases. The first one is the pulse detecting phase being responsible for detecting the number of pulses of each signal, whereas the other phase is the cross frequency detector which has the task to convert these pulses to the frequency form, as illustrated as follows:

The input frequency signals in the “when available” is provided to proposed system via the general purpose input/output (GPIO). Now, in order to detect the pulses embedded within the laser missile frequency, the pulses of the input signal must be counted via determining the width of the time period of the input signal. To do so, once this unit receives the input signal provided from the GPIO and counts the number of the pulses and then processes that signal depending on time period of the master clock of the board. With each clock cycle, the time period of the pulse is calculated, and an internal parameter increases, and then this parameter is assigned at the end to the output. This sub-stage assumes a frequency limit to process the detected input time period. This assumption has not been selected at random but depends on the frequency range that proposed project is able to detect. Once the number of pulses has been calculated, the cross



frequency detector phase begins to convert the detected time period to a frequency representation via the following equation:

$$F=1/T \quad (1)$$

As can be seen from the equation above, the frequency (F) can be calculated depending on the time period (T).

b) Signal conversion module

In order to view the captured frequencies as separate digits over the 7-segment as well as facilitate view these frequencies on the LCD touch-screen of the NEEK board, this module has been created. The detected frequencies are in the binary form and to convert this form to the Binary Coded Decimal (BCD), many algorithms are available; however, the Double-Dabble algorithm (DD) is chosen. Simply, the (DD) algorithm applies the shift and adds 3 approaches, which means shifting the data in binary form one bit to the left and add 3 to this data if the value of the data is (≥ 5) [12]. In this paper, proposed system is capable of capturing frequencies up to (200 MHz), which means that this module is designed in such a way to convert (6-digits) from the binary form to the BCD form. For this purpose, a temporal variable to store both of the frequency in the binary form and the converted digits is used. After the value of this temporal register to zero is initialized, the shifting process begins, whereas the input to this module is shifted to the left with one bit at each time, and at the same time the value of the input data is checked to add (3) to its value if it is (≥ 5) in the binary form. This procedure is iterated until all the input data in the binary form are converted to the BCD form.

c) Distribution module

The output of the previous module is a frequency in the BCD form. This module has the task to convert this frequency with the BCD form to the ASCII form in order to be viewed on the LCD touch-screen of the board as well as multiplex the (6-digits) to send each one of these digits to the LCD at a time. Now, multiple data should be sent to o/p peripherals; the multiplexing is a considerable approach. Depending on this, this module is proposed to send the digits which represent the captured frequency to be view over the LCD one digit at a time. This functionality in general depends on timing the sequence that the signals should be sent in a correct manner, and at the same time identify the destination that the signals should be sent and when to be sent. The 6-BCD digits converted in the last stage will be multiplexed in this module to send a single digit at a time using 3-control signals. At the same time, the selected digit to be sent will be in the ASCII form in order to be viewed on the touch screen of the NEEK board. The figure below highlights partially the internal design of this module via the RTL tool of the Quartus II web edition:

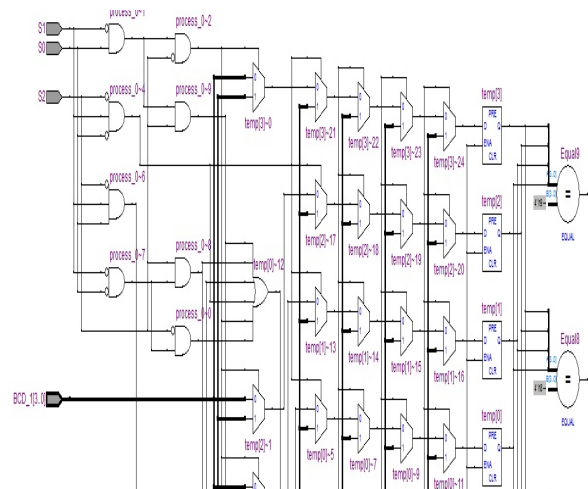


Figure-3. RTL view for the distribution module.

3.5 Concurrent jammer module

The constant pursuit of the designers and researchers is to improve the performance of the systems via speeding up the computation mechanism and increasing throughput but not at the expense of the cost or power consumption. All the functionalities of proposed laser missile frequency jamming system modules was designed and tested via the simulation CAD tool. After this verification phase, the next phase was to apply spatial parallelism concept which has been harnessed to enrich proposed system with ability to process multiple frequency signals per time. The main functionality of this module is to duplicate the functions of each module. This action is enough to decrease the used resources of the FPGA as well as improve the system throughput and performance. The spatial parallelism is used within this module to split the sub-functionalities of the system over multiple modules to be processed.

3.6 View-sub system

After the main functionality of this system has been performed via the previous stage, the need to show the obtained results of the embedded LCD touch screen within the NEEK board pushed towards the creation of this module where it is responsible for transmitting the overall results to the touch screen view unit mentioned earlier. For the general information purpose, the NEEK board's LCD touch screen is a color LCD, which has the ability to view resolution up to (800 * 480 pixel) and also 10-bit VGA digital access card. The mechanism used within this module is all over the Finite State Machine (FSM). Many state machines have been used within this module and for multiple purposes starting from initializing the LCD touch screen itself and preparing it to receive commands to the steps of viewing the results of the system. The processes of viewing the result are divided into three steps. The first one is to view the letters (DET. Freq=), where the first three letters (DET.) refer to the word (Detected), whereas the next four letters refer to the word (Frequency). The next step within this module is to



view the frequency value itself on the LCD where this state machine begins with the first digit sent from the distribution module, then the next state is the next digit and so on until all the digits is fully received and viewed on the board. In the final stage, where the characters (KHz) were displayed on the LCD touch screen.

3.7 Control-sub system

The main purpose to design this system was to jam the laser missile frequency signals used to guide the missiles to a specific target. In order to handle multiple jamming signals, there is a need to control the multiple jamming platforms. This module is responsible for controlling four jamming platforms. The most effective mechanism to control these platforms is using the Pulse Width Modulation to control the speed of the motors of these platforms and direct these platforms towards the attacking aircraft fighters. At the same time, the jitter time was reduced when using the PWM approach with the motors as well as increasing or decreasing the pulse width can organize the energy which is flowed to the motor shaft [13]. When the interfering between the beam lasers happens, the accuracy of the guidance can decrease. Depending on that, this module simulated the situation where four aircraft fighters are attacking a single target. The PWM used digital signals instead of the continuous signals for the controlling purpose. The proposed control module is of eight speeds, the effectiveness of the control module is highlighted in the table below:

Table-1. Pulse width modulation effectiveness [10].

Module states	Percentage of effectiveness
PWM 0	0 %
PWM 1	15 %
PWM 2	30 %
PWM 3	45 %
PWM 4	60 %
PWM 5	75 %
PWM 6	90 %
PWM 7	100 %

3.8 Storing-sub system

This module consists of output data buffer as well as addresses generator. The output data buffer was built using the dual channel technique for enabling the reading and writing process. The main purpose of designing this module is to store the captured frequencies for the research purpose. The other part of this module is a small address generation unit to allocate addresses to the data.

4. RESULT AND SYSTEM EVALUATION

In this section, the results of proposed laser missile frequency jamming system were collected and highlighted. In this paper, results are divided into two parts. The first one can be considered as the verification

part where the results of each module of proposed system was tested using the (Quartus II web edition) CAD tool, where the second part highlights the results shown on the LCD touch screen of the NEEK board, and this part is considered as the implementation phase.

For the signal emulator module, the result obtained via the CAD tool is illustrated in the figure below:

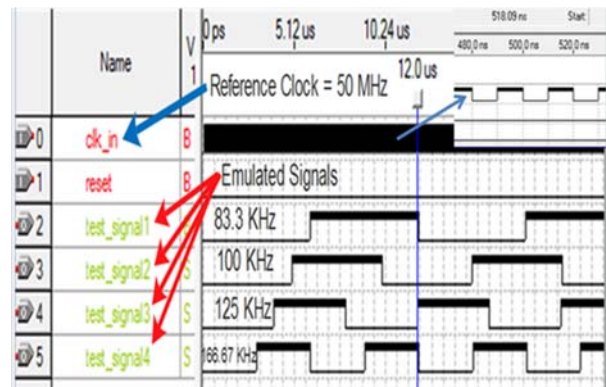


Figure-4. Emulated signals via signal emulator module. [10].

The results obtained via the frequency detection module for the signals (83.3 KHz, 100 KHz, 125 KHz, and 166.67 KHz) are shown below respectively:

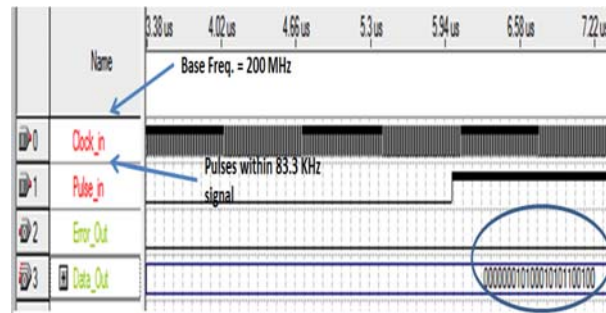


Figure-5. The Detected frequency by the frequency detection module for (83.3 khz) signal. [10]

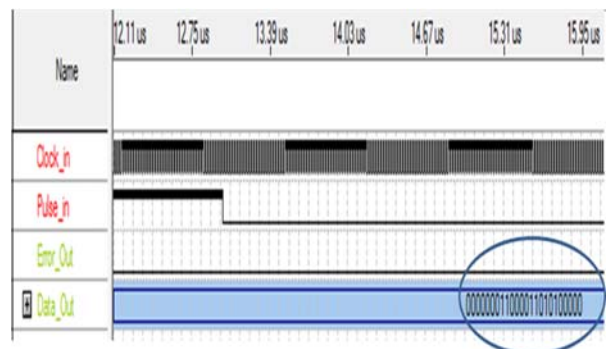


Figure-6. The detected frequency by the frequency detection module for (100 khz) signal.

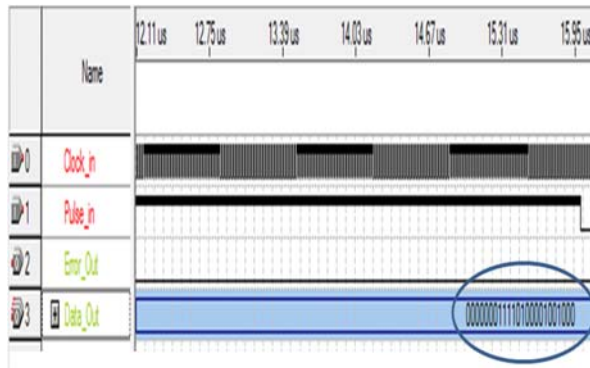


Figure-7. The detected frequency by the frequency detection module for (125 khz) signal.

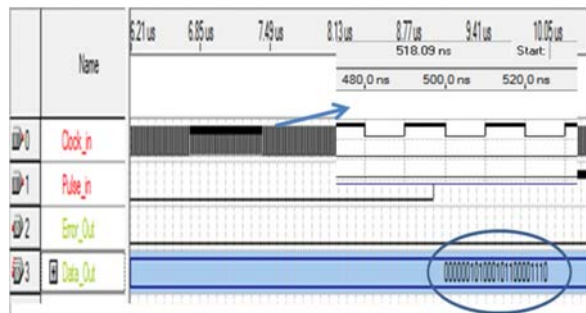


Figure-8. The detected frequency by the frequency detection module for (166.67 khz) signal.

As can be seen from the Figures 5, 6, 7 and 8, the results are in the binary form, and they are converted into the BCD form. Figures 9, 10, 11 and 12 show the signal conversion module bits stream.

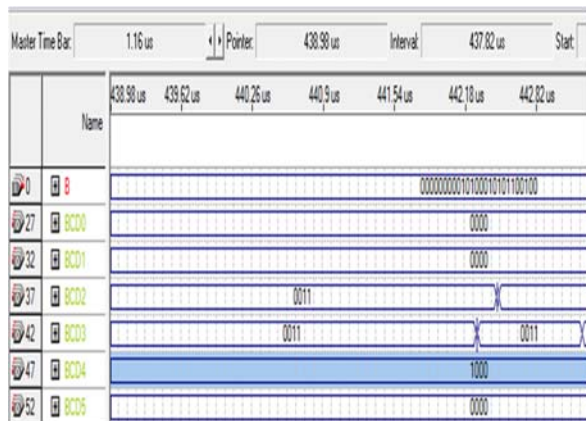


Figure-9. The converted signal by the signal conversion module for (83.3 khz) signal. [10].

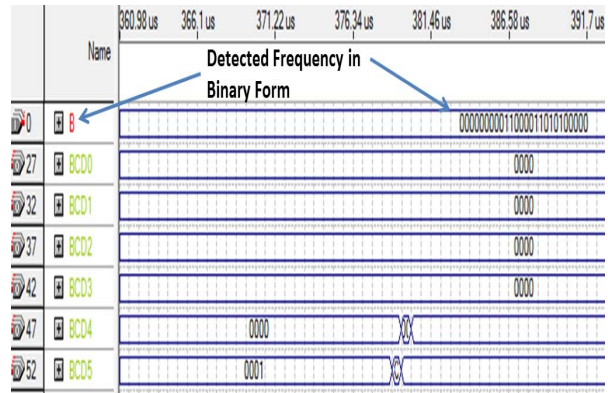


Figure-10. The converted signal by the signal conversion module for (100 khz) signal.

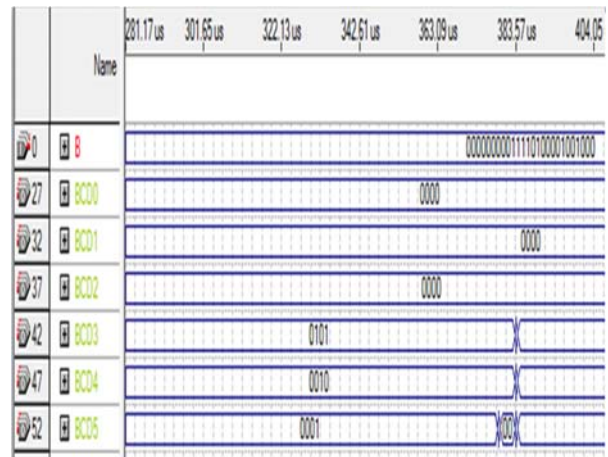


Figure-11. The converted signal by the signal conversion module for (125 khz) signal.

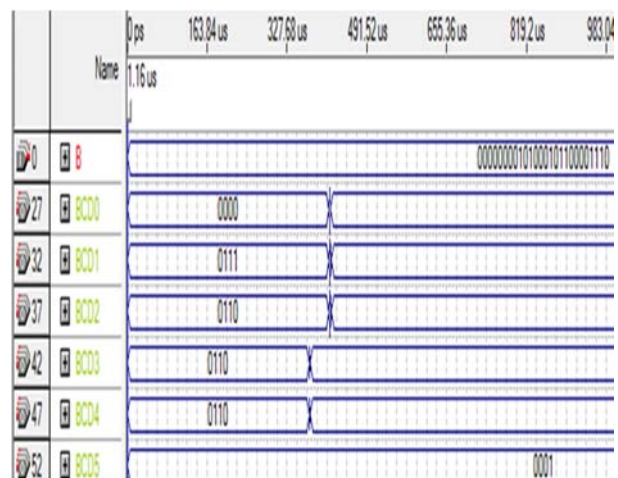


Figure-12. The converted signal by the signal conversion module for (166.67 khz) signal.

Figure-13 shows the distribution module bits stream and output signals.



Figure-13. Converted and distributed frequencies sent to the lcd touch screen.

To control the jamming platform, the control sub-system was designed, and the result of this module is illustrated in Figure-14.

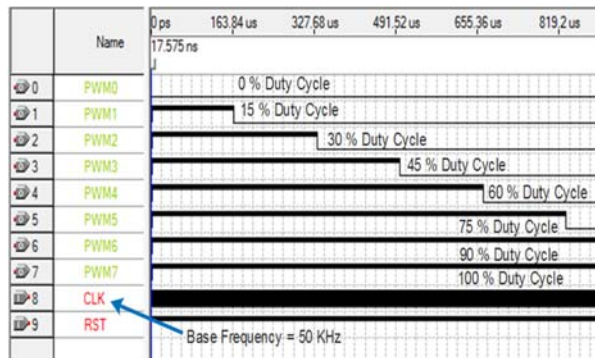


Figure-14. The modulated signals result.

On board testing is done by using NEEK board and the detected frequencies are shown on attached

multimedia LCD touch screen board as shown in Figures 15, 16, 17, 18, 19 and 20.



Figure-15. Multi-signals processing result.



Figure-16. Result of signal (100 khz) on the lcd touch-screen.



Figure-17. Result of signal (100 khz) on the lcd touch-screen using frequency generator.



Figure-18. Result of Signal (125 KHz) on the LCD Touch-Screen.



Figure-19. Result of Signal (125 KHz) on the LCD Touch-Screen using Frequency Generator.



Figure-20. Result of Signal (83.3 KHz) on the LCD Touch-Screen. [10].

5. CONCLUSIONS

In this paper, we focused on how to perform jamming for the emitted frequencies and implement this scheme on FPGA. It starts from the frequency detection itself background based on how to detect the pulses within the signal.

Many features within the Altera® Nios II Embedded Evaluation Kit, Cyclone III Edition were harnessed to implement this project such as the LCD touch screen alongside with the switch inputs and LEDs. The final design of the frequency jamming system confronted multiple improvements and reconfigurations to reach the desired results. In fact, the obtained results from the hardware implementation were much faster in comparison with the results obtained from the software implementation of the system. The system performance had a quantum leap when the FPGA chip unique characteristics and spatial parallelism principle applied over the system. The FPGA chip provided the system with abilities comes in the forefront the flexibility, re-configurability, and reliability. Considering the obtained results, it can be concluded that applying the spatial parallelism principle enabled the system modules to process multiple data per time to perform multiple outputs and this decrease the overall system complexity as well as increasing the modules utilization.

Depending on the results shown on the LCD touch screen, the exploitation of NEEK board enhanced proposed system performance in many aspects like the speed as well as the flexibility in the implementation of the design; whereas the NEEK shows the desired results even when there was a noise within the input signals. The research results show that the real time processing for multiple signals at a time can be done, and it can be concluded that the spatial parallelism can be considered as a solution for those embedded systems which requires real-time processing feature. Furthermore, it is known that many embedded systems are confronting real challenges represented in the constraints over the system resources such as the allowed memory size within the system, power consumption, and speed. Depending on that and even more, the FPGA chip was selected to be the hardware platform in order to overcome these issues.

Finally, it should be mentioned that the hardware design of the proposed laser missile frequency jamming system. The results confirmed that the system has a high throughput for detecting the frequencies and processing these frequencies to be sent to defused platforms as well as to be shown on the LCD touch screen, and all that was done with a low hardware resource utilization.

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