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ANALYSIS OF CMOS IMAGE SENSOR BASED TIME TO THRESOLD PWM ARCHITECTURE USING CURRENT MODE LOGIC

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ABSTRACT

CMOS image sensor (CIS) VLSI architecture based on time to threshold pulse width modulation an era of processor which habituated on the successful representation of low power and high speed applications. This paper deals with current mode logic based PWM architecture which dealt with various analysis of power, delay and power delay product.The pixel circuit will perform in many switched devices to reduce the leakage of current and it can do the power consumption also. It can be connected to time to threshold converter to reduce the power consumption.

Keywords: PWM Architecture, current mode transmitter, power, delay.

1. INTRODUCTION

PWM (Pulse width modulation) is one of the modulation technique used to encode a message into a pulsing signal. Although this technique can also be used to encode information for transmission purpose, its main use is to allow the control the power supplied to electronic devices, especially to inertial loads such as motors. In addition, PWM is one of the two principal used in photo-voltaic solar battery chargers the other being maximum power point tracking. The average value of voltage and current fed in the load is controlled by turning the switch ON in between supply and load on and off at fast rate. After long time the switch is on compared to the off periods, the higher the total power supplied to the load.

2. METHODS OF PWM

2.1 PWM in FPGA process

By the concept of pulse width modulation (PWM) in power electronics control system is not new; there are many approaches for improving pulse width modulation. Different digital circuits can generate PWM signals, but the interesting accepts is, by using Hardware Description Language to generate pulse width modulation (VHDL) and applying it on FPGA. FPGA developing of PWM is selected because these can process information faster, controller architecture, hardware design flexibility, design reuse. Pulse-width modulation (PWM) is a technique that can controls the width of the pulse, formally the pulse duration. The word duty cycle describes the proportion of 'on' time to the regular interval or 'period' of time; the term a low duty cycle is related to low power, because the power the power can be off for most of the time. Duty cycle can be expressed in 100% being fully on.

PWM is a modulation technique which can provide a logic “1” and logic “0” for a controlled period of time. PWM is a signal source that involves in the modulation of its duty cycle. It is a constant period square wave with a varying duty cycle. PWM signal has stable frequency but the time the signal varies high. PWM is the process that causes shift in the range of frequencies in a signal. PWM may be varied from 0 to 100% in ON time. The width of pulses are proportional to the input signal. When signal is small, the series of narrow pulses are generated. When signal is large, a series of large pulses are generated. The frequency of a PWM signal is remains same but the time the signal varies high as shown in Fig.1. The duty cycle is given by τ/T.

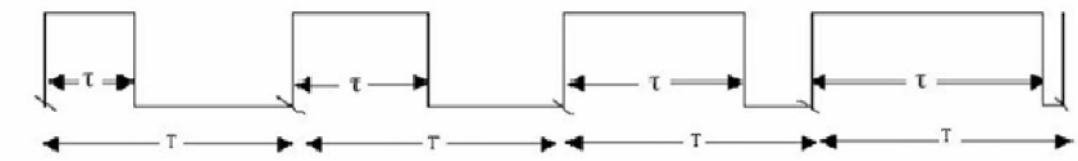

Figure-1. PWM signal with different duty cycles.

FPGAs are configurable ICs (user can design, program and make changes to his circuit whenever he wants) and used to implement logic functions. Today’s FPGAs can hold several millions gates and have some significant advantage. They ensure ease of design, lower development costs and the opportunity to speed products to market. FPGA are programmable semiconductor devices that are based around a matrix of configurable logic block (CLBs) connected via programmable interconnects. FPGA can be programmed to the desired application or functionality requirement.

2.2 PWM processor

In conventional CIS, the output from a pixel is analog. To realize smart functions such as current mode, digital mode or pulse processing modes have been introduced as options. Digital and pulse mode image sensors having a good fill factor are, however, difficult to

achieve. The approach pursued in CISs based on pulse width modulation (PWM) architecture incorporates a CMOS inverter as a comparator within a pixel. The technique creates additional pixel area allowing to the incorporations of the additional process circuitry [1]. Eklund*et al.* [2] adopted an inverter as a light intensity to time convertor. A single inverter as a comparator based on single-photon avalanche diodes was also introduced in [3]. Niclass and Rochas [4] implemented a similar architecture based on time-of-flight for 3-D vision system. Culurciello [5] he proposed a biologically inspired readout method to implement a biomorphic digital image sensor where inverters were adopted a comparator to generate a spike (a 1-bit pulse) derived from the photodiode (PD) output.These approaches have relatively low fill factor and hence their performance is compromised in low-voltage applications.

On-chip autonomous wireless security cameras and disposable medical imaging systems and the like require adoption of technologies that can operate under low voltage, consume low power and are compatible with deep submicron processes. Therefore, instead of using the more conventional APS, PWM imaging has become a popular approach that overcomes the limited signal swing encountered under low-voltage operation. Kagawa *et al.* achieved 3.6 pw/frame pixels with 1.35 V supply voltage using dynamic pixel-by-pixel readout approach. Proposed threshold variation noise cancelling scheme with high dynamic range and 2.98 pw/frame pixel under 0.5 V supply voltage. Employed an in-pixel two-transistor comparator with column-shared current limiter that gave 23.4 Db of SNR at 0.5 V supply voltage and consuming 8.6 pw/frame pixel.

Achievement of the ultralow power consumption, however, requires aggressive supply voltage scaling and the need for introduction of control techniques that consequently limit the frame rate. This approach is susceptible to supply voltage variation. In this concept, we present a novel CIS VLSI architecture that uses a single-inverter time-to-threshold PWM circuitry incorporating an offset reduction scheme fabricated using 130-nm CMOS technology. The significant feature of the imager is that it operates successfully at a supply voltage as low as 330 Mv while retaining a SNR of 24 Db because of the pixel's the pixel dissipates only 5.9 Nw while keeping a dynamic range of 54 Db at 7.8 fps under 500-Mv supply voltage.

2.3 CMOS digital image logical architecture

2.3.1 Time-to-threshold PW Mimager architecture

The logical architecture for the time-to-threshold PWM imaging system is shown below. It includes PWM pixel array, control circuits, and TTC. Timing waveforms of pixel integration including reset and enable phases, and time-to-threshold conversion based on row-by-row operation are shown in Figure below. In $M \times N$ CIS array, a pixel $P_{i,j}$ is in readout mode when the row signal reset I is low and the row enable is high.

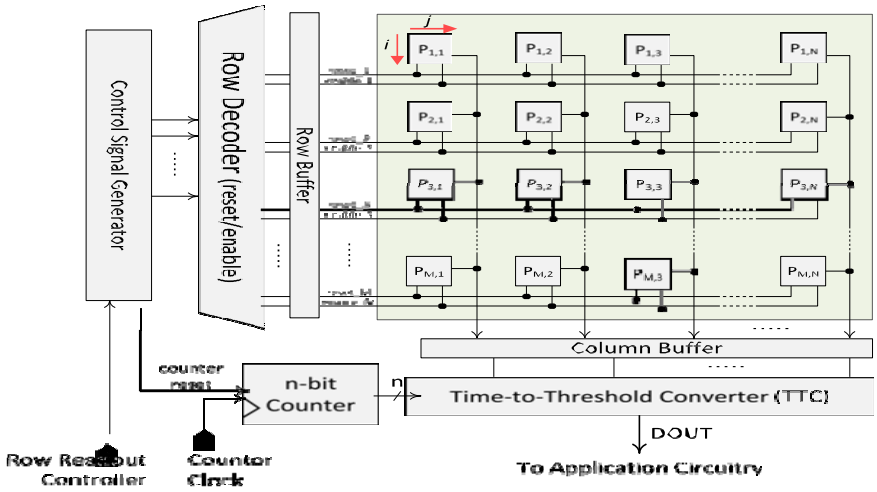

Figure-2. PWMarchitecture.

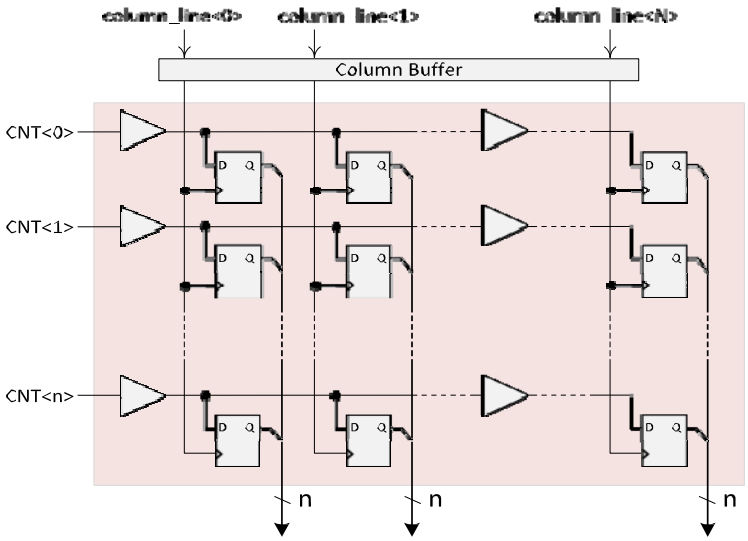

Figure-3. Time to threshold converter.

2.3.2 Time to threshold converter

2.4 PWM based CIS

The fundamentals of image acquisition sensor architecture based on PWM an extension of pulse modulation (PM). In this construct, the output signal is produced whenever the signal reaches a threshold value. The digital form of output is compatible for asynchronous operation such as various self-resetting schemes. Because the PM sensor acts as an ADC, the architecture is highly suitable for on-chip signal processing applications [7], [8]. A column line of the PWM readout is driven by digital form of a comparator having a higher drive current than a source follower of the 3T APS. This facilitates the output signal to be more identifiable.

2.5 Comparator structure using signal-inverter CIS

The pixel-based CIS architecture uses a single-inverter sensor circuitry. The basic pixel structure shown figure, includes a PD, a single CMOS inverter, two reset Nmos transistors' M1 and M2, and the two Nmos transistors M3 and M4 to enable the pixel output.

The operation is initiated with the reset signal being asserted. Node PD commences to charge up toward $+V_{DD}$, followed by the integration phase whereby the reset is switched to logic 0 and the enable signals is switched logic The PD enters a floating mode during this period. Upon illumination on PD, the photocurrent created by generation of electron–hole pairs results in the voltage $+(V_{DD}–V_{TH})$ at node PD to decrease as a function of the intensity of incident light that falls on the PD. The node voltage PD drives the inverter for time-to-threshold modulation. By careful geometric considerations, it becomes possible to minimize the deviation of the logic threshold voltage that may be encountered as the result of process parameter variations. Associated gain of the inverter is large and therefore the inverter gain will have a minor effect on the process variation. The inverter in sub micrometer technology ensures that the threshold variation is minimal assuring stability at low power supply [9].

The $t_{trigger}$ shown in Figure-3(b) is determined by the level of illumination, which is converted to a voltage level, thus establishing the time-to-threshold PWM for analog-to-digital (A/D) conversion. High illumination results in faster voltage drop, whereas low illumination makes the discharge slower. The output of the inverter is mapped to corresponding dig-ital pulses with variable width according to the change of the voltage at PD node. The time-to-threshold conversion is incorporated at the end of column lines to realize digital data instead of deployment of the more conventional ADC.

2.6 Pixel characterization

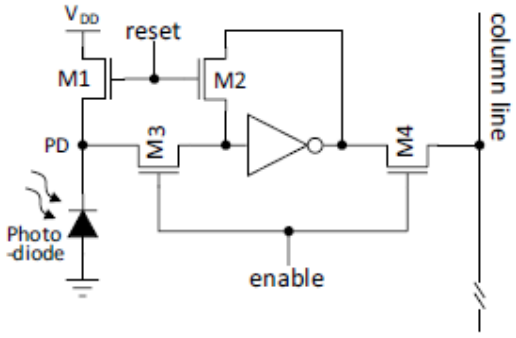

Figure-4. Pixel circuit.

Local variations in threshold voltage are not negligible, and can cause differences in performance between two neighbouring pixels. The differences between the individual pixels in the array result in variations in the analog readout, which culminates in the fixed pattern noise (FPN). The two important sources of errors are: 1) variation in gain and 2) offset of the comparator. Because

the gain in the comparator is large, the local gain variation will have a minor effect. However, the PD gain, namely the sensitivity to illumination and the leakage current, are difficult to control. Therefore, the comparator offset is the only parameter available for optimization. M2 reduces this offset to a significant degree. The simulation result for the pixel with M2 and without M2. During reset, input and output nodes of the inverter are recharged at $+V_{DD}/2$ thus reducing the offset voltage between input and output of the inverter by providing the same amount of charge to the intersection of M2, M3, and the inverter input at the commencement of enable phase. M2 effectively enhances the pixel response at low illumination and hence a noticeable improvement in the dynamic range (DR) is achieved.

2.7 Current mode logic

In the proposed methodology such as proposed modified PWM architecture by connecting the current mode transmitter to the PWM circuit.

Current mode logic (CML) or source-coupled logic is a differential digital logic family intended to transmit data at speeds between 312.5 Mbit/s and 3.125 Gbit/s across standard printed circuit boards. CML termination scheme.

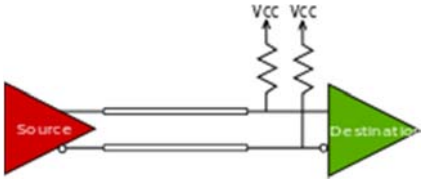

Figure-5. CML termination scheme.

a) The transmission is point-to-point, unidirectional, and is usually terminated at the destination with 50 Ωresistor to v_{cc} both differential lines. CML is frequently used in interfaces to fibre optic components.

b) CML signals have also been found useful in connection between the modules. CML is the physical layer used `in DVI and HDMI video links, the interfaces between a display a controller and a monitor.

c) This technology has widely been used in design of high speed integrated systems, such as telecommunication systems (serial data transceivers, frequency synthesizers, etc.).

d) The fast operation of CML circuits is mainly due to their lower output voltage swing compared to the static CMOS circuits the very faster current switching taking place at the input differential pair transistors.

2.8 Current mode transmitter and distribution

In order to integrate the PWM, a Tx provides a push-pull current into the clock network and distributes the required amount of current to each PWM.TheTx receives a traditional voltage CLK from a PLL/clock divider at the root of the H-tree network and it supplies the pulsed current to the interconnect model which is held at a near constant voltage. The clock distribution is a symmetrically H tree withan equal impedances in each branch so that current is distributed equally to PWM Architecture.

The pulsed current Tx in Figure-6(a) is similar to previous Tx circuits but uses a NAND-NOR design. The NAND gate uses the CLK signal and delayeda inverter CLK signal, clkb, as inputs to generate a small negative pulse to briefly turn on M1. Hence, the PMOS transistor briefly sources charge from the supply while the NMOS is off. Similarly, the NOR gate utilize the negative edge of the CLK and clkb signals to briefly turn on M2. Hence, the NMOS transistor briefly the current sinks while the M1 is off. The non-overlapping input signals from the NAND-NOR gates remove any short circuit current from Tx.

The Tx M1 and M2 device sizes are adjusted to supply/sink charge into/from the CDN. Depending on the size of load (number of sinks) and the size of chip, the device sizes need to be adjusted. The root wires of the CDN carry current that is distributed to all branches so the sizing of CDN wires are critical for both performance and reliability. If the resistance of the wire is too high, the current waveform magnitude and period will be distorted. The wire width must also consider electro migration effects while carrying a total current to drive all the FFs with the required current amplitude and duration.

3. SIMULATION WAVEFORM OFPWM ARCHITECTURE USING CURRENT MODE LOGIC

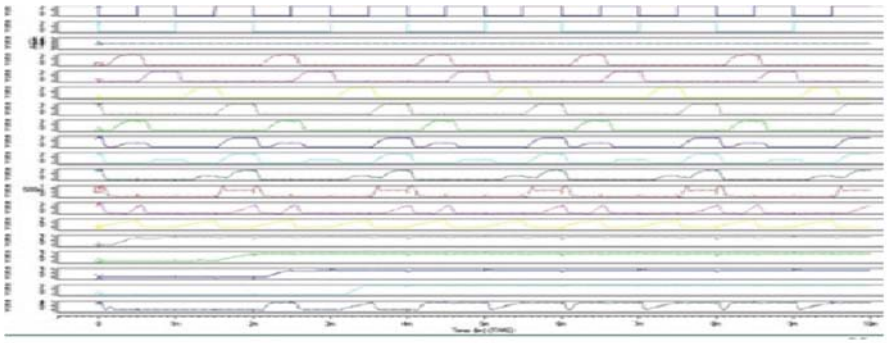

Figure-6. Pulse width modulation simulation waveform.

4. PERFORMANCE ANALYSIS

Table-1. Comparison of existing and proposed PWM architecture average power in 130nm CMOS technology.

Device	Average power (Watts)
PWM Architecture	2.104e-03
PWM With Current Mode Logic Transmitter	1.738e-03

Table-2. Comparison of existing and proposed PWM architecture delay time in 130nm CMOS technology.

Device	Delay time (Seconds)
PWM Architecture	5.238e-04
PWM With Current Mode Logic Transmitter	2.503e-03

Table-3. Comparison of existing and proposed PWM architecture power delay product in 130nm CMOS technology.

Device	Power delay product (Joules)
PWM Architecture	42.324e-8
PWM With Current Mode Logic Transmitter	4.350e-6

Above Table1, 2 and 3 shows the comparison analysis of PWM architecture with current mode logic.

5. CONCLUSIONS

The current mode logic transmitter is connected to pwm architecture through the output of the transmitter is connected to input of the pwm architecture. The current mode logic function is to reduce the power consumption and its converts the current to voltage signal. The decoder is near to output of the transmitter and its does change a code into no. of signals and it's directly connected to pixel circuit. The pixel circuit will perform in many switched devices to reduce the leakage of current and it can do the power consumption also. It can be connected to time to threshold converter to reduce the power consumption and output will be displayed. Analyzing PWM Architecture modified by applying current mode using H- spice tool.

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