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PERFORMANCE ANALYSIS OF AN EFFICIENT FFT PROCESSOR USING LEAKAGE POWER REDUCTION TECHNIQUE

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ABSTRACT

FFT processors are involved in a wide range of applications today. Not only a savory important block in digital TV, broadband systems, but also in areas like radar, medical electronics, imaging and the SETI project(Search for Extra-terrestrial Intelligence). FFT is used in everything from broadband to 3G and Digital TV to radio LAN's. Due to its heavy computational requirements, it occupies large space and consumes more power in hardware. In these FFT processors there will leakage power so to reduce these leakage power we are implementing some of the low power techniques. The main parameters such as power, delay and power delay product of FFT processor are analyzed using 130nm technology. The FFT processor is implemented by modified sleepy stack approach which is having low leakage power. All three parameters are measured and examined for proposed FFT processor and its components using HSPICE tool in 130nm technology. As a result of this, it is concluded that the leakage feedback technique shows a better performance by reducing the leakage power efficiently. The resultant architecture can be used for many low power applications in digital electronics.

Keywords: FFT processor, leakage power, sleepy stack approach, modified sleepy stack approach, average power, delay time, power delay product.

INTRODUCTION

From the past two decades, Complementary Metal Oxide Silicon (CMOS) technology is playing a very important role in the global integrated circuit industry. MOSFETs offer the compelling advantage that they draw almost zero control current in idle state. They come in two flavors: nMOS and pMOS, using n-type and p-type silicon, respectively. The metal oxide semiconductor Field Effect Transistor (MOSFET) is based on the modulation of charge concentration by a pMOS or nMOS capacitance between body and gate electrodes which is located above the body and insulated from all other device regions by a gate dielectric layer. But in this case MOSFET act as an oxide such as silicon dioxide. FFT processors are used in a large range of applications today. Most of these systems are real time application systems, which mean that the systems produce the result in a particular time. The working of FFT calculations are more and a better approach than a general purpose processor is necessary, to satisfy the requirements at a reasonable cost. The major concern for researchers is to fulfil real-time processing techniques and to reduce hardware complexity mainly with respect to power and to improve speed of processor. There are different types of FFT processors and some of the examples of them are Memory based architectures, Cache memory architectures, Array architectures, Pipelined architectures, Sequential, Parallel, Parallel Iterative, Array Architecture. Power consumption of CMOS consists of dynamic and static components. Dynamic power is used when transistors are switching and static power is used regardless of transistor switching. The power leakage has become an important consideration due to the increased integration, operating speeds and the explosive growth of battery operated appliances. One of the main reasons causing the leakage power increase is sub-threshold leakage power. When technology feature size decreases, supply voltage and threshold voltage also decreases but sub threshold leakage power increases exponentially as threshold voltage decreases. To solve the power leakage problems researchers have implemented different ideas from the device level to the architectural level and above. We have introduced low power technique in FFT processor to reduce the leakage power.

EXISTING METHODOLOGY

As we consider FFT processor which is the main part of our project in which the main goal is to reduce leakage power by implementing power reduction technique. We considered a FFT processor [4] as shown in Figure1 in which Supply voltage scaling has been extensively used in FFT processors to improve energy efficiency. In order to verify the output data quality degradation of FFT caused by SRAM failures, we use radix-2, 8K FFT processor, which consists of two radix-2 modules and 8K-word (24-bit) single-port embedded SRAM memory. In the FFT process, the outputs of each radix-2 module are temporarily stored in the embedded SRAM memory devices, and the stored data are read again for the next iterations. In this FFT processor we have to implement low power technique. There are many low power techniques in which we have to choose the best in them and apply the best one in the FFT processor. In this FFT processor there are several components such as a RAM, ROM unit for the storage of data, address generation unit, butterfly processing unit and a sequential control unit. The dualport RAM is used to store input data, intermediate results and output data. Twiddle factors are stored in ROM. The address generation unit generates the address for reading data for butterfly operations and

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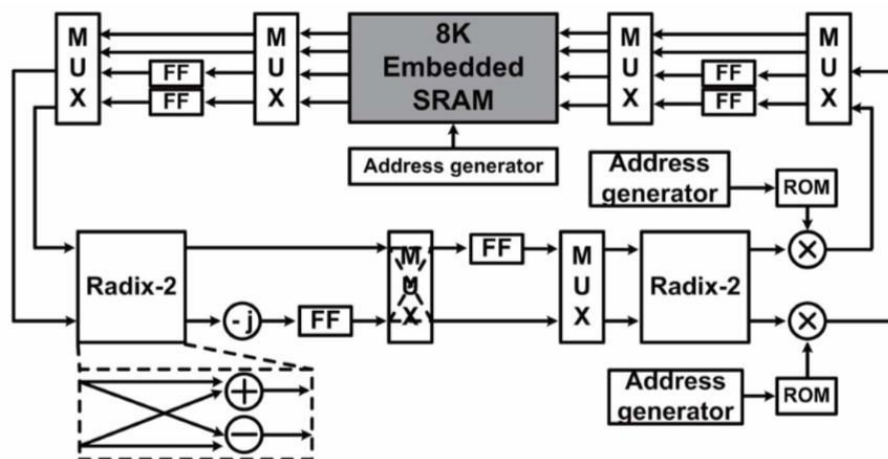

Figure-1. Block diagram of FFT Processor.

also for storing the output data results in RAM. Sequential control unit generates the control signals for each module. In each of these blocks we have apply low power technique to get the better results.

POWER REDUCTION TECHNIQUES

In today's technology, the main contribution to static power consumption of a CMOS circuit is sub threshold leakage. Since sub threshold current increases exponentially as the threshold voltage decreases, deep submicron technologies with scaled down threshold voltages will severely suffer from leakage power consumption. In addition to this leakage power, another contribution to leakage power is gate-oxide leakage power due to the tunneling current through the gate-oxide insulator. The gate-oxide thickness will be reduced as the technology decreases; deep sub-micron technologies will also suffer from gate-oxide leakage power. As CMOS technology rapidly improved to support large chip sizes, the issue of power consumption became very critical. CMOS technology has firmly established itself as the dominant VLSI technology for the most recent years, leakage power dissipation has become an overriding concern for VLSI circuit designers. For better understanding we have studied some of the low power techniques as explained below.

SLEEP APPROACH

In the sleep approach, [14] both an extra 'sleep' PMOS transistor is placed between VDD and the pull-up network of a circuit and an extra 'sleep' NMOS transistor is placed between the pull-down network and GND [8]. These sleep transistors turn off the circuit by blocking the power rails. Figure 2 shows its structure. The sleep transistor turns on during the active mode and turns off during the idle mode. By blocking the power source, leakage power reduces effectively. However, output will be in floating state after sleep mode, so the technique results in destruction of state and a floating output voltage.
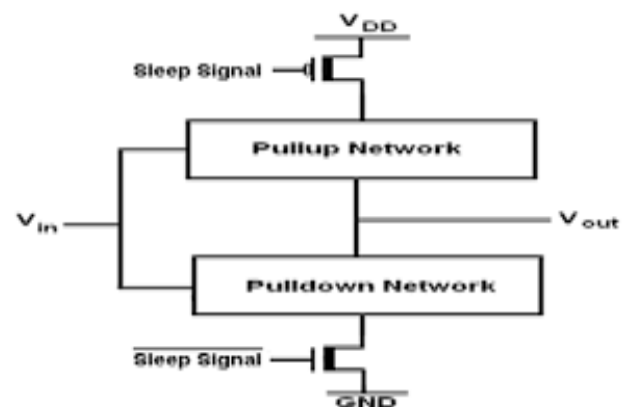
Figure-2. Sleep approach.

STACK APPROACH

In this approach,[10] stack effect takes place by breaking down an existing transistor into two half size transistors. Figure 3 shows its structure. When the two transistors are in off state at the same time, induced reverse bias between the two transistors results in sub threshold leakage current reduction. But these divided transistors increase delay significantly and could limit the usefulness of the approach.
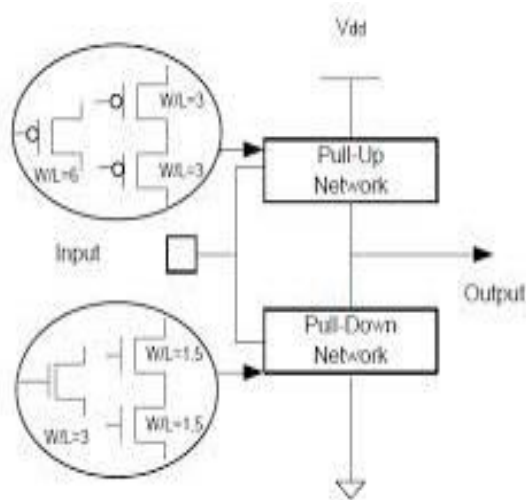
Figure-3. Stack approach.

ZIG-ZAG APPROACH

The zigzag approach[6] reduces wake-up overhead caused due to sleep transistors placement by replacing a particular pre-selected input vector. In Figure-4, assume that in sleep state, the input of the logic is '0' and each logic stage reverses its input signal, i.e., the output is '1' if the input is '0,' and the output is '0' is the input is '1.' If the output is '1,' then a sleep transistor is added to the pull down network; if the output is '0', then a sleep transistor is added to the pull-up network. Therefore this approach uses only few sleep transistors than the original sleep approach. Even though this approach results in destruction of state (i.e., state is set to the particular pre-selected input vector), although the problem of floating output voltage is eliminated.
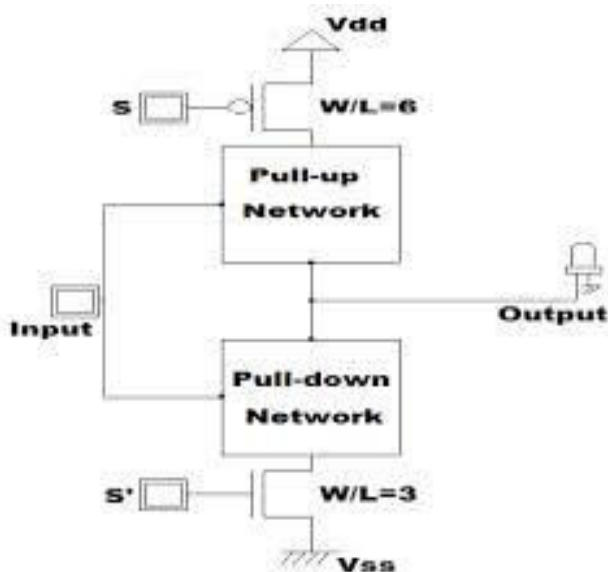

Figure-4. ZigZag approach.

SLEEPY STACK APPROACH

The sleepy stack approach combines the sleep and stack approaches [3]. The sleepy stack technique

divides existing transistors into two halves like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. Figure-5 shows its structure. During sleep mode, sleep transistors are turned off and stacked transistors decreases leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors reduces the resistance path, so delay is decreased during active mode. However, area penalty is a matter to be considered for this approach since every transistor is replaced by three transistors and additional wires are added for S and S', which are sleep signals.
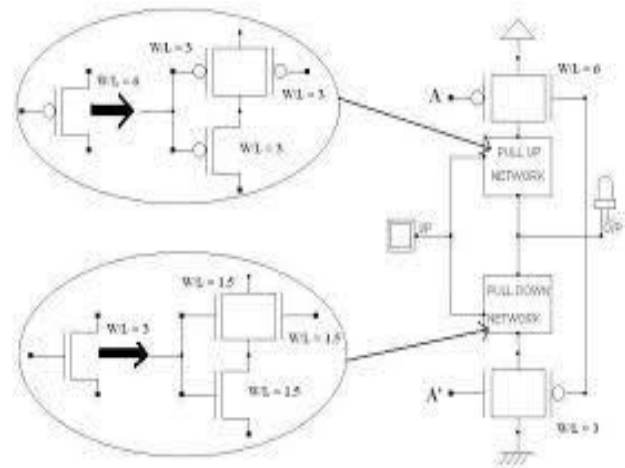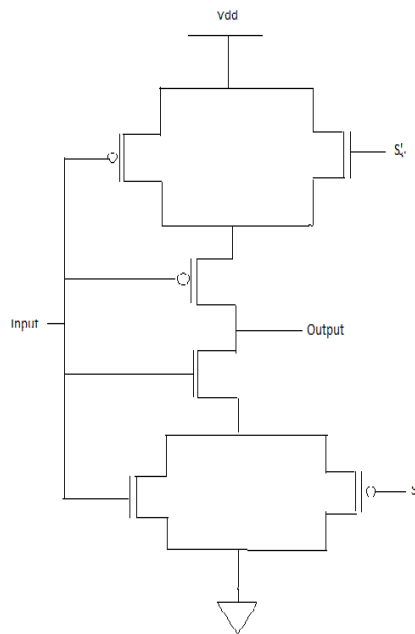

Figure-5. Sleepy stack approach.

PROPOSED METHODOLOGY

In FFT processors there will leakage power so to reduce these leakage power we are implementing some of the low power techniques. To reduce the leakage power problems researchers have proposed different ideas from the device level to the architectural level and thus designers are required to choose suitable techniques that satisfies application and product needs. The sleepy stack technique divides existing transistors into two halves like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. The new design which has been proposed will be having the characteristics of the sleepy stack but it has the ability to reduce leakage power better than sleepy stack approach. In modified sleepy stack approach n-mos sleep transistor is added parallel to divided pull up transistor and p-mos sleep transistor is added parallel to divided pull down transistor. By applying both existing and modified sleepy stack approaches to the FFT processor we will be comparing both the results. In these results the modified sleepy stack approach will be having reduced power than existing sleepy stack approach and it's about 0.005.

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Figure-6. Modified Sleepy Stack approach.

We have applied this modified sleepy stack in fft processor of each component to get the better output and compare these with existing methodology.

As shown in Figure-7 there will be dividing the existing P-mos and N-mos into two transistors by using stack approach. There will be adding sleep N-mos in between VDD supply and pull up network and P-mos in between ground and pull down network in multiplexer to reduce leakage power.
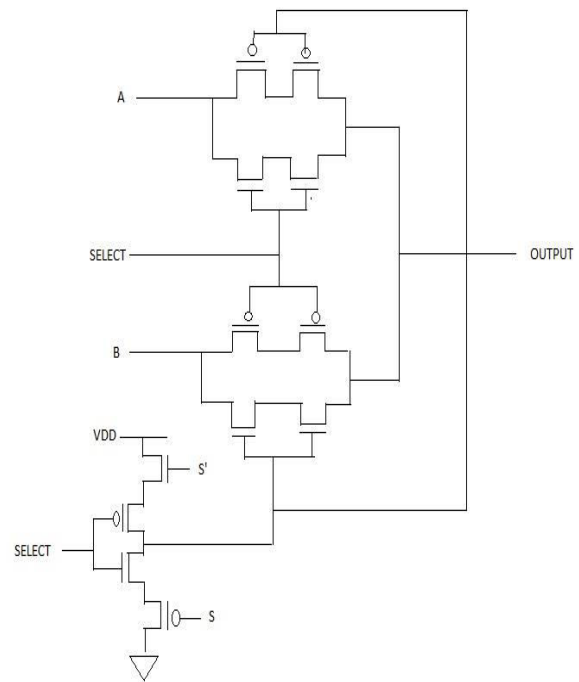

Figure-7. Modified multiplexer.

As shown in Figure-8 there will be dividing the existing P-mos and N-mos into two transistors by using stack approach at the input of the flip flop. There will be adding sleep N-mos at VDD supply and pull up network and P-mos at ground and pull down network in D flip flop to reduce leakage power.

Applying the both modified multiplexer and D flip flop in the FFT processor we can get better power reduction technique compared with the existing FFT processor of sleepy stack approach. The reason behind for applying the sleepy stack which is modified is due to its dual measuring of threshold voltage and better performance reducing the leakage current.

In further section we are going to analyze the both techniques by tabulating the results and drawing graph. This will be make us understand the difference between Average power, delay time and power delay product.

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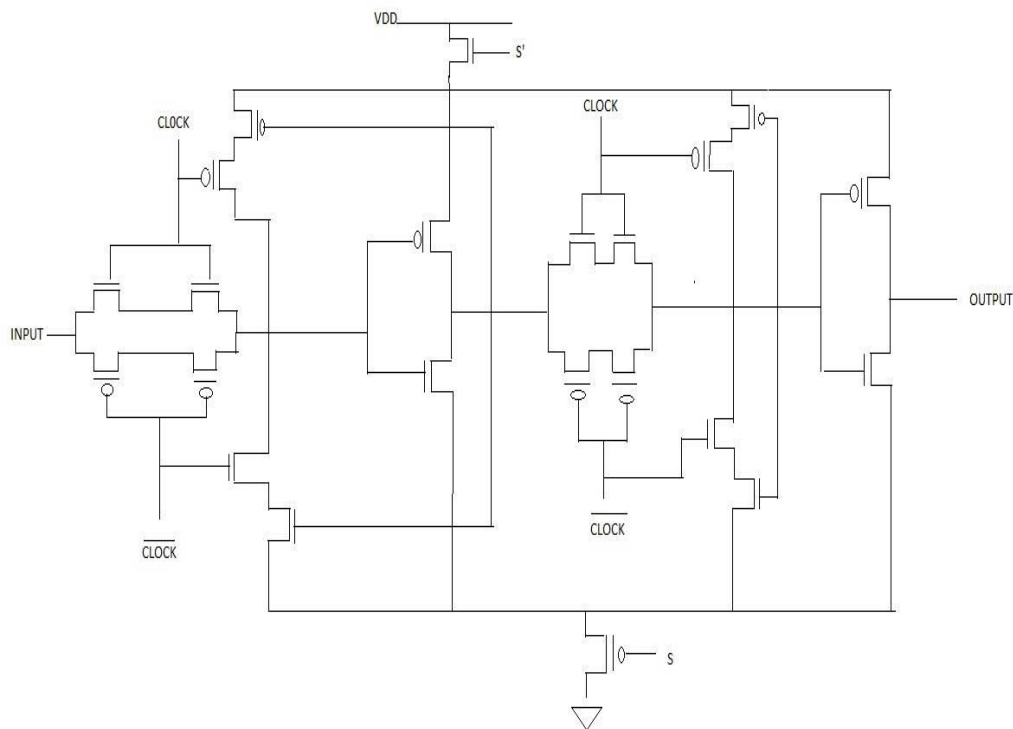
Figure-8. Modified D flip flop.

RESULTS AND DISCUSSIONS

In this section we are going to discuss about the out coming of the project, their resultant tables and graphs

FFT PROCESSOR AND ITS COMPONENTS SIMULATION OUTPUTS USING 130nm CMOS TECHNOLOGY

The following graph shows the final output of the FFT processor after applying the modified sleepy stack approach.
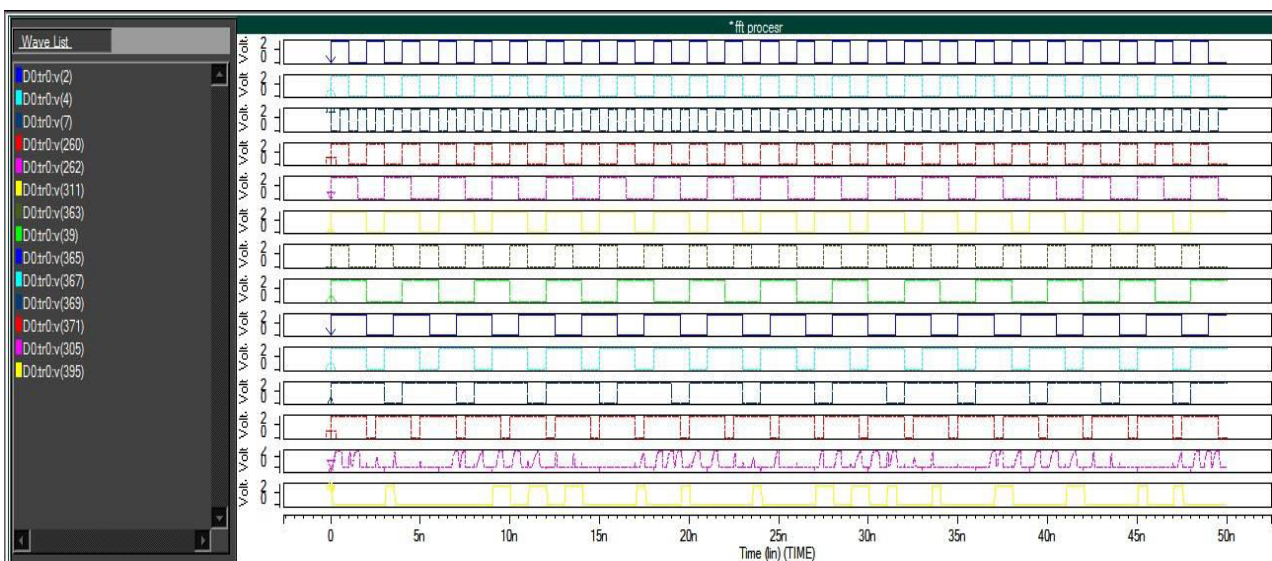
Figure-9. Simulation result of FFT output.

In the above graph as V (2) and V (4) are considered as the inputs to the FFT processor. The V (7) which is referred as the clock. The inputs which are given to the FFT are given as the inputs to the SRAM and the outputs are V (260) and V (262). The outputs of the SRAM are given as inputs to the D flip flop and the outputs are V (311) and V (363). These outputs are given as inputs to the first multiplexer and the output is V (39). There is a radix with outputs as V (367) and V (365). These outputs are given as inputs to another multiplexer and the output is V (369). The second

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output of the radix is given as input to the flip flop and the output will be V (371). The outputs of these will be input of another radix and gives the output of V (305). The final output which will coming out of the multiplexer which is V (355).

PERFORMANCE ANALYSIS

Table-1. Comparison chart of Average power in CMOS technology.

Device	Average power (Watts)
Existing FFT processor	571.1u
Sleepy stack FFT processor	112.8u
Modified Sleepy stack FFT processor	105.7u

The above table which tells about how much power will be consuming by each method which is applied to the FFT processor and tabulated them to make sure if there is any decrease in power. As the modified method will be having less power consumption and considered as best method.

**Table-2.** Comparison chart of Delay Time in CMOS technology.

Device	Delay time (Seconds)
Existing FFT processor	550.21p
Sleepy stack FFT processor	395.55p
Modified Sleepy stack FFT processor	390.22p

The above table which tells about the delay time which is consumed by each method used by the FFT processor and tells which method will be giving the least delay time.

Table-3. Comparison chart of Power Delay Product inCMOS technology.

Device	Power delay product (Joules)
Existing FFT processor	314.22f
Sleepy stack FFT processor	44.61f
Modified Sleepy stack FFT processor	41.24f

The above table which tells about how much energy will consumed by each of the method performed by FFT processor and tabulated for finding the least consumable energy FFT processor for the power saving and better use of the processor.
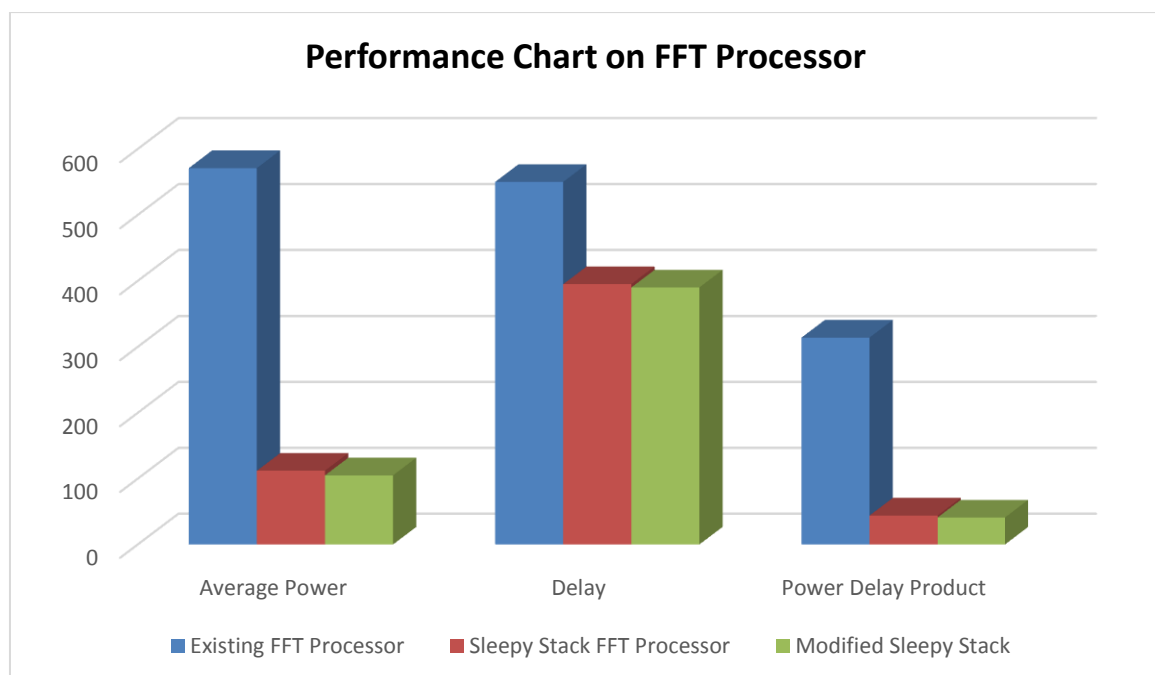
Figure-10. Performance chart on FFT processor.

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The graph states that there will power consumption among different methodology of the FFT processor and consider plotted graph between them. The difference is considered and the least power consumption will be considered as shown in Figure-10.

CONCLUSIONS

In this paper, the circuits were designed using 130nm CMOS technology. The circuits performance parameters power, delay and power delay product were compared. Later, the circuits designed with the Stanford model were modified using the low power techniques and the circuit parameters were compared with the base models. The simulation for 130nm MOSFET was carried out at 3.3 V. The transient, power, delay and power delay product analyses have been carried out. These observations are compared. It is noted that, the proposed circuits in 130nm MOSFET consumes less power than the existing circuits. The FFT architecture includes basic logic gates and basic digital circuits. The performance parameters like power, delay and power delay product for the D Flip Flop, Multiplexer, SRAM, Radix are measured and analyzed by using HSPICE tool. The FFT is designed using this CMOS and its parameters are also analyzed using the 130nm CMOS technology.

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