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A SYSTEM CONCEPTUAL DESIGN OF FLYBACK CONVERTER WITH SPLIT-PLANAR TRANSFORMER STYLE FOR SINGLE PHOTOVOLTAIC MODULE

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ABSTRACT

Flyback topology is considered as the lowest part count topology in Switched Mode Power Supplies (SMPS) family with isolated output capability. Without needing any output inductor the critical magnetic part to be considered within the circuit was only flyback transformer. Benefitting the recent advancement of a technology which used in constructing integrated circuits the reproducibility quality of the transformer could be guaranteed. Thus the new flyback topology with split-planar transformer style was introduced. Topology circuit simulation has been conducted and discussed within the model parameters of 5 W capacity, 500 to 1.5 MHz operation, 15 V output voltage with 80% efficiency, taking input from a single photovoltaic module. The most suitable pairs of power transformer to be microfabricated on a silicon wafer found to be 6 pairs with the core gap of 100 um at 1 MHz operation frequency.

Keywords: planar transformer, flyback converter, photovoltaic.

INTRODUCTION

Flyback converter topology has become the utmost high efficient yet low cost SMPS being used due lower part counts. The isolated multi-output capability has boost the converter to be the most used dc to dc converters in the world which is well known as a good solution for low power applications (Siyang Zhao, 2012).

However the most important components to be designed in the flyback converters is the transformer itself. In general, the flyback magnetic component has a different behavior than other common transformer does. Instead of directly transfer the energy in a forward fashion it needs to stores the energy during switch ON cycle and only transfer it to the secondary during the switch OFF cycle of the power switch. Thus the design of the flyback transformer is usually carried out merely to follow the design of an inductor compared to a normal power transformer (Salem *et al.*, 2006).

RECENT FLYBACK CONVERTER DEVELOPMENT

In recent modern technology advancement everything seems to get smaller and smaller. So does in SMPS, the basic parts such as resistor, capacitor, diodes, power switch has gone to surface mount technology (SMT) design except magnetic parts especially the transformer which still need human touch to wind, fine-tune and assemble their components. Figure-1 shows a basic circuit diagram of a power converter consisting of a flyback transformer. Herewith, even with the latest approach of planar design on PCB the transformer still seems to be the most noticeable bulky parts of all.

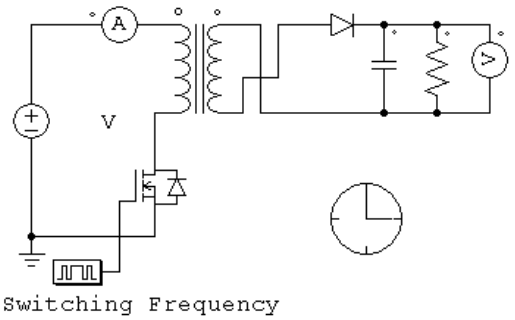

Figure-1. Basic circuit diagram of flyback converter with planar transformer.

In reaching hundreds of kilohertz moreover in megahertz operation the transformer cannot exempt from parasitic elements of L and C. Figure-2 shows a detailed transformer model including parasitic elements. The higher the frequency the more they become dominant parameters that significantly impact the design and performance of the converter. Of particular concern are the leakage inductances (Ll1 and Ll2) of the transformer which essentially inhibit the rapid, efficient transfer of energy from the primary to the secondary.

Furthermore, the leakage inductance leads to voltage spikes on the switch often necessitating the use of an over-voltage snubber circuit. The parasitic capacitances (C1, C2, and C12) also become important as their presence can lead to current in-rush, circuit resonance, and increased voltage stress on the output diode. Again, the harmful nature of these effects is more prominent and crucial in high, pulsed-power applications, (Prieto *et al.*, 1996), (S. Chung, 2004).

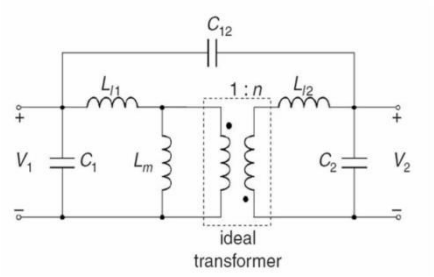

Figure-2. A detailed transformer model including parasitic elements (Salem *et al.*, 2006).

THE PROPOSED TOPOLOGY

In general, design step of flyback converter can be summarize as in Figure-3. Basically it required only information on four critical parameters which are output power, input voltage, switching frequency and expected efficiency.

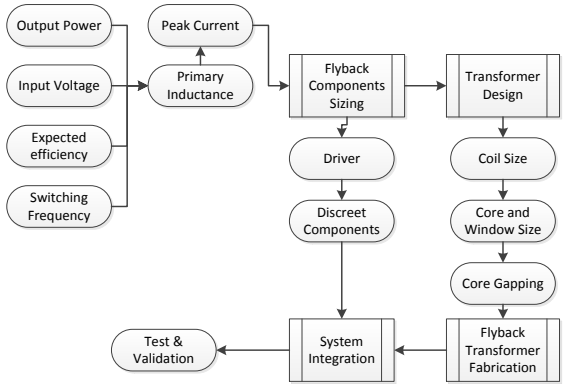

Figure-3. Design flow diagram of flyback converter.

Once the four parameters are opted, the design flow in Figure-3 can easily been followed. Based on literature (Forest, F. *et al.*, 2009), (Murthy-Bellur *et al.*, 2011) the flyback converter is best to perform up to 100 W only, but a higher output power are possible through stacking or paralleling. The practical input voltage is between 5 to 600 V which depend mostly on discreet component to cater the anticipated current and voltage within the circuit. Meanwhile the switching frequency usually depends on the practical available driver in the market. The higher the frequency the smaller the converter magnetic parts can be reduced. From the decided parameters, the primary inductance can be calculated as

$$L_{pri} = \frac{V_{in\_min}^2 \partial_{max}^2}{2fP_{out}} \quad (1)$$

L_{pri} = Primary inductance, H
V_{in_min} = Minimum input voltage, V
∂_{max} = Maximum ON time duty cycle
f = Switching frequency, Hz
P_{out} = Output power, W

Once the inductance is known, peak current I_{pk} can be calculated as

$$I_{pk} = \frac{V_{in\_min}\partial_{max}}{fL_{pri}} \quad (2)$$

Herewith the average current input power and the selection of power switch and discreet components can be made based on expected efficiency or estimated part losses. While the required core area, A_c and winding window area, W_a can be calculated as

$$W_a A_c = \frac{0.68 P_{out} d_w}{B_{max} f} \text{ m}^4 \quad (3)$$

d_w = Area of wire used in primary winding, m^2
B_{max} = Peak operating flux density, T

In the flyback magnetics design the most critical to consider was the gap formation, l_{gap} (xxx)

$$l_{gap} = \frac{0.4\pi L_{pri} I_{pk}^2}{A_c B_{max}^2} \quad (4)$$

A_c = Core window area, m
B_{max} = Peak operating flux density, T

Primary turn numbers, Npri and Nsec can be calculated as

$$N_{pri} = \frac{B_{max} l_{gap(actual)}}{0.4\pi I_{pk}} \quad (5)$$

$$N_{sec} = \frac{N_{pri}(V_{out}+V_{fwd})(1-\partial_{max})}{V_{in\_min}\partial_{max}} \quad (6)$$

With the advancement of CMOS technology the reproducibility issue faced by flyback transformer manufacturing is possible to be overcome. To prove our claim herewith we have introduced a split-planar transformer design as can be seen in Figure-4. Hereby the core and the coil traces are sliced and splitted into a few wedges and spread in paralleled style. The main advantages expected are the transformer will have a better temperature handling capacity, lower profile structure, high reproducibility quality and lower cost due it will be CMOS mass production compatible.

SIMULATION AND DISCUSSIONS

Detail fabrication technique of the flyback transformer is further explained in (A. R. Abdul Razak *et al.*, 2015). Meanwhile the simulation of flyback SMPS part is conducted using calculated parameters specification per Table-1. The assumption made was that this SMPS is getting voltage supply from a single panel PV module of 12 Vmin to 17 Vmax range. The system will convert the voltage into 15 Vdc, 5 W with 80% efficiency expectation. Within three different operating frequency, the simulation is to foresee the trend of primary inductance, core gap distance and parasitic capacitance effect of the flyback transformer.

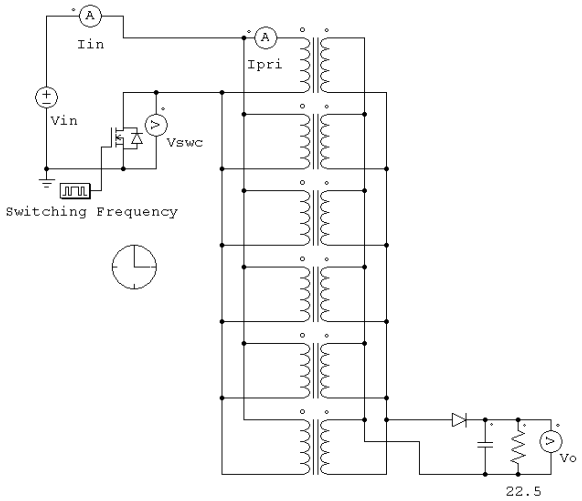

Figure-4. Circuit diagram of flyback converter with split-planar transformer design.

With ideal circuit of flyback topology the output waveform can be seen as per Figure-5 but when the parasitic capacitance of C1, C2 and C12 are incorporated the distortion can be seen per Figure-6.

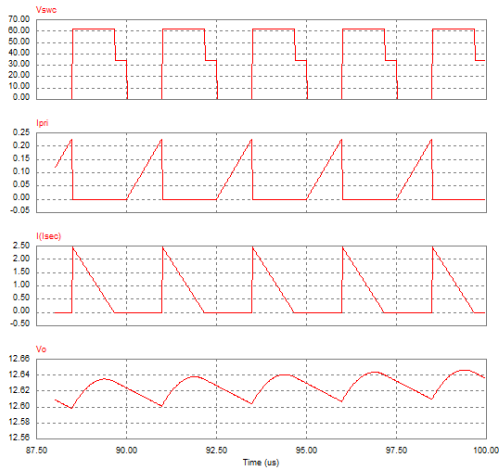

Figure-5. Output waveform of ideal flyback converter.

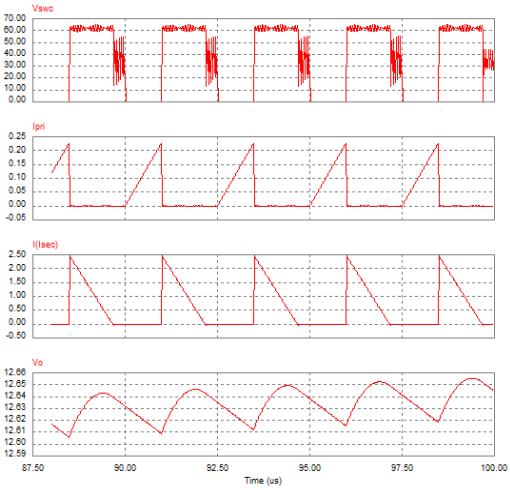

Figure-6. Output waveform of flyback converter with parasitic elements.

Table-1. Calculated parameters for split-planar flyback transformer design at 500 kHz operation.

Pair numbers	**P_{out}** (Watt)	**L_{prim}**(Henry)	**I_{pk}**(amp)	**Core Area** (mm^2)	**Gap** (mm)
1	5.00	$7.2x10^{e-6}$	1.667	133.8	0.208
2	2.50	$14.4x10^{e-6}$	0.417	47.3	0.073
3	1.67	$21.6x10^{e-6}$	0.185	25.7	0.040
4	1.25	$28.8x10^{e-6}$	0.104	16.7	0.026
5	1.00	$36.0x10^{e-6}$	0.067	11.9	0.018
6	0.83	$43.2x10^{e-6}$	0.046	9.1	0.014
7	0.71	$50.4x10^{e-6}$	0.034	7.2	0.011
8	0.62	$57.6x10^{e-6}$	0.026	5.9	0.009
9	0.55	$64.8x10^{e-6}$	0.020	4.9	0.007

It can be seen that the total handling power capacity of each transformer is distributed evenly per pair numbers cascaded in the system. Anyway the peak current I_{pk} and the core gap are more associated to the primary inductance of the transformer. The trends of both parameters are shown in Figure-7 and Figure-8.

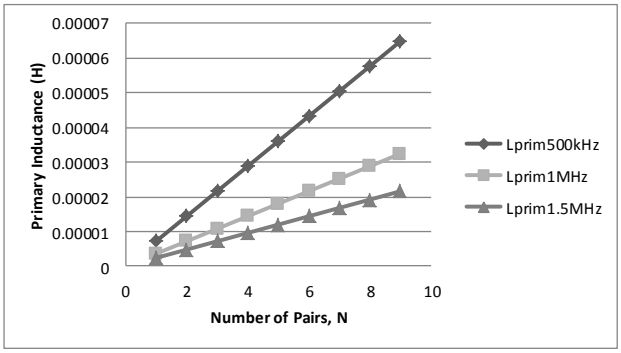

Figure-7. Primary inductance vs transformer pair numbers.

As the number of pairs increased the primary inductance value of each transformer increases linearly. When higher operating frequency was introduced, The slope decreases almost 50% at 1 MHz operation frequency. However, another 500 kHz increment of frequency does not much improving the slope as it only reduced the slope another 25%. Furthermore it is quite difficult to find in market the driver of such frequency of higher than 1 Mhz which conclude the 1.5 MHz operation option as not so practical.

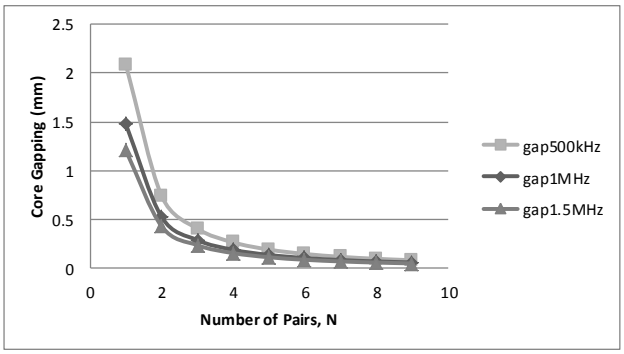

Figure-8. Core gapping distance vs transformer pair numbers.

At single core, the inductance value at minimum thus gap distance is at peak. When the transformer divided into multiple core side by side the cascaded inductance value of each parallel transformer reduces the gap value of each transformers. As the transformer is dedicated for a planar style to be fabricated on silicon wafer thus some constrain should be comprised. Standard thickness of the wafer is 500 um thus the practical gap should be less than 200 um only can be considered. Can be seen in the graph that at any of three frequency simulated the number of pairs for planar transformer can be built on the wafer is 4 pairs and above.

CONCLUSIONS

Flyback topology is considered as the lowest part count topology in SMPS family with isolated output capability. By assumption that using the recent advancement of CMOS manufacturing technology to solve the issues reproducibility quality of the transformer especially on the gap issue, the new conceptual design of flyback topology with split-planar transformer was discussed. Topology circuit simulation has been conducted within single photovoltaic module of 12-17 V input, 15 V output, 5 W power at 80 % efficiency. It come to conclusion that 1 MHz operation as the most practical environment operation with 6 pairs of 21.6 uH planar transformer fabricated on silicon chip with 100 um gap each.

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