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THE CONSEQUENCE OF SOURCE/DRAIN FACTOR TOWARD DRIVE CURRENT IN 10NM SOI MOSFET DEVICE

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ABSTRACT

Silicon on insulator (SOI) technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrate or known as a Buried oxide layer (BOX). SOI Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been introduced to enhance the drive current (I_{ON}) and low short channel effect (SCE). The virtual device fabrication and characterization were executed by using ATHENA and ATLAS modules from SILVACO TCAD tool. In this paper, an orthogonal array of L_9 in Taguchi method was used to analyze the consequence of Source/Drain factor toward I_{ON} in SOI Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device. Four process parameter (control factor) has been chosen to perform nine experiments considering the interaction effect towards 10nm SOI MOSFET, whereas two noise factor were varied for 2 levels to get four reading of I_{ON} for every row of the experiment. The signal-to-noise (S/N) ratio of a I_{ON} for an SOI MOSFET device is 56.40 dB and within the predicted range. As conclusion, it is shown that L_9 orthogonal array in Taguchi method is effectively can predict the best solution to finding the best setting level to produce the highest I_{ON}. Based on analysis of variance, S/D Implant energy is one of the significant factors that effecting I_{ON} in SOI MOSFET.

Key words: SOI, BOX, ANOVA, MOSFET.

INTRODUCTION

Over recent years, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices need to have good performance with low cost and low power dissipation (Mohamad *et al.*, 2013). With better Drive current (I_{ON}) there will be a better power dissipation thus increase the performance of the MOSFET. The most effective way to increase this performance is to scalling the gate length and gate oxide, scalling the gate oxide will lead to enchances the drive current and low short channel effect (SCE) but when we scale down this device the SCE becomes the major effect of the device and with the concept of high performance and low power dissipation becoming a major goal for MOSFET device Silicon on insulator (SOI) MOSFET been introduced. This silicon on insulator MOSFET have a very high performance compare to common Bulk MOSFET (Aziz *et al.*, 2014). With superior drive current and low leakage current has made this device has low power dissipation thus increases the performance of MOSFET devices.

Silicon on insulator devices first been introduced by J.E Lilienfield namely "method and Apparatus for controlling Electric currents" (Mehandia 2012). He proposed a three terminal device where the source to drain current is controlled by a field effect from the gate and is dielectrically insulated from the rest of the device. The active part of the device was built on a thin semiconductor film, which is deposited on insulator and this is the first SOI MOSFET been introduced (Mehandia 2012). Due to technology by that time that is 80 years ago this this concept very fast been forgotten due to technology on that era. This method then been implemented and practicable when the method of the separation of implanting oxygen technology (SIMOX) was introduced in 1966.The SOI or silicon on insulator MOSFET device has the advantage of speed up to 20 to 30 percent faster than normal MOSFET and it consumes only one third to one-half the power of bulk MOSFET. This criteria fulfill what current MOSFET needed that is low power dissipation and high performance of MOSFET device. Which this concept being introduced, it's necessary to increase this silicon on insulator (SOI) MOSFET to its maximum potential, thus the optimization of this device is important to give high end product.

Through a recent year, the Taguchi method has become a powerful tool for improving productivity during research and development so that high quality and low cost product can be achieved. This is because the Taguchi method is a systematic application of design and analysis of experiments for the purpose of designing and improving product quality at the design (Salehuddin *et al.*, 2012). Taguchi method is actually first proposed by the Englishman, Sir R.A. Fisher but this proposed method has no general guidelines for its application or the analysis of the results obtained by performing the experiments thus Taguchi constructed a special set of general design guidelines for factorial experiments that cover many applications. Taguchi method is a new method of conducting the design of experiments which are based on well defined guidelines. This method uses a special set of arrays called orthogonal arrays. These standard arrays stipulate the way of conducting the minimal number of experiments which could give the full information of all the factors that affect the performance parameter. The crux of the orthogonal array method lies in choosing the level combinations of the input design variables for each experiment.

In this paper, to identify semiconductor process parameters whose variability would impact most of the device characteristic is realized using Taguchi method. This research will focus on drive current and what

parameters are affected the most the value of drive current (I_{ON}). Drive current is one of certain aspects that important to silicon on insulator (SOI) device. Which is increasing the value of drive current the ratio of I_{ON} over I_{OFF} will be increasing thus lowering power dissipation of a device. In this research, the simulation of 10nm silicon on insulator MOSFET is done by using the ATHENA module while the simulation for electrical is done by using the ATLAS module of SILVACO software. They will proceed using L_9 orthogonal array that will have four different process parameter (control factor). These experiments will focus to the main control factor such as Halo implantation dose, Halo implantation energy, Source/Drain (S/D) implantation dose and Source/Drain (S/D) implantation energy. The use of Taguchi method to determine the process parameters with the highest Drive current (I_{ON}) was reported (Yang *et al.*, 2007). Optimization process parameter is the key step in Taguchi to achieve high quality without increasing cost. This is because optimization of process parameters can improve quality and the optimal process parameters obtained from Taguchi method are insensitive to the variety of environmental conditions and others noise (Esme 2009). By using orthogonal arrays to design the experiment could help the designers to study the influence of multiple controllable factors on the average of quality characteristic and the variations in a fast and economic way. Meanwhile, using a signal-to noise ratio to analyze the experimental data could help the designer of the product or the manufacture to easily find out the optimal parametric combinations (Salehuddin *et al.*, 2010).

EXPERIMENTAL

The process and device simulations of SOI MOSFET was used ATHENA and ATLAS modules of SILVACO TCAD tool respectively.

Designing SOI MOSFET device

Firstly, the main substrate which is P-type silicon with <100> orientation has been employed, followed by Buried Oxide Layer (BOX) formation. 200Å oxide layer was grown on top of silicon bulk. This oxide layer is significant as it has been employed as a mask during P-well implantation process. Later in the doping process was finished, the oxide layer has been engraved and it was followed by annealing process. The purpose of annealing process was to beef up the device‟s structure. Afterwards that, shallow trench isolation (STI) has been taken in parliamentary procedure to isolate the neighbor transistor. A 130Å stress buffer has been used on the wafers with 25 min diffusion processes. LPCVD process, or known as Low-Pressure Chemical Vapor Deposition has been utilized to deposit a 1350Å nitride layer. The use of nitride layer was to behave as a mask when silicon was etched to expose the STI area.

Photo resistor layer was then banked on the wafer layer and any unwanted parts were etched away using the Reactive Ion Etching (RIE) process. The primary function of oxide layer grown on the trench sides was to rid of impurity from entering the silicon substrate. After that, to eliminate extra oxide on the wafer, the chemical Mechanical polishing (CMP) was applied. A sacrificial oxide layer was then developed and etched to eliminate any flaws on the surface (Mansor *et al.*, 2013). The gate oxide must be produced before the Boron Difluoride (BF_2) threshold-adjustment procedure. The polysilicon gate was then deposited and followed by halo implantation. To receive a better and optimum performance for MOSFET device, indium was doped. Sidewall spacer was then banked to a mask for source/drain implantation. Arsenic was implanted with an appropriate value of concentration to get smooth current flow in NMOS device. After that, the silicide layer has been grown and annealed at the top of polysilicon. The next stage is to deposit Boron Phospor Silicate Glass (BPPG) layer. This stratum was a Premetal dielectric (PMD) which is the first layer deposited on the wafer surface when transistor produced. The transistor was then linked to aluminum metal. After that, the second aluminum layer was deposited on top of the intel-Metal Dielectric (IMD) and unwanted aluminium was etched to make the contacts (Elgomati *et al.*, 2011). The measure was completed when etching and metallization was performed for electrode formation and bonding pads were opened. Figure-1 shows how BOX formation has been deposited.

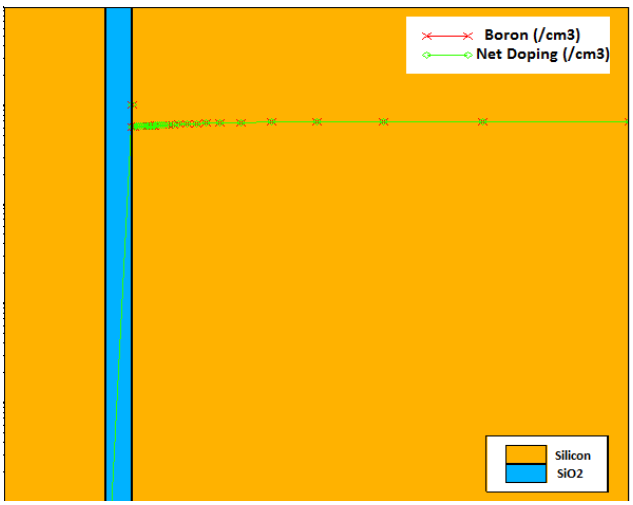

Figure-1. BOX formation

Meanwhile, Figure-2 shows the block diagram of SOI MOSFET in designing stage, but the most important thing and crucial in this stage is Buried oxide thickness (BOX) formation (Aziz *et al.*, 2014).

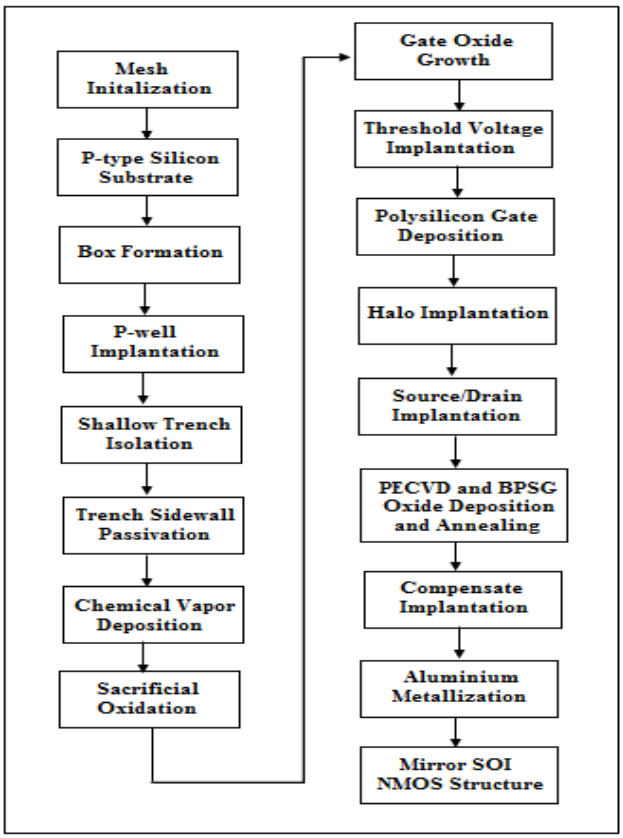

Figure-2. Block diagram of designing stage for SOI MOSFET.

Optimization stage

In this optimization stage the method that's going to be used is the Taguchi method L9 orthogonal array. This L9 orthogonal array needed four process parameter and two noises factor to enable the design to proceed creating four sets of experiment consisting 46 experiments. This two noise factor is needed to ensure that the result taken more insensitive to variation, thus it will apply when design been in process fabricated later. Generally L_9 orthogonal array needed four process parameter and two noises factor to proceed. Table-1 indicates the layout of L_9 orthogonal array in Taguchi method. A, B, C and D are the parameter that will be optimized (Phadke, 1998).

Table-1. L_9 (3^4) orthogonal array level layout.

Experiment No.	Control Factors			
	A	B	C	D
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

Taguchi L9 (3^4) orthogonal array involving four process parameters at three different levels with two noise factors included. Therefore, a total of 36 runs are required to optimize the process parameters in SOI MOSFET device. All the values of process parameters and noise factors with their corresponding levels are enlisted in Table-2 and Table-3 respectively. Table-2 specifies the noise layout for L_9 orthogonal array. As said before this, the noise factor is crucially needed to make sure the design structure of SOI MOSFET insensitive to variant, so while it's been fabricated it will not be effected (Phadke, 1998).

Table-2. Process parameters and their levels.

Sym	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Halo implant Dose	atom/cm^3	4.81E13	4.82E13	4.83E13
B	Halo Implant Energy	keV	178	180	182
C	Source/ Drain Implant Dose	atom/cm^3	1.72E14	1.73E14	1.74E14
D	Source/Drain Implant Energy	keV	11	12	13

Table-3. Noise factors and their levels.

Symbol	Noise Factor	Unit	Level 1	Level 2
M	Sacrificial oxide temperature	^{o}C	950	951
N	Annealing process temperature	^{o}C	910	912

RESULTS AND DISCUSSIONS

Optimization of 10nm SOI MOSFET device

The process parameter that has the most influence on the device characteristic can be determined by analyzing the outcome that has been recorded in Table-4. With this result the scalling factor and adjustment factor can be identified during the optimization stage. To find out the optimal process parameter, the signal-to-noise ratio has been recorded. The drive current in this experiment is using S/N ratio the larger the better.

Table-4. Drive current value for SOI MOSFET device.

Expt No.	I_{ON} (μA/μm)			
	M_1N_1	M_1N_2	M_2N_1	M_2N_2
1	336.0	336.12	336.50	336.38
2	661.15	661.94	661.46	662.26
3	676.42	686.29	676.74	685.34
4	633.85	646.91	634.13	647.23
5	371.08	371.31	371.62	371.85
6	644.11	644.41	644.61	644.92
7	666.38	666.71	667.42	667.78
8	620.32	620.59	625.88	626.19
9	364.91	364.61	364.80	365.03

As for value of S/N ratio, it is always indicated that the bigger the value of a ratio, the better the performance of characteristic of the design device that's been experimented. So the most optimize level in this research will be the highest signal-to-noise (S/N) ratio (Salehuddin *et al.*, 2014). With the highest S/N ratio, the value of drive current (I_{ON}) will also at the highest peak value.If the value of drive current (I_{ON}) is high, so the ratio of I_{ON} over I_{OFF} is also high. It indicates the low power consumption of the device. The S/N ratio (Larger the better), can be expressed as (Phadke 1998):

$$SNR = 10log\left[\frac{1}{n}\sum {}^{1}/_{yi^2}\right] \quad (1)$$

where *n* is the number of tests and *Yi* is the experimental values of drive current (I_{ON}). By utilizing formula given in Equation (1), the SNR for each row of experiments were computed and recorded in Table-4. The optimization using L_9 orthogonal array has been conducted for larger the better analysis of the device. All four parameters which are halo implantation dose, halo implantation energy, source drain (S/D) implantation dose and source drain (S/D) implantation energy are indicating that there is only one dominant factor which is Source/Drain implantation energy. Source/Drain (S/D) implantation energy leads the percent with 99%, followed by S/D implantation dose (1%), halo implantation dose (0%) and energy (0%). Signal-to-noise ratio has been analyzed and been recorded in Table-5.

Table-5. MSSQ and S/N ratio value for SOI MOSFET device.

Experiment number.	Mean sum of squares (MSSQ)	S/N ratio (Larger-the-Best)
1	8.84E-06	50.53
2	2.28E-06	56.41
3	2.16E-06	56.66
4	2.44E-06	56.13
5	9.30E-01	51.40
6	2.41E-06	56.18
7	2.25E-06	56.48
8	2.57E-06	55.89
9	7.51E-06	51.24

Refer to Table-5, it can be seen distinctly that in row 2, row 3 and row 7 was the highest S/N ratio. With a value of 56.66dB, row 3 lead all the others with 0.25 dB different from the second highest that is row 2 with a value of 56.41dB follow by row 7 that is 56.48dB. The high value of the S/N ratio for these 3 rows clearly shows that these 3 rows have best possible combination of the response and also indicates that this combination have the most insensitivity for the response characteristic. Since the experimental design stage is orthogonal arrays, the S/N ratio of each process parameter can be separated out (Phadke, 1998). The full outcome of S/N ratio (SNR) for each process parameter with a total mean of SNR is recorded in Table-6.

Table-6. SNR of Process Parameters in SOI MOSFET Device.

Process Parameter	SNR (Larger-the-best)			Overall mean SNR
	Level 1	Level 2	Level 3	
A	54.54	54.57	54.54	54.55
B	54.38	54.57	54.70	
C	54.20	54.59	54.85	
D	51.06	56.36	56.23	

Based on the data in Table-6, the factor effects graph for SNR (Lower-the-better) is plotted as illustrated in Figure-3. The dashed on the graph indicated the overall mean of the S/N ratio which is 54.55dB.

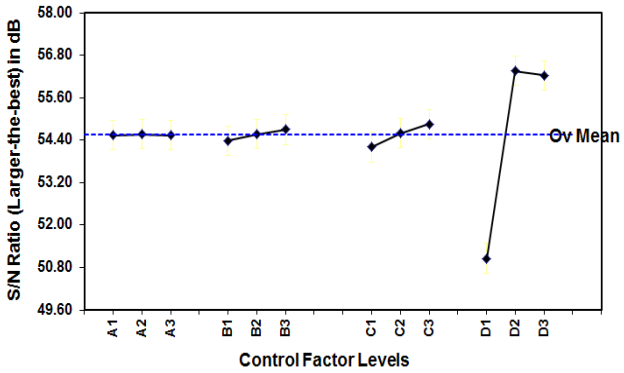

Figure-3. S/N ratio (Larger-the-better) graph.

From the graph, it can be observed that factor A1, B1, C1 and D2 have been selected as the optimum value due to their higher SNR. Factors A, B, C and D represent Halo Implantation Dose, Halo Implantation Energy, S/D Implantation Dose and S/D Implantation Energy respectively. The bigger the value of S/N ratio, the better quality of characteristics for drive current (I_{ON}) (Phadke, 1998).

Analysis of variance (ANOVA)

Through the comprehensive study, the most effecting parameter with respect to drive current (ION) was investigated to ensure the truthfulness of the optimum combination of all control factors. The result of analysis of variance (ANOVA) for the 10nm SOI MOSFET as shown in Table-7. The factor effect of process parameter is clearly showing that this factor dominantly affecting the S/N ratio to reduce variation. The higher the percentage of factor effect (process parameter), the greater it will affect the stability of the response characteristic with respect to the noise parameters (Phadke 1998). ANOVA is a common statistical technique to determine the percent contribution of each factor that could significantly affect the drive current (I_{ON}) in SOI MOSFET device.

Table-7. Result of ANOVA.

Process parameter	DF	SS	MS	Factor effect on SNR (%)
A	2	0	0	0
B	2	0	0	0
C	2	1	0	1
D	2	55	27	99

Based on Table-7, S/D implantation energy is observed to be the most significant process parameter in increasing drive current (I_{ON}) value with percentage of 99%. Other process parameters are recognized as neutral (pooled) as they do not have much effect on drive current (I_{ON}) value.

Optimization runs through suggested setting

The best possible result of optimization based on ANOVA analysis is A3, B3, C2 and D2. The optimize setting that suggested by Taguchi method is recorded in Table-8.

Table-8. Best setting of the process parameters.

Factor	Process parameter	Unit	Level	Best value
A	Halo implant dose	atom/cm^3	3	4.83E13
B	Halo implant energy	keV	3	182
C	Source/Drain Dose	atom/cm^3	2	1.72E14
D	Source/Drain Energy	keV	2	13

The value of SNR (Larger-the-better) of the drive current (I_{ON}) for an SOI MOSFET device is 56.40dB. This value was observed to be in the range of the predicted SNR where the range is between 56.94dB and 55.78dB (56.36±0.58). Its show that L9 orthogonal array in Taguchi method is effectively can predict the best solution to finding the best setting level to produce the highest drive current (I_{ON}) on SOI MOSFET device. The verification test was then run by utilizing ATHENA and ATLAS module. The highest drive current (I_{ON}) value obtained was 660.42µA/µm as shown in Table-9.

Table-9. Optimum result of drive current value.

I_{ON} (µA/um)				SNR (Larger-the-better)
I_{ON1} (M_1N_1)	I_{ON2} (M_1N_2)	I_{ON3} (M_2N_1)	I_{ON4} (M_2N_2)	
659.93	660.243	660.59	660.90	56.40dB

The maximum value of drive current (I_{ON}) was successfully achieved by using Taguchi method along with nominal threshold voltage (V_{TH}) of 0.285V (±12.7% of ITRS 2013 prediction) (ITRS 2013), very low leakage current (I_{OFF}) of 28.45pA/µm and high I_{ON}/I_{OFF} ratio of $23.21x10^6$.

CONCLUSIONS

As a conclusion, Silicon on insulator MOSFET is a device that certainly superior than common bulk MOSFET and through this experiment its clearly shown that the Taguchi method is reliable method in achieving the optimum solution in fabricating a nanoscale MOSFET device. The drive current (I_{ON}) is one of the important electrical characteristic that determine power consumption or power dissipation of a MOSFET. This is because with a higher I_{ON} value over I_{OFF}, lower the power consumption of the SOI MOSFET device.

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