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DESIGN AND ANALYSIS OF RF LOW NOISE AND HIGH GAIN AMPLIFIER FOR WIRELESS COMMUNICATION

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ABSTRACT

This paper deals with the design of Low Noise Amplifier using MODFET for Wireless Communication. The proposed LNA will be operating at 6 GHz and uses two stages for improved gain and low noise figure. The first stage is based on Common source which is followed by the second stage of cascoding configuration. The transistor used in this design is based on p-HEMT technology from Sirenza micro devices. Advanced Design System (ADS) is used to design this LNA. The individual stages include capacitors and inductors for DC bias. The input and output matching networks are designed using microstrip transmission lines. The simulation results show gain of 28.27 dB and noise figure as 0.83 dB at 6 GHz with biasing voltage at 3.0 V.

Keywords: two-stage LNA, p-HEMT, ADS, gain, noise figure.

1. INTRODUCTION

Low Noise Amplifier is the key component in almost all wireless communication systems. It plays a vital role of reducing the noise from signal received from antenna. The gain of this amplifier is also important as it will reduce the noise figure of next stages. This concept is mathematically illustrated by Friis formula as

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \quad (1)$$

where F_{total} is total noise figure of the system, n is the number of stages, G is the gain of the stage. The proposed design finds its application in IEEE C Band, satellite communication.

A. Basic LNA design

The basic LNA design has three main stages: Amplifier, input matching network & output matching network. This is shown in Figure-1. Amplifier is designed for stability, low noise figure and high gain. The input and output matching networks ensures the maximum power transfer.

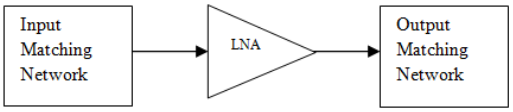

Figure-1. Basic LNA design.

B. Two-Stage design

The comparison among various topologies reveals that Common Source (CS) configuration exhibits the lowest noise figure and moderate gain. In contrast, cascode configuration offers the highest gain but slightly higher noise figure than CS topology [11]. The aim of this paper is to take advantage of these two topologies in efficient manner to achieve both low noise figure and high gain. The first stage comprises of CS configured LNA design providing the sufficient suppression of noise and the second stage is designed for improving gain of the amplifier using cascode configuration [13]. The amplifier design proposed in this paper is based on two-stage amplifier as shown in Figure-2.

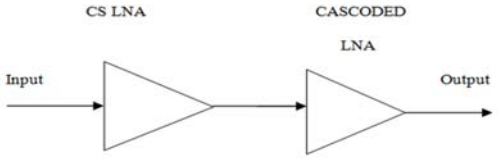

Figure-2. Two stage LNA design.

2. AMPLIFIER DESIGN

A. Device selection

The selected device must satisfy the stability criteria, provide high gain and low noise figure. P-HEMT transistors have high added efficiencies and excellent low noise figures and performance. As our goal being sub-1 dB noise figure, pHEMT GaAs FET may be suitable and is widely used in satellite communication. SPF-2086 TK from Sirenza Microdevices is a high performance 0.25µm pHEMT Gallium Arsenide FET with Schottky barrier gates [1]. This device has 0.7 dB minimum noise figure and maximum gain of 13.5 dB under matched conditions with biasing voltage of 3 V and drain current, 20 mA.

The device has to be verified for its stability using Rollett's Stability Factor based on S-parameters, defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}.S_{21}|} \quad (2)$$

where $|\Delta| = S_{11}S_{22} - S_{12}.S_{21}$. The conditions for a transistor to be unconditionally stable are $K > 1$ and $|\Delta| < 1$. The S-

parameter values are obtained from datasheet and the value of K is found to be greater than 1. The stability of the device is also verified using ADS and the results are shown below.

B. First stage design

In this design, the inductors and capacitors are used for DC biasing of amplifier. The input and output matching networks are designed using microstrip lines. Microstrip lines are widely used for matching networks in RF design circuits as they provide easy integration and good mechanical support.

The values of inductance and capacitance are calculated using Smith Chart utility from ADS by taking stability, optimum gain and lowest possible noise figure. The substrate used in this design is Duroid RO3006. For matching network design, the electrical lengths of the open stub microstrip lines are calculated using Smith Chart Utility in ADS and optimized for low noise using the parameters mentioned in the datasheet [2]. For matching network design, the electrical lengths of the open stub microstrip lines are calculated using Smith Chart Utility in ADS and optimized for low noise. The matching impedance is chosen to be 50 ohm which is common in LNA design. This produces gain value 13.2 dB and noise figure as 0.8 dB. The design of the single stage CS configured LNA is shown in Figure-3.

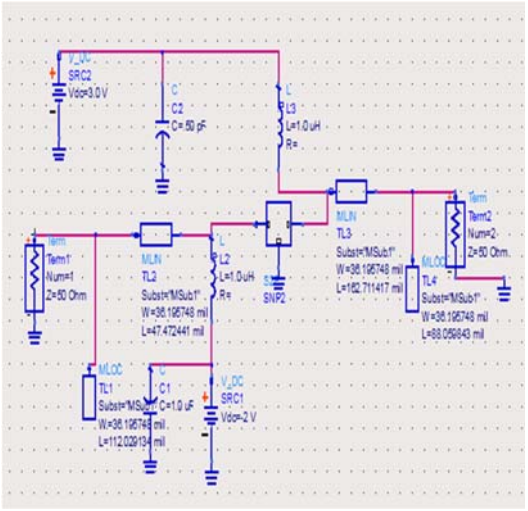

Figure-3. Design of common source LNA.

C. Second stage design

The second stage is designed with cascode configuration. This is chosen because of its advantage of reducing Miller effect capacitance and can be used in higher frequency range. This produces gain value 16 dB and noise figure as 0.957 dB. The design is shown in Figure-4.

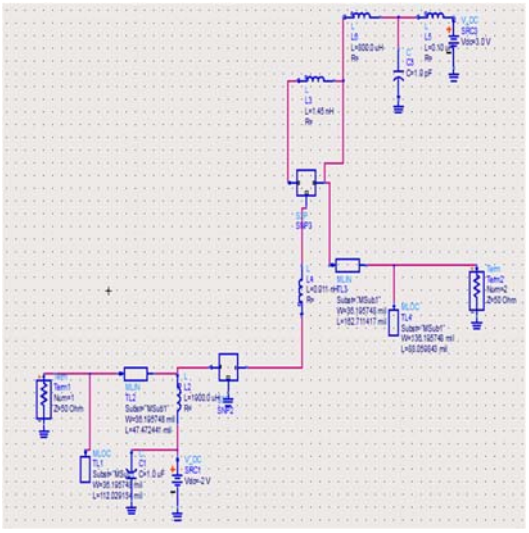

Figure-4. Design of cascode LNA.

D. Cascaded design

Cascading of two stage amplifier improves gain as equal to the sum of the gain of two stages. Cascading does not only improve the power gain but also has significant effect of amplifying noise. Hence, decision of cascading LNA should be made careful. As discussed earlier, CS configuration provides the lowest possible noise figure and hence, made as first stage of the amplifier design. Next, to improve gain, it is cascaded with cascode LNA and it is shown in Figure-5.

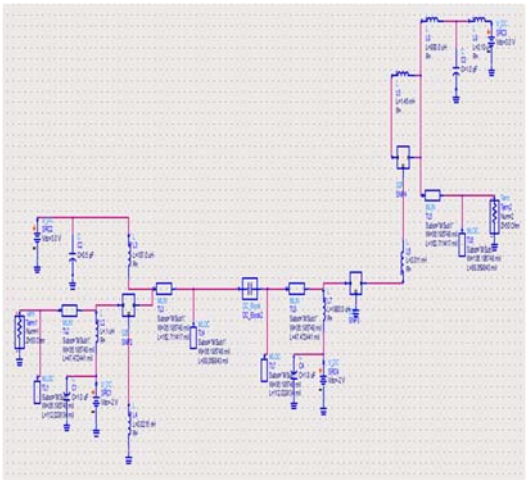

Figure-5. Design of cascaded LNA.

4. RESULTS AND DISCUSSIONS

The designs are simulated in ADS. The major LNA parameters like gain, noise figure, S-parameters and VSWR are calculated with respect to frequency range from 1 GHz to 10 GHz.

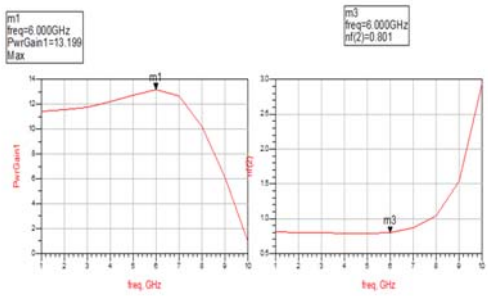

Figure-6. Gain and noise figure of common source LNA.

Single stage (common source) LNA produces a gain value 13.2 dB and noise figure as 0.8 dB. The simulation results have been shown in Figure-6. The S-parameters of common source amplifier are shown in Figure-7. The results shows that, for the operating frequency at 6 GHz, S (1,1) is -12.913 dB, S (2,1) is 13.19 dB, S (2,2) is -14.609 dB and S (1,2) is -18.188 dB. This design has good reverse isolation, sufficient input and output reflection co-efficient and forward gain of 13 dB.

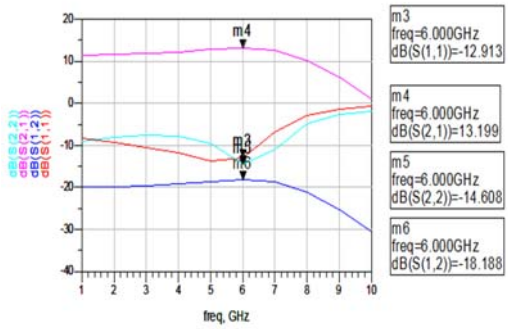

Figure-7. S-parameters of CS amplifier.

The simulation results of cascade design such as Power gain, Noise figure, S-parameters with respect to frequency are shown in Figures 8 and 9. The cascode amplifier produces gain value 16 dB and noise figure as 0.957 dB. Compared to the single stage common source design, the cascode design has higher gain at the cost of noise increase by 0.15 dB.

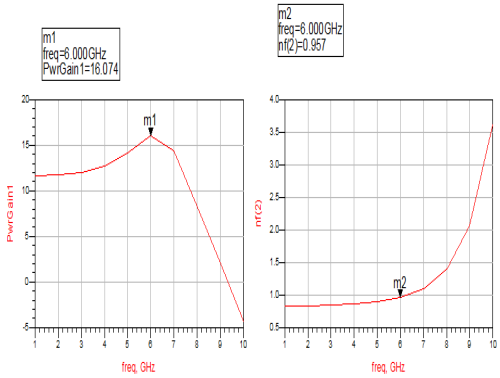

Figure-8. Gain and noise figure of cascode LNA.

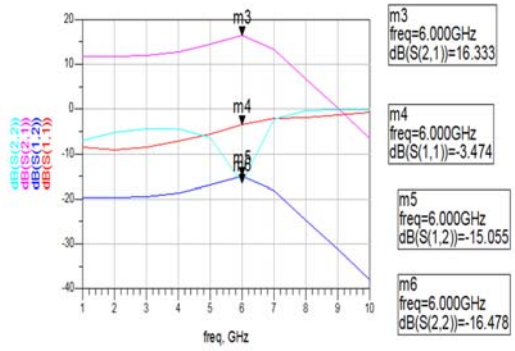

Figure-9. S-parameters of cascode amplifier.

The single stage provides lowest possible noise figure and the second stage offers good gain, using these two merits and the cascaded LNA has designed. The simulation results show gain and noise value as 28.28 dB and 0.83 dB respectively at 6 GHz. The gain performance, noise performance and S-parameters are shown in Figures 10 and 11.

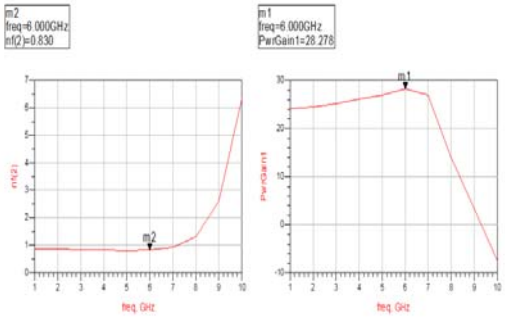

Figure-10. Gain and noise figure of cascaded LNA.

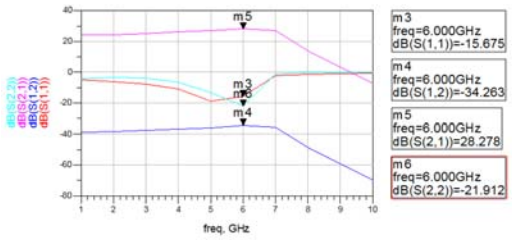

Figure-11. S-parameters of cascaded amplifier.

The results of the common source, cascaded and cascaded LNA designs are compared with the existing similar works and the results are given in the Table-1 to Table 3. These show the achieved results are comparatively better than previous works.

Table-1. Comparison of common source design.

Parameter	Designed CS LNA	Existing Ref [3]	Existing Ref [4]
Transistor	p-HEMT	GaAs FET	GaAs MESFET
Frequency (GHz)	1-6	1-8	5 – 6
Noise Figure (dB)	0.801	0.81	1.26
Gain (dB)	13.199	13.12	15.83

Table-1. Comparison of cascode design.

Parameter	Designed CS LNA	Existing Ref [5]	Existing Ref [6]
Transistor	p-HEMT	CMOS	CMOS
Frequency (GHz)	1-6	1-2.4	3- 10 GHz
Noise Figure (dB)	0.95	2.8	3.85
Gain (dB)	16.1	14.5	15.04

Table-3. Comparison of Cascaded design.

Parameter	Designed CS LNA	Existing Ref [7]	Existing Ref [8]
Transistor	GaAs FET	GaAs FET	CMOS
Frequency (GHz)	1-6	3.7 - 4.2	2.4
Noise Figure (dB)	0.83	1.1	2.65
Gain (dB)	28.278	25.4	25.27

These tables show that the noise performance is better in CS design than cascode design. But, gain is better in cascode than CS design. As noise at the first influences the overall system, the final cascaded LNA has CS design as its first stage followed by cascode which has better gain. Thus, the cascaded design has reasonably less noise figure and high gain shown in Table-4.

Table-4. Design performances comparison.

Topology	Noise figure (dB)	Gain (dB)
Common Source LNA	0.8	13.2
Cascode LNA	0.95	16.1
Proposed Cascaded LNA	0.83	28.278

5. CONCLUSIONS

The proposed LNA has designed using common source amplifier cascaded with cascode amplifier. This LNA is designed using SPF- 2048 TK transistor, which is based on PHEMT technology operating at 6 GHz. The designs are simulated using ADS and the overall gain & noise figure are obtained. At 6 GHz frequency, the designed low noise amplifier exhibits low noise, moderately high gain, and good input and output return loss. The CS amplifier provides gain of 13.2 dB with noise figure as 0.8 dB and the cascoded design offers gain of 16.1 dB and noise figure as 0.95 dB. The designed cascaded LNA produces gain of 28.278 dB and noise figure of 0.83 dB. The gain is improved by 11.3 % and the noise figure has been reduced by 24.54 % when compared to the reference work [7]. The gain is improved by 11.9 % and the noise figure has been reduced by 68.7 % when compared to reference work [8].

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